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MG2475

(No.ADS1101)

Revision 1.0

July 2015

DataSheet

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Revision History

Revision No.	Date	Description
V1.0	2015-07-30	• First version is released.

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1 INTRODUCTION

MG2475AZZ-F340C (hereinafter called “MG2475”) is a true 2.4 GHz system-on-chip (SOC) designed for low-power and low-cost applications based on industry standards, IEEE802.15.4 and RF4CE. Some special features and peripherals such as peripherals DMA, memory and I/O retention under the power down modes, etc are added to achieve both enhanced performance and low-power. MG2475 uses an ISM band of 2.4 ~ 2.48 GHz. In addition to the standard 250Kbps data-rate specified in IEEE802.15.4, enhanced high data-rate mode (1Mbps) with channel coding is supported.

MG2475 combines an advanced RF transceiver with an industry-standard enhanced 8051 MCU, a baseband PHY, a MAC with AES-128 HW engine, an in-system programmable 64KB flash memory, a 7-KB RAM, and many other application-specific peripherals. For voice applications, the voice encoder/decoder of ADPCM and μ/a-law are embedded.

MG2475 fits best for low-cost and low-power RF4CE remote control applications.

APPLICATIONS

-2.4 GHz IEEE 802.15.4 Applications

- RF4CE Remote Control Systems
- Lighting Systems
- Voice Applications
- Home/Building Automation
- Industrial Control and Monitoring
- Energy Management
- Low Power Wireless Sensor Networks
- Consumer Electronics
- Health-care equipment
- Toys

2 KEY FEATURES

RF Transceiver

- Integrated 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of –98.5 dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9.0dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- High Data Rate including 250Kbps specified in IEEE802.15.4: 1Mbps
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 128-byte FIFOs for Modem Tx and Rx
- CRC-16 Computation and Check
- Address filtering enhanced
- Voice MAC header H/W generation

8051-Compatible MCU

- 8051 Compatible (single cycle execution)
- 64KB Embedded Flash Memory
- 7KB Data Memory (support the retention in all power down modes, power-off is possible)
- 128-byte CPU dedicated Memory(support the retention in all power down modes, power-off is possible)
- 1KB Boot ROM
- Dual DPTR Support
- 4-channels peripheral DMA(channel 0 is only for MAC RX)
- AES-128 Encryption/Decription Engine
- ECC(Error Checking and Correction) logic for the Flash or RAM data integrity
- I2S/PCM Interface with two 128-byte FIFOs
- μ-law/a-law/ADPCM Voice Encoder/Decoder
- Two High-Speed UARTs with Two 16-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer

- Sleep Timer using the 32kHz internal RC-OSC
- Quadrature Signal Decoder
- 22 General Purpose I/Os (support the retention in deep sleep mode)
- 16 MHz RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- SPI Master/Slave Interface with two 16-byte FIFOs
- I2C Master/Slave with 16-byte FIFO
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

Clock Inputs

- 32MHz Crystal for System Clock

Power

- 1.2V(Core)/2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))

Package

- Lead-Free 40-pin QFN Package (6mm x 6mm)

3 BLOCK DIAGRAM

[Figure 1] shows the block diagram of MG2475. MG2475 consists of a 2.4GHz RF, a baseband PHY, a MAC hardware engine, an industry-standard enhanced 8051 MCU, an in-system programmable flash memory 64KB, a 7KB data RAM, and rich peripherals such as a voice encoder/decoder block, I2C, 5-channel PWM.

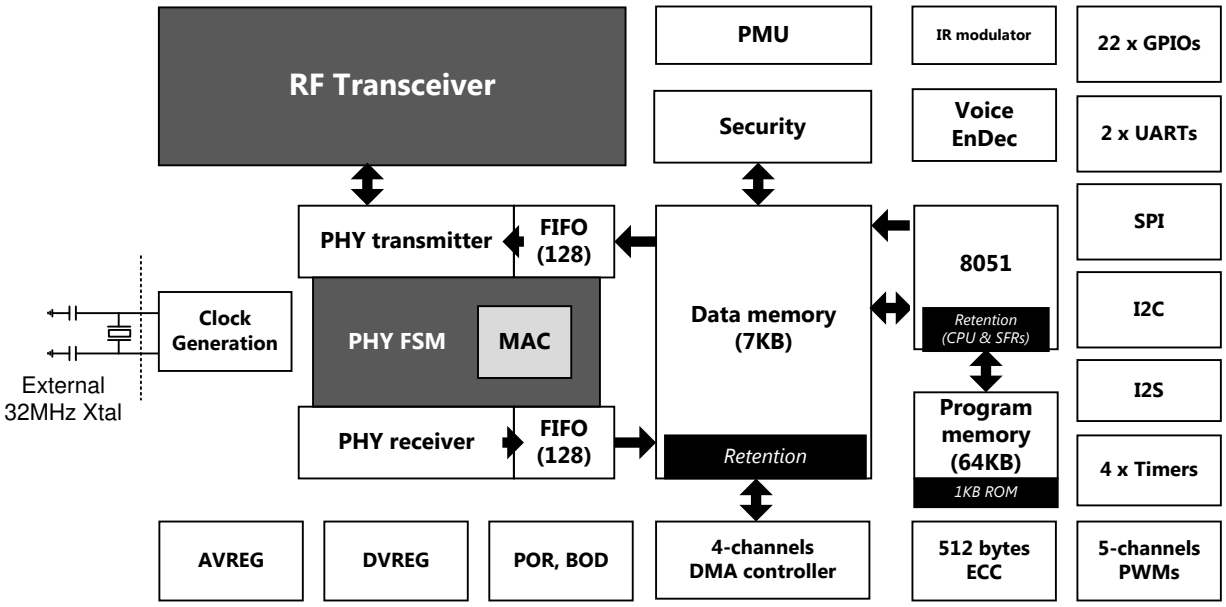


Figure 1. Functional Block Diagram of MG2475

MG2475 integrates an RF transceiver compliant to IEEE802.15.4 RF. The RF transceiver operates on an ISM band of 2.4 ~ 2.48GHz with excellent receiver sensitivity and programmable output power up to +9dBm.

The MAC block supports IEEE802.15.4 compliant functions and it is located between the microprocessor and the baseband modem. MAC block includes FIFOs for transmitting/receiving packets, a CRC generation and the enhanced address filtering and its control circuit. In addition, it supports automatic CRC check and address decoding. And AES engine for security is accessed like the general 8051 peripheral and operated through direct data memory access without 8051 intervention. Also, MG2475 supports the ECC (Error Checking and Correction logic) code generation per 512-bytes for guaranteeing the reliable memory data integrity.

The 4-channels DMA block enables efficient, high-speed operation of the peripherals such as UARTs, SPI, etc by reducing the load on the CPU. The DMAC of MG2475 only supports the data transfer between peripheral FIFOs and the DMA buffers in data memory. The channel-0 of DMAC is only for the baseband modem RX FIFO.

MG2475 integrates a high performance embedded microcontroller, compatible to industry standard 8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single

cycle.

The memory part of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanations, refer to Section 7.1.2 Data Memory.

MG2475 includes 22 GPIOs and rich peripherals to aid in the development of the application circuit with the various external peripherals interface. All I/O pins are retained in deep sleep mode such as PM2 and PM3. MG2475 uses 32MHz crystal oscillator for RF PLL and 8MHz clock generated from 32MHz in clock generator is used as the default clock of 8051 MCU subsystem. The clocks for MAC, a baseband modem are separately controlled by the internal clock controller block.

MG2475 supports a voice function as follows. The data generated by an external ADC is inputted to the voice block via I2S interface. After the data is received via I2S, it is compressed by the voice encoder and stored in the Voice TXFIFO. Then the data in the Voice TXFIFO is transferred to the MAC TXFIFO and transmitted via PHY. On the other hand, the received data in the MAC RXFIFO is transferred to voice RXFIFO through the internal direct path. Then the data in the Voice RXFIFO is decompressed in the internal voice decoder. After that, the decompressed data is transferred to the external DAC via I2S interface.

4 PIN DESCRIPTION

The pin-out diagram of MG2475 is shown in [Figure 2]. The description for that is summarized in [Table 1].

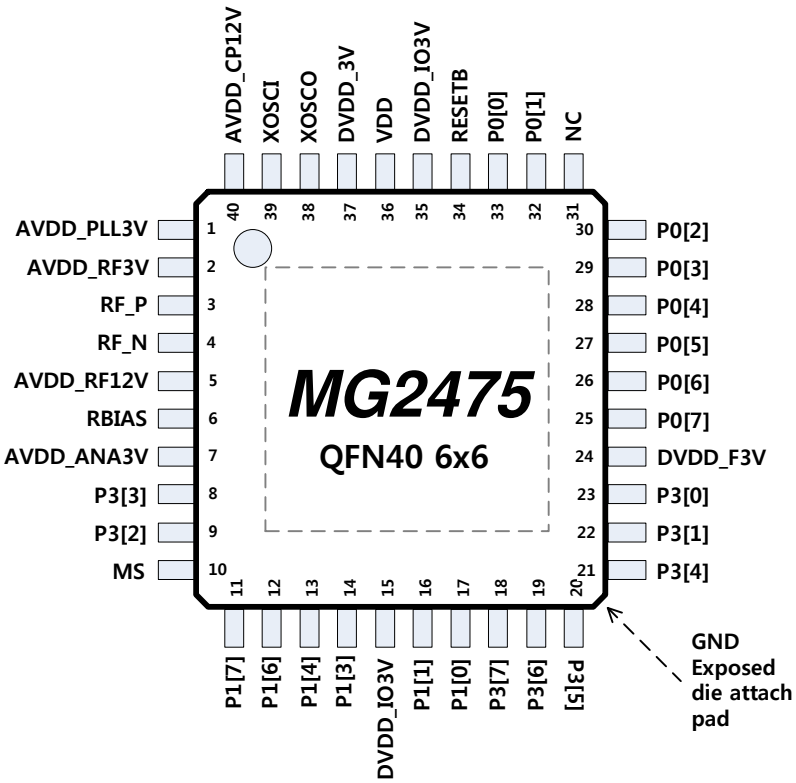


Figure 2. Pinout Top View of MG2475

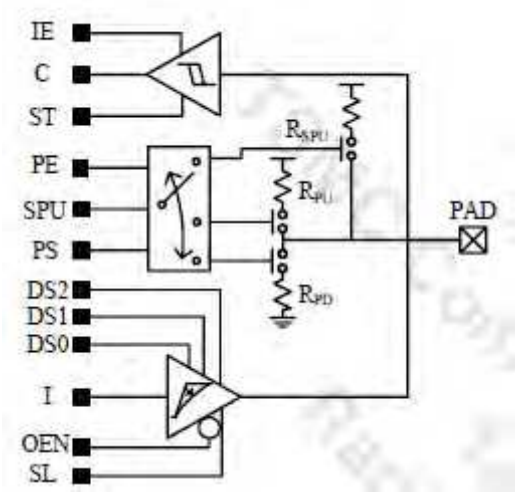
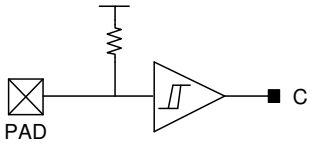
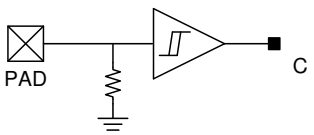
NOTE: The exposed ground pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.

Table 1. Pin Description

Radio, Synthesizer, and Oscillator			
Name	Pin	Type	Description
AVDD_PLL3V	1	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_RF3V	2	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_ANA3V	7	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_RF12V	5	Power	Regulated Output of AVDD_RF3V for PA bias
AVDD_CP12V	40	Power	Regulated Output of AVDD_PLL3V for decoupling
RF_P	3	RF I/O	Positive RF input signal to LNA in RX mode Positive RF output signal from PA in TX mode
RF_N	4	RF I/O	Negative RF input signal to LNA in RX mode Negative RF output signal from PA in TX mode
RBIAS	6	Analog I/O	External precision bias resistor(510kohm) to generate the reference current
Digital and Oscillator			
Name	Pin	Type	Description
DVDD_IO3V	15, 35	Power	2.0V to 3.6V Digital power supply connection(I/O supply)
DVDD_F3V	24	Power	2.0V to 3.6V Digital power supply connection(Flash supply)
DVDD_3V	37	Power	2.0V to 3.6V Digital power supply connection to digital regulator input
VDD	36	Power	1.2V Regulated Output of DVDD_3V for decoupling *Note: Do not use for supplying external circuits.
RESETB	34	Digital input	External Reset pin, active low
MS	10	Digital input	Mode slection 0 = Normal Mode, 1= ISP Mode
P0[0]	33	Digital I/O	Port P0.0/I2SRX_DI/PWM0
P0[1]	32	Digital I/O	Port P0.1/I2SRX_LRCLK/PWM1
P0[2]	30	Digital I/O	Port P0.2/I2SRX_BCLK/PWM2
P0[3]	29	Digital I/O	Port P0.3/I2SRX_MCLK/PWM3
P0[4]	28	Digital I/O	Port P0.4/I2STX_DO/PWM4/TRSWB

P0[5]	27	Digital I/O	Port P0.5/I2STX_LRCLK/PTC_GATE0/TRSW
P0[6]	26	Digital I/O	Port P0.6/I2STX_BCLK/PTC_GATE1
P0[7]	25	Digital I/O	Port P0.7/I2STX_MCLK/PTC_GATE2
P1[0]	17	Digital I/O	Port P1.0/RXD1
P1[1]	16	Digital I/O	Port P1.1/TXD1
P1[3]	14	Digital I/O	Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT
P1[4]	13	Digital I/O	Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4
P1[6]	12	Digital I/O	Port P1.6/I2C_SCL
P1[7]	11	Digital I/O	Port P1.7/I2C_SDA
P3[0]	23	Digital I/O	Port P3.0/RXD0/QUADXA
P3[1]	22	Digital I/O	Port P3.1/TXD0/QUADXB
P3[2]	9	Digital I/O	Port P3.2/nINT0
P3[3]	8	Digital I/O	Port P3.3/nINT1/ATEST0
P3[4]	21	Digital I/O	Port P3.4/RTS0/QUADYA/SPIDI/T0
P3[5]	20	Digital I/O	Port P3.5/CTS0/QUADYB/SPIDO/T1
P3[6]	19	Digital I/O	Port P3.6/RTS1/SPICLK
P3[7]	18	Digital I/O	Port P3.7/CTS1/SPICSN
XOSCI	39	Analog I/O	32MHz crystal oscillator pin
XOSCO	38	Analog I/O	32MHz crystal oscillator pin or external clock input
Ground			
Exposed bottom		Ground	Ground for RF, Analog, digital core, and I/O
NC			
NC	31	NC	-

Table 2. I/O Pins Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIOs(P0[7:0], P1[1:0], P1[7:6], P3[7:0])		
	Input with pull-up	I/O with the programmable pull-up/pull-down function
RESETB		
	input with pull-up	External Reset Input, Low Active
MS		
	input with pull-down	Mode Selection Pin (0: Normal, 1: ISP)

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter		Min.	Max	Unit	
Supply Voltage (AVDD_PLL3V, AVDD_RF3V,AVDD_ANA3V, DVDD_3V,DVDD_F3V, DVDD_IO3V)		-0.3	3.6	V	All supply pins must have the same voltage.
Core voltage(AVDD_RF12V, AVDD_ANA12V, VDD, XOSCI, XOSCO)		-0.3	1.32	V	
Storage Temperature		-40	150	°C	
ESD	HBM		2000	V	According to human-body model(JEDEC STD 22)
	MM		200	V	According to machine model(JEDEC STD 22)
	CDM		1000	V	According to charged-device model(JEDEC STD 22)

Exceeding one or more of these ratings may cause permanent damage to the device.

These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: These values were obtained under worst-case test conditions specially prepared for the MG2475 and these conditions are not sustained in normal operation environment.

Caution: ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

5.2 Recommended Operating Conditions

Parameter	MIN	MAX	UNIT
Operating ambient temperature range, TOP	-40	125	℃
Operating supply voltage, VDD (AVDD_PLL3V, AVDD_RF3V,AVDD_ANA3V, DVDD_3V,DVDD_F3V, DVDD_IO3V)	2	3.6	V
Voltage on any digital pin	-0.3	VDD	V

5.3 Digital IO DC Characteristics

All voltage values are based on AGND.

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	I/O supply voltage(DVDD_IO3V)	2.0	3.0	3.6	V
AGND	Chip ground		0		V
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{OH}	Output high voltage	2.4			V
V_{OL}	Output low voltage			0.4	V
R_{PU}	Pull-up Resistance		66		kΩ
R_{PD}	Pull-down Resistance		66		kΩ
R_{SPU}	Strong Pull-up Resistance (@ DVDD_IO3V=3.3V)	1.42	1.62	1.92	kΩ

5.4 Current Consumption and Timing Characteristics

TOP = 25˚C, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
MCU active. No radio and peripherals (UART1&RNG) active. @ MCU clock = 8MHz @ MCU clock = 16MHz		 2.13 3.28		mA
RX mode. MCU active @ MCU clock = 8MHz		16.3		mA
TX mode. MCU active @ MCU clock = 8MHz @ +9 dBm Output Power @ +8 dBm Output Power @ +7 dBm Output Power @ +6 dBm Output Power @ +5 dBm Output Power @ +4 dBm Output Power @ +3 dBm Output Power @ +2 dBm Output Power @ +1 dBm Output Power @ 0dBm Output Power		 36.5 30.8 27.0 24.1 22.4 21.3 19.9 19.7 18.7 16.9		mA
Power mode1. Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		7.6		µA
Power mode2. Digital regulator off, retention mode 1(7KB SRAM retained), GPIO retention, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		4.6		µA
Power mode3. Digital regulator off, retention mode 3(all digital off), GPIO retention, 16MHz RCOSC, 32MHz crystal oscillator, 32kHz RCOSC, BOD and sleep timer off.		1.7		µA
Wake-up and timing				
Power mode1 → MCU Active Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of 16MHz RCOSC		200		µs
Power mode2 → MCU Active Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of regulator and 16MHz RCOSC		380		µs
MCU Active → TX or RX (Power mode1) Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator.		1.16		ms
MCU Active → TX or RX (Power mode2) Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator.		1.054		ms
TX/RX and RX/TX turnaround			192	µs

5.5 RF Receive Section

Measured on 2-layer reference design with TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[1](center frequency)	2405		2480	MHz
Maximum input level (PER≤1%) @ 1000kbps @ 250kbps		 10 10		dBm
Spurious radiation @ 30MHz – 1000MHz @ 1GHz – 12.75GHz		 -70 -70		dBm
Received RF bandwidth		2		MHz
Channel spacing[2]		5		MHz
Receiver sensitivity (PER≤1%, PSDU length of 20-byte) @ 1000kbps @ 250kbps		 -95 -98.5		dBm
Adjacent channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps) +5MHz -5MHz		 36.2 34.7		dB
Adjacent channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps) +5MHz -5MHz		 31.2 31.4		dB
Adjacent channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps, filtered) +5MHz -5MHz		 48.4 48.8		
Adjacent channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps, filtered) +5MHz -5MHz		 46.9 46.2		dB
Alternate channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps) +10MHz -10MHz		 47.7 48.1		dB
Alternate channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps)				

[1] Extended range: 2394~2507MHz

[2] Specified in IEEE Standard 802.15.4™

+10MHz -10MHz		43.7 43.6		
Alternate channel rejection (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps, filtered) +10MHz -10MHz		 56.2 57.0		
Alternate channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps, filtered) +10MHz -10MHz		 54.8 56.2		dB
Others channel rejection (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps) ≥+15MHz ≥-15MHz		 58.4 58.5		dB
Others channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps) ≥+15MHz ≥-15MHz		 56 55.3		dB
Others channel rejection (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps, filtered) ≥+15MHz ≥-15MHz		 63.3 64.1		
Others channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps, filtered) ≥+15MHz ≥-15MHz		 61.6 62.5		dB
Co-channel rejection (-82 dBm. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-4		dB
Co-channel rejection @ 1 Mbps (-82 dBm. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-8		dB
Wifi Rejection @ 250 kbps (-82 dBm, 802.11n (BW40MHz), @ ±27 MHz offset)		45.5		
Wifi Rejection @ 1 Mbps (-82 dBm, 802.11n (BW40MHz), @ ±27 MHz offset)		44		dB
Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -28 -30 -26.7 -28 -26.3 -23.2		dBm

Blocking/desensitization @ 1 Mbps (wanted signal is with power 3 dB larger than sensitivity, -92 dBm) -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -25.8 -26.9 -25.6 -27.0 -25.8 -23.9		dBm
RSSI dynamic range		95		dB
RSSI accuracy		±3		dB

5.6 RF Transmit Section

Measured on 2-layer reference design with TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[3](center frequency)	2405		2480	MHz
TX output power (using the recommended matching circuit)		9		dBm
Transmit chip rate		2		Mcps
Error vector magnitude (EVM)		6		%
Harmonics 2nd harmonic 3rd harmonic		 -45 -50		dBm
Spurious emission (complies with EN 300-440, FCC and ARIB STD-T66) 30Hz ~ 1GHz 1GHz ~ 12.75GHz 1.8 ~ 1.9GHz 5.15 ~ 5.3GHz		 -60 -70 -70 -70		dBm

[3] Extended range: 2394~2507MHz

5.7 Frequency Synthesizer

TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset @ ±10MHz offset @ ±50MHz offset		 -82.3 -108.8 -116.6 -120 -125.2 -134.9 -151.7		dBc/Hz
Lock time			80	μs

5.8 32MHz Crystal Oscillator

T_{OP}=25℃, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Crystal frequency		32		MHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		30[4]		Ω
Crystal shunt capacitance(CO)		5[4]		pF
Crystal load capacitance(CL)		13[4]		pF
Start-up time			0.8	ms

5.9 32kHz RC Oscillator

T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Calibrated frequency		32.787		kHz
frequency accuracy after calibration	-0.3		0.3	%
Initial calibration time		5.6		ms
Start-up time			100	μs

[4] Equivalent series resistance, Crystal shunt capacitance (CO) and Load capacitance (CL) can vary with the selection of Crystal Oscillator.

5.10 Flash Memory

5.10.1 Flash memory characteristics

Characteristic	Symbol	Conditions	MIN	TYP	MAX	UNIT
Endurance	Nendu	20 ms erase and 20 us program time	10,000			cycles
Data retention	Tret	85 °C	10			years

5.10.2 Flash memory and page size

Name	Size	Unit
Flash main memory block	65,536	bytes
Flash information block	4,096	bytes
Flash page size	2048	bytes