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MGM111 Mighty Gecko Mesh Networking Module Data Sheet

The Silicon Labs Mighty Gecko Module (MGM111) is a fully-integrated, pre-certified module, enabling rapid development of wireless mesh networking solutions.

Based on the Silicon Labs EFR32™ Mighty Gecko SoC, the MGM111 combines an energy-efficient, multi-protocol wireless SoC with a proven RF/antenna design and industry-leading wireless software stacks. This integration accelerates time-to-market and saves months of engineering effort and development costs.

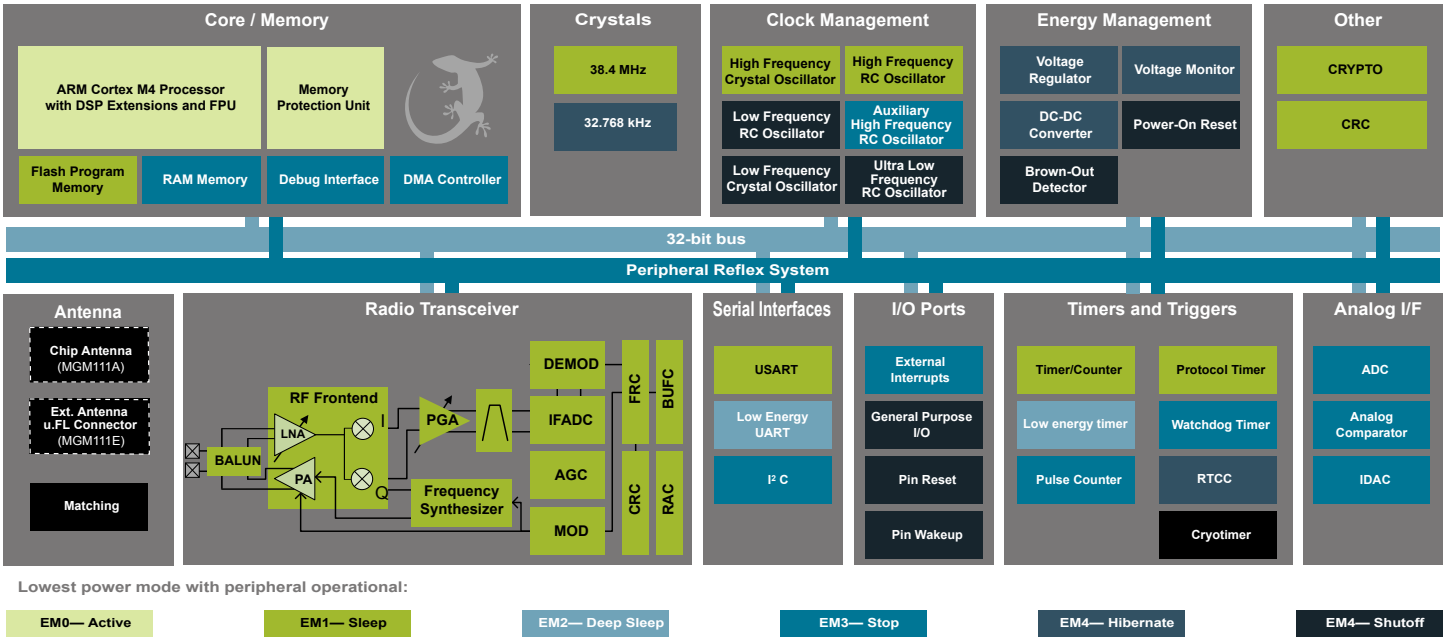
In addition, common software and development tools enable seamless migration from a module to discrete SoC-based design when the time is right.

MGM111 can be used in a wide variety of applications:

- Connected Home
- Building Automation
- Lighting
- Security and Monitoring
- Smart Grid / Metering
- Industrial Automation
- Others

KEY FEATURES

- Industry-leading mesh networking (ZigBee/Thread) software and development tools
- Antenna: internal chip and U.FL variants
- TX power: up to +10 dBm
- RX sensitivity: down to -99 dBm
- 32-bit ARM® Cortex®-M4 at 40 MHz
- Flash memory: 256 kB
- RAM: 32 kB
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated DC-DC Converter



1. Feature List

MCU Features

- ARM Cortex®-M4 + Floating Point Unit
- Up to 40 MHz Clock Speed
- Low Active Mode Current: 63 µA/MHz
- 256 kB flash, 32 kB SRAM
- Advanced hardware cryptographic engine with support for AES-128/-256, ECC, SHA-1, SHA-256, and a Random Number Generator
- 8 Channel DMA Controller

Digital Peripherals

- 2 x USART (UART, SPI, IrDA, I^2S)
- Low Energy UART (LEUART™)
- I^2C peripheral interface (address recognition down to EM3)
- Timers: RTCC, Low Energy Timer, Pulse Counter
- 12-channel Peripheral Reflex System (PRS)
- Up to 25 GPIO with interrupts

Analog Peripherals

- ADC (12-bit, 1 Msps, 326 µA)
- Current-mode Digital to Analog Converter (IDAC)
- 2 x Analog Comparator (ACMP)

Energy Efficient Low Power Modes

- Energy Mode 2 (Deep Sleep) Current: 2.5 µA

  (Full RAM retention and RTCC running from LXFO)
- Ultra-fast wake up: 3 µS down to EM3
- Wide Supply Voltage range of 1.85 to 3.8 V

Environmental & Regulatory

- Operating Temperature: -40 to +85°C
- FCC, IC, CE, Aus/NZ, Korea certifications (pending)

Dimensions

- W x L x H: 12.9 x 15.0 x 2.2 mm

Radio Features

- 2.4 GHz with integrated balun
- Support for wireless mesh networking (ZigBee/Thread)
- Integrated PA (up to +10 dBm TX power)
- Packet Trace Interface (PTI) for non-intrusive packet trace with Simplicity Studio development tools
- Antenna interface: integrated high-performance chip antenna or u.FL variant for external antenna

ZigBee and Thread Features

- IEEE 802.15.4
- Data Rate / Modulation: 250 kbps DSSS-OQPSK
- +10 dBm Programmable TX Power
- -99 dBm RX Sensitivity
- 9.8 mA RX current
- 8.2 mA TX current (at +0 dBm)
- Support for SoC and Network Co-Processor (NCP) architectures with SPI/UART host support
- Serial and Over-The-Air (OTA) bootloaders

2. Ordering Information

Ordering Code	Description	Max TX Power	Antenna	Packaging	Production Status
MGM111A256V1	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Initial Production / Engineering Samples (non-certified)
MGM111A256V1R	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Reel (1000 pcs)	Initial Production / Engineering Samples (non-certified)
MGM111E256V1	Mighty Gecko Module	+10 dBm	External (U.FL)	Cut Reel (100 pcs)	Initial Production / Engineering Samples (non-certified)[1]
MGM111E256V1R	Mighty Gecko Module	+10 dBm	External (U.FL)	Reel (1000 pcs)	Initial Production / Engineering Samples (non-certified)[1]
MGM111A256V2	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Full Production (certified)[1]
MGM111A256V2R	Mighty Gecko Module	+10 dBm	Integrated chip antenna	Reel (1000 pcs)	Full Production (certified)[1]
MGM111E256V2	Mighty Gecko Module	+10 dBm	External (U.FL)	Cut Reel (100 pcs)	Full Production (certified)[1]
MGM111E256V2R	Mighty Gecko Module	+10 dBm	External (U.FL)	Reel (1000 pcs)	Full Production (certified)[1]
SLWRB4300B	MGM111A Radio Board Add-On for Mesh Networking Kit (SLWSTK6000A)	+10 dBm	Integrated chip antenna	Single unit	Initial Production / Engineering Samples (non-certified)

Note:

1. Contact sales for availability and certification timelines.
2. IAR license required for ZigBee and Thread software development.

3. System Overview

3.1 Introduction

This section provides a brief overview of the MGM111 module architecture including both MCU and RF sub-systems. A detailed functional description of the EFR32MG1 SoC used inside the module is available in the *EFR32MG1 Mighty Gecko Datasheet* and *EFR32xG1 Wireless Gecko Reference Manual* and a block diagram of the EFR32MG1 SoC is shown in the figure below.

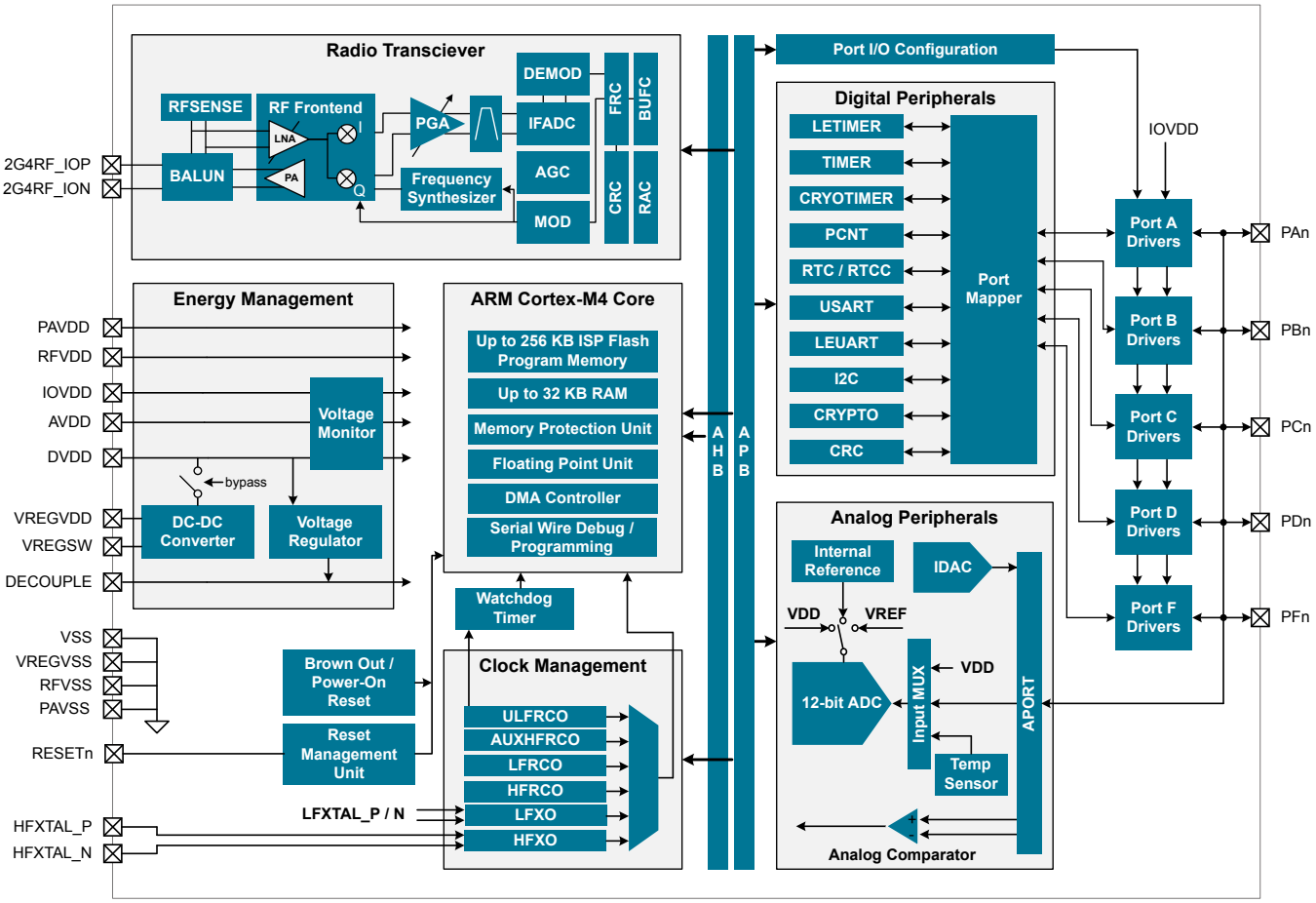


Figure 3.1. Detailed EFR32MG1 Block Diagram

3.2 Radio

The MGM111 features a flexible, multi-protocol radio that supports wireless mesh networking (ZigBee® / Thread) protocols.

3.2.1 Antenna Interface

The MGM111 module family includes options for either a high-performance, integrated chip-antenna (MGM111A) or external antenna (MGM111E) via a U.FL connector. The table below includes performance specifications for the integrated chip antenna.

Table 3.1. Antenna Efficiency and Peak Gain (MGM111A)

Parameter	With optimal layout	Note
Efficiency	-2 dB to -3 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Chapter 6. Layout Guidelines for PCB layout and antenna integration guidelines for optimal performance.
Peak gain	1.0 dBi	

3.2.2 Packet and State Trace

The MGM111 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The MGM111 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

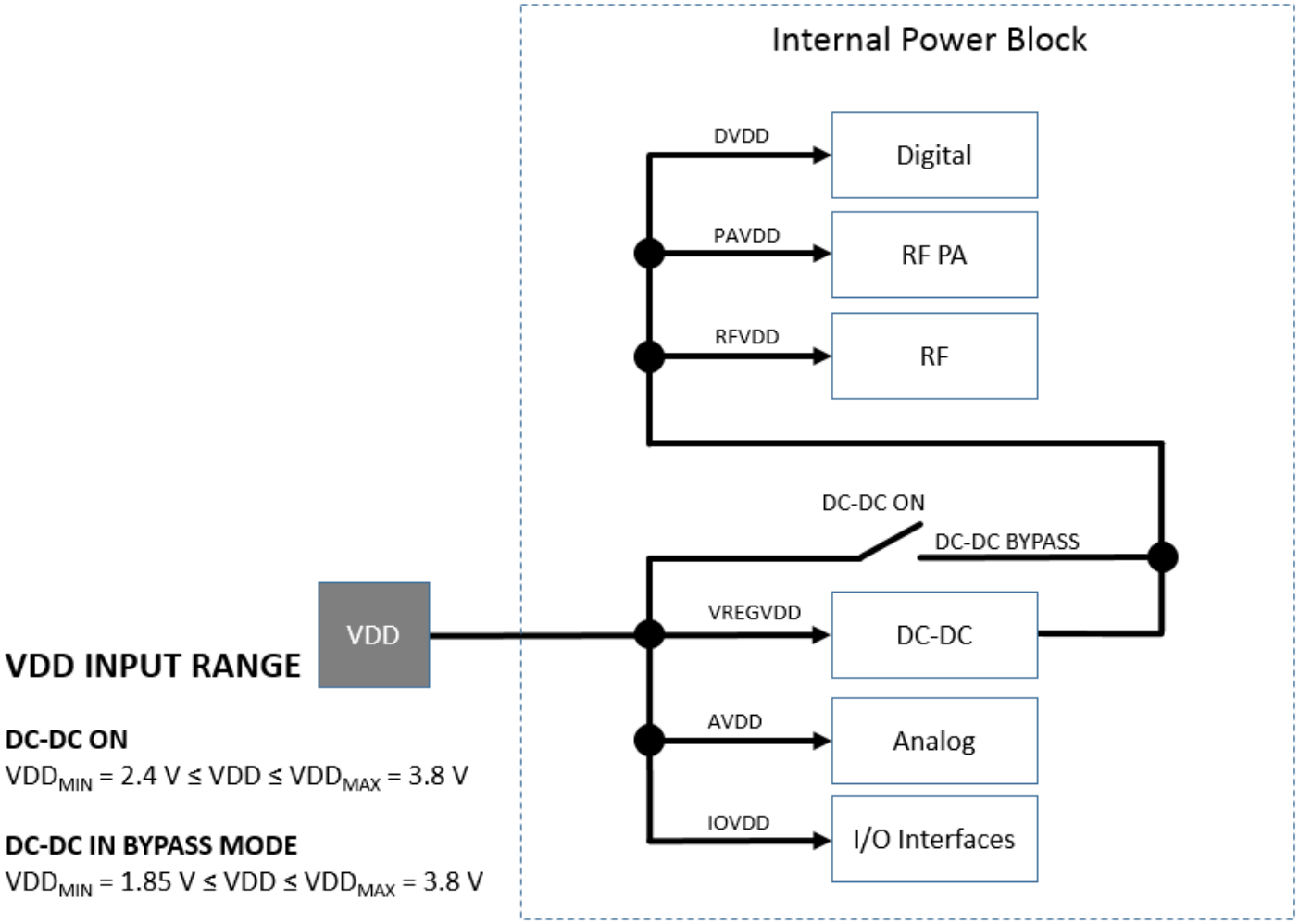


Figure 3.2. MGM111 Power Block

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

MGM111 has up to 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM111. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators

The MGM111 fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05 µA and 64 µA with several ranges with various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM111. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The MGM111 memory map is shown in the figures below.

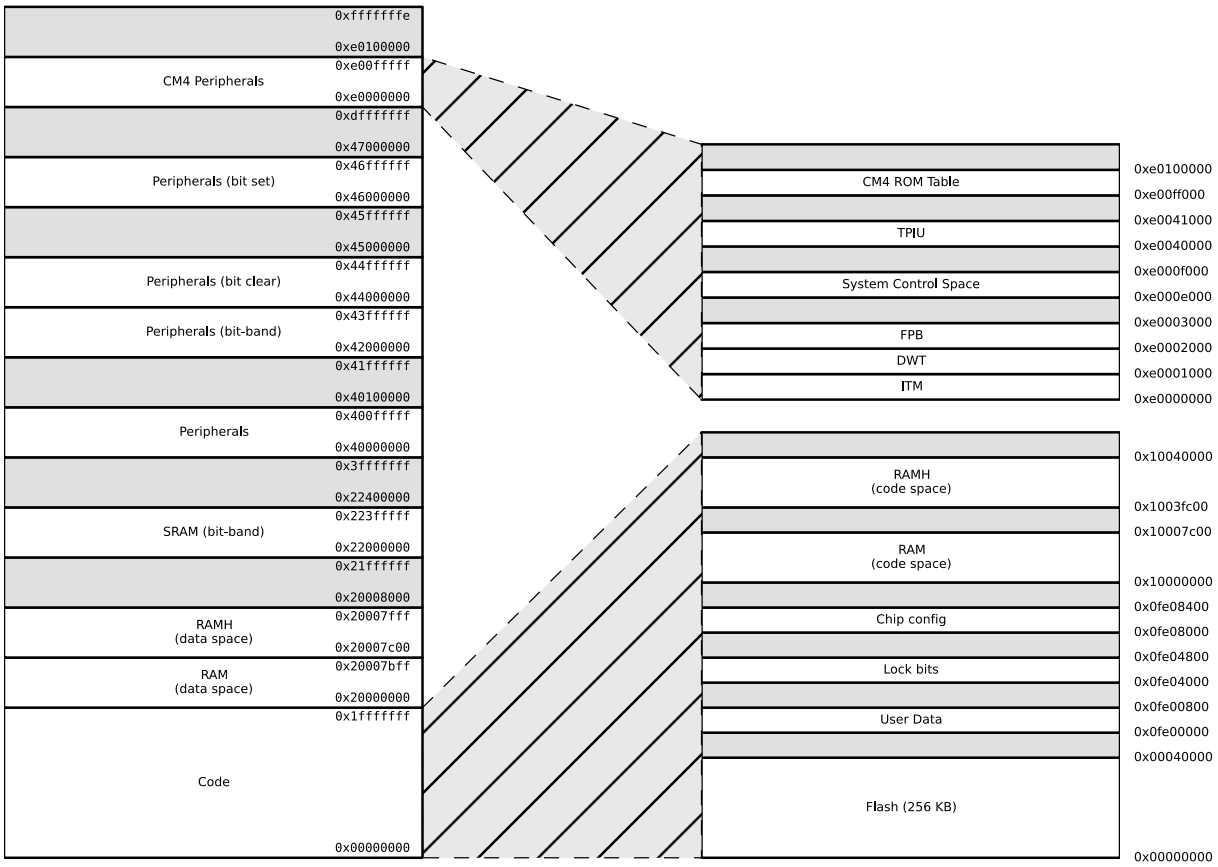


Figure 3.3. MGM111 Memory Map — Core Peripherals and Code Space

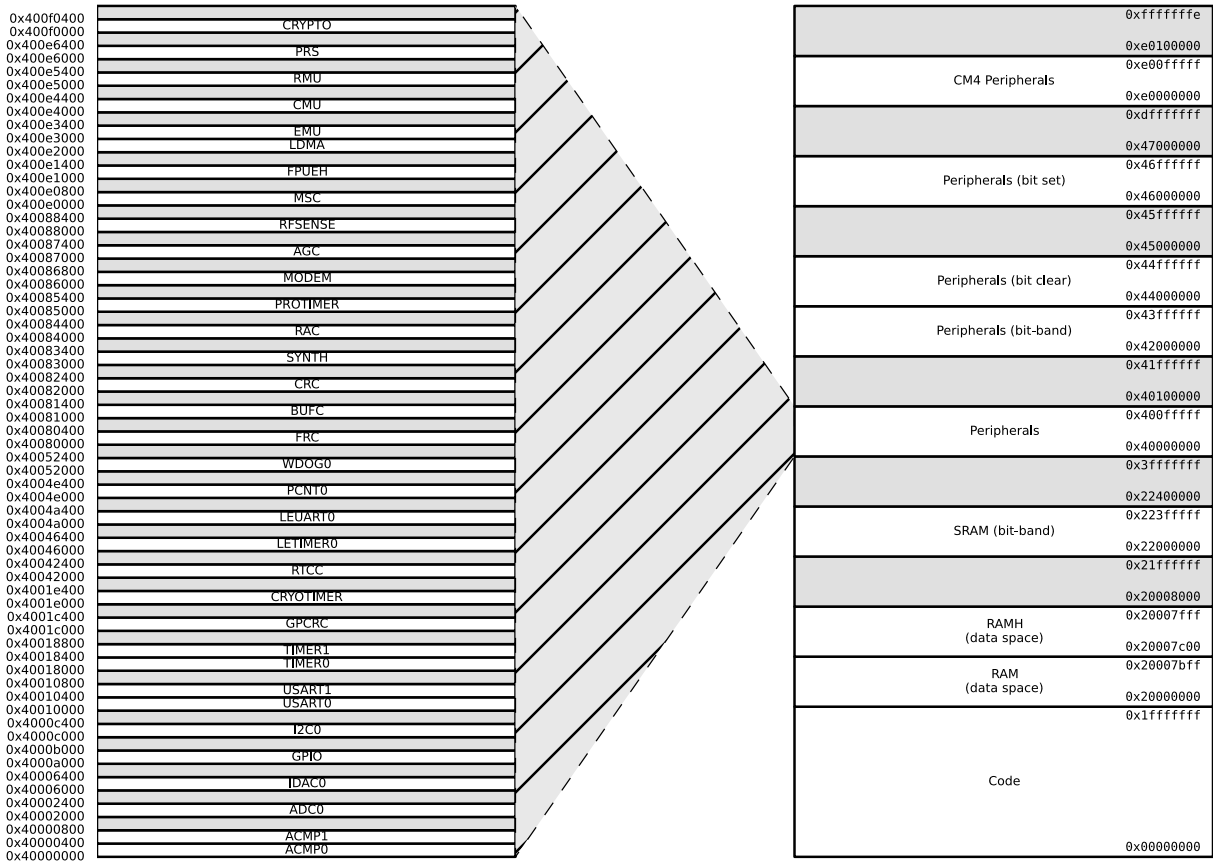


Figure 3.4. MGM111 Memory Map — Peripherals

3.13 Configuration Summary

The features of the MGM111 are a subset of the feature set described in the *EFR32xG1 Wireless Gecko Reference Manual*. The Pin Definitions section describes device specific implementation of the features.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation and operating temperature.

Refer to Table 4.2 General Operating Conditions on page 13 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+85	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and VDD+2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	VDD+0.3	V
Input RF level	$P_{RFMAX2G4}$		—	—	10	dBm
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = VDD.

4.1.2 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	Ambient Temperature	-40	25	85	°C
VDD supply voltage[1]	V_{VDD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
VDD Current	I_{VDD}	DCDC in bypass	—	—	200	mA
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [2]	—	—	26	MHz
		1 wait-states (MODE = WS1) [2]	—	38.4	40	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{VDD\_min}+I_{LOAD} * R_{BYP\_max}$
2. in MSC_READCTRL register

4.1.3 DC-DC Converter

Test conditions: V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=7 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.85	—	V_{VDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	V_{VDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	V_{VDD_MAX}	V
Output voltage programmable range [1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive [3]	—	—	200	mA
		Low noise (LN) mode, Medium Drive [3]	—	—	100	mA
		Low noise (LN) mode, Light Drive [3]	—	—	50	mA
		Low power (LP) mode, LPCMPBIAS [2] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIAS [2] = 3	—	—	10	mA

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VDD}
2. In EMU_DCDCMISCCTRL register
3. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.4. Current Consumption 3.3V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[2]	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	71	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	µA/MHz
Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal, CPU running while loop from flash[2]	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	75	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode[1].	I_{EM1}	38.4 MHz crystal[2]	—	49	—	µA/MHz
		38 MHz HFRCO	—	32	—	µA/MHz
		26 MHz HFRCO	—	38	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode[3].		38.4 MHz crystal[2]	—	61	—	µA/MHz
		38 MHz HFRCO	—	45	—	µA/MHz
		26 MHz HFRCO	—	58	—	µA/MHz
Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode[4].	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	2.5	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.2	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.1	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	0.86	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.58	—	µA
		128 byte RAM retention, no RTCC	—	0.58	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

Note:
1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DCDC voltage.
2. CMU_HFXOCTRL_LOWPOWER=0
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DCDC voltage.
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DCDC voltage.

4.1.4.2 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	9.8	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	F = 2.4 GHz, CW, 0 dBm, Radio clock prescaled by 3	—	8.2	—	mA
		F = 2.4 GHz, CW, 10.5 dBm	—	32.7	—	mA

4.1.5 Wake up times

Table 4.6. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	t_{EM2_WU}	Code execution from flash	—	10.7	—	µs
		Code execution from RAM	—	3	—	µs
Wakeup time from EM1 Sleep	t_{EM1_WU}	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	—	10.7	—	µs
		Executing from RAM	—	3	—	µs
Wake up from EM4H Hibernate[1]	t_{EM4H_WU}	Executing from flash	—	60	—	µs
Wake up from EM4S Shutoff[1]	t_{EM4S_WU}		—	290	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

4.1.6 Brown Out Detector

For the table below, see Figure 3.2 MGM111 Power Block on page 5 to see the internal connection and relation between DVDD and AVDD. The module itself has only one external power supply input (VDD).

Table 4.7. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	1.62	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	21	—	mV
AVDD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.7 Frequency Synthesizer Characteristics

Table 4.8. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution	F_{RES_2400}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation	ΔF_{MAX_2400}		—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C, VDD = 3.3 V. RF center frequency 2.45 GHz. Measurements are conducted from the antenna feed point.

Table 4.9. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power	$POUT_{MAX}$		—	10	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm < Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.85 V < V_{VDD} < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, DCDC enabled	—	1.5	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_{OP} = 25 °C,VDD = 3.3 V. RF center frequency 2.440 GHz. Measurements are conducted from the antenna feed point.

Table 4.10. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm

4.1.8.3 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T=25 °C,VDD = 3.3 V. RF center frequency 2.445 GHz. Meaurements are conducted from the antenna feed point.

Table 4.11. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[1]. Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-99	—	dBm
		Signal is reference signal. Packet length is 20 octets. DC-DC converter in bypass mode.	—	-99	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 10 dB above sensitivity limit	—	-2.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{+1}	Interferer is reference signal at +1 channel-spacing.	—	33.75	—	dB
		Interferer is filtered reference signal[3] at +1 channel-spacing.	—	52.2	—	dB
		Interferer is CW at +1 channel-spacing.[4]	—	58.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{-1}	Interferer is reference signal at -1 channel-spacing.	—	35	—	dB
		Interferer is filtered reference signal[3] at -1 channel-spacing.	—	54.7	—	dB
		Interferer is CW at -1 channel-spacing.	—	60.1	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ±2 channel-spacing	—	45.9	—	dB
		Interferer is filtered reference signal[3] at ±2 channel-spacing	—	56.8	—	dB
		Interferer is CW at ±2 channel-spacing	—	65.5	—	dB
Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]	IR	Interferer is CW in image band[4]	—	49.3	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]. Interferer is reference signal.	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	57.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	57.9	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz	$BLOCK_{80211G}$	Desired is reference signal at 6dB above reference sensitivity level[2]	—	51.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		5	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-98	dBm
RSSI resolution	$RSSI_{RES}$	over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	$RSSI_{LIN}$		—	±1	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s
2. Reference sensitivity level is -85 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stopband rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ±5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.1.9 Oscillators

4.1.9.1 LFXO

Table 4.12. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{LFXO}		—	32.768	—	kHz
Crystal Frequency Tolerance			-100		+100	ppm

4.1.9.2 HFXO

Table 4.13. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		—	38.4	—	MHz
Crystal Frequency Tolerance			-40		+40	ppm

4.1.9.3 LFRCO

Table 4.14. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	30.474	32.768	34.243	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	30.474	32.768	33.915	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. Block is supplied by VDD if ANASW = 0, or DCDC if ANASW=1 in EMU_PWRCTRL register

4.1.9.4 HFRCO and AUXHFRCO

Table 4.15. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	f_{HFRCO}	Any frequency band, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	f_{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f_{HFRCO} < 19 MHz	—	1	—	µs
		f_{HFRCO} ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	204	228	µA
		f_{HFRCO} = 32 MHz	—	171	190	µA
		f_{HFRCO} = 26 MHz	—	147	164	µA
		f_{HFRCO} = 19 MHz	—	126	138	µA
		f_{HFRCO} = 16 MHz	—	110	120	µA
		f_{HFRCO} = 13 MHz	—	100	110	µA
		f_{HFRCO} = 7 MHz	—	81	91	µA
		f_{HFRCO} = 4 MHz	—	33	35	µA
		f_{HFRCO} = 2 MHz	—	31	35	µA
		f_{HFRCO} = 1 MHz	—	30	35	µA
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.9.5 ULFRCO

Table 4.16. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.10 Flash Memory Characteristics

Table 4.17. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	26	40	µs
Page erase time	t_{PERASE}		20	27	40	ms
Mass erase time	t_{MERASE}		20	27	40	ms
Device erase time[2]	t_{DERASE}		—	60	74	ms
Page erase current[3]	I_{ERASE}		—	—	3	mA
Mass or Device erase current[3]			—	—	5	mA
Write current[3]	I_{WRITE}		—	—	3	mA

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
3. Measured at 25°C

4.1.11 GPIO

Table 4.18. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	VDD*0.3	V
Input high voltage	V_{IOIH}		VDD*0.7	—	—	V
Output high voltage relative to VDD	V_{IOOH}	Sourcing 3 mA, VDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	VDD*0.8	—	—	V
		Sourcing 1.2 mA, VDD ≥ 1.62 V DRIVESTRENGTH[1] = WEAK	VDD*0.6	—	—	V
		Sourcing 20 mA, VDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	VDD*0.8	—	—	V
		Sourcing 8 mA, VDD ≥ 1.62 V DRIVESTRENGTH[1] = STRONG	VDD*0.6	—	—	V
Output low voltage relative to VDD	V_{IOOL}	Sinking 3 mA, VDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	VDD*0.2	V
		Sinking 1.2 mA, VDD ≥ 1.62 V DRIVESTRENGTH[1] = WEAK	—	—	VDD*0.4	V
		Sinking 20 mA, VDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	VDD*0.2	V
		Sinking 8 mA, VDD ≥ 1.62 V DRIVESTRENGTH[1] = STRONG	—	—	VDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ VDD	—	0.1	30	nA
		LFXO Pins, GPIO ≤ VDD	—	0.1	50	nA
Input leakage current on 5VTOL pads above VDD	$I_{5VTOLLEAK}$	VDD < GPIO ≤ VDD + 2 V	—	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		30	43	65	kΩ
I/O pin pull-down resistor	R_{PD}		30	43	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		20	25	35	ns
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns