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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SILICON LABS

MGM12P Mighty Gecko Multi-Protocol Wireless Mesh Module Data Sheet

The Silicon Labs Mighty Gecko Module (MGM12P) is a fully-integrated, certified module, enabling rapid development of wireless mesh networking solutions.

Based on the Silicon Labs EFR32MG12 Mighty Gecko SoC, the MGM12P combines an energy- efficient, multi-protocol wireless SoC with a proven RF/antenna design and industry leading wireless software stacks. This integration accelerates time-to-market and saves months of engineering effort and development costs.

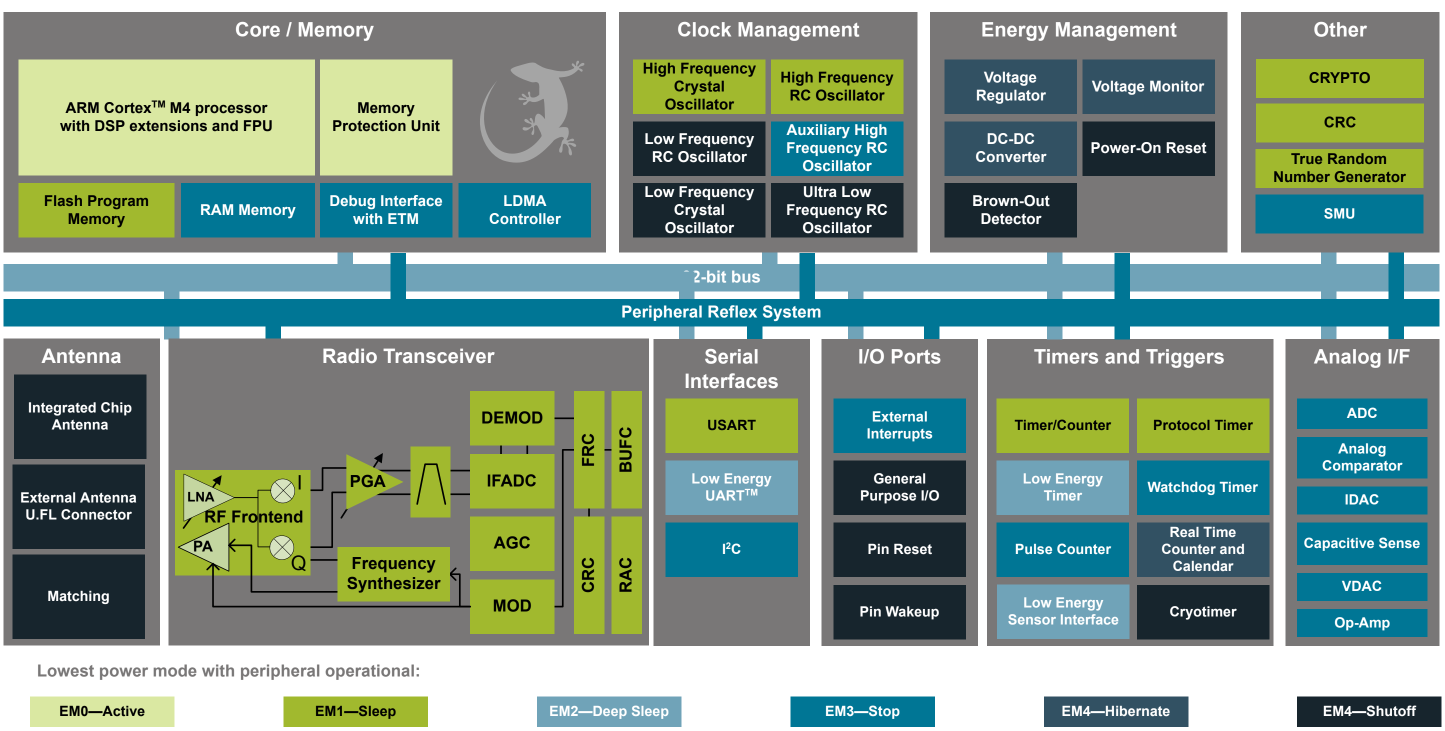
In addition, common software and development tools enable seamless migration from a module to discrete SoC-based design when the time is right.

MGM12P can be used in a wide variety of applications:

- IoT Multi-Protocol Devices
- Connected Home
- Lighting
- Health and Wellness
- Metering
- Building Automation and Security

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- 1 MB of flash and 256 kB of RAM
- ZigBee, Thread, BLE, and multi-protocol support
- Pin-compatible with MGM111 module
- 12-channel Peripheral Reflex System, Low-Energy Sensor Interface & Multi-channel Capacitive Sense Interface
- Integrated PA with up to +17 dBm transmit power
- Robust peripheral set and up to 25 GPIO



1. Feature List

The MGM12P highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - 1024 kB flash program memory
  - 256 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to +17 dBm
- **Low Energy Consumption**
  - 10.3 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 10.8 mA RX current at 2.4 GHz (250 kbps O-QPSK DSSS)
  - 10 mA TX current @ 0 dBm output power at 2.4 GHz
  - 70 μA/MHz in Active Mode (EM0)
  - 2.1 μA EM2 DeepSleep current (256 kB RAM retention and RTCC running from LFXO)
- **High Receiver Performance**
  - -101 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -105 dBm sensitivity @ 250 kbps O-QPSK DSSS (modules with LNA)
  - -95 dBm sensitivity @ 1Mbps 2GFSK
  - -101.6 dBm sensitivity @ 1Mbps 2GFSK (modules with LNA)
- **Supported Modulation Format**
  - Shaped OQPSK
  - 2-FSK / 4-FSK with fully configurable shaping
- **Supported Protocols:**
  - Bluetooth® Low Energy (Bluetooth 5)
  - zigbee
  - Thread
- **Support for Internet Security**
  - General Purpose CRC
  - True Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2×Analog Comparator (ACMP)
  - 2×Digital to Analog Converter (VDAC)
  - 3×Operational Amplifier (Opamp)
  - Digital to Analog Current Converter (IDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Multi-channel Capacitive Sense Interface (CSEN)
  - Up to 25 pins connected to analog channels (APORT) shared between analog peripherals
  - Up to 25 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 2×32-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 3×16-bit Pulse Counter with asynchronous operation
  - 2×Watchdog Timer with dedicated RC oscillator
  - 4×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - 2×I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - -40 °C to 85 °C
- **WxLxH:** 12.9 x 17.8 x 2.3 mm

2. Ordering Information

Ordering Code	Description	Max TX Power	Sensitivity (O-QPSK)	Antenna	Packaging	Production Status
MGM12P32F1024GA-V2	Multi-protocol Module	+17 dBm	-105 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Full Production (certified)
MGM12P32F1024GA-V2R	Multi-protocol Module	+17 dBm	-105 dBm	Integrated chip antenna	Reel (1000 pcs)	Full Production (certified)
MGM12P32F1024GE-V2	Multi-protocol Module	+17 dBm	-105 dBm	External (U.FL)	Cut Reel (100 pcs)	Full Production (certified)
MGM12P32F1024GE-V2R	Multi-protocol Module	+17 dBm	-105 dBm	External (U.FL)	Reel (1000 pcs)	Full Production (certified)
MGM12P22F1024GA-V2	Multi-protocol Module	+10 dBm	-105 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Full Production (certified)
MGM12P22F1024GA-V2R	Multi-protocol Module	+10 dBm	-105 dBm	Integrated chip antenna	Reel (1000 pcs)	Full Production (certified)
MGM12P22F1024GE-V2	Multi-protocol Module	+10 dBm	-105 dBm	External (U.FL)	Cut Reel (100 pcs)	Full Production (certified)
MGM12P22F1024GE-V2R	Multi-protocol Module	+10 dBm	-105 dBm	External (U.FL)	Reel (1000 pcs)	Full Production (certified)
MGM12P02F1024GA-V2	Multi-protocol Module	+10 dBm	-101 dBm	Integrated chip antenna	Cut Reel (100 pcs)	Full Production (certified)
MGM12P02F1024GA-V2R	Multi-protocol Module	+10 dBm	-101 dBm	Integrated chip antenna	Reel (1000 pcs)	Full Production (certified)
MGM12P02F1024GE-V2	Multi-protocol Module	+10 dBm	-101 dBm	External (U.FL)	Cut Reel (100 pcs)	Full Production (certified)
MGM12P02F1024GE-V2R	Multi-protocol Module	+10 dBm	-101 dBm	External (U.FL)	Reel (1000 pcs)	Full Production (certified)
SLWRB4304A	MGM12P Radio Board[3]	+17 dBm	-105 dBm	Integrated chip antenna	Single Unit	Development Board

Note:

1. IAR license required for zigbee and Thread software development.
2. *Bluetooth*® Low Energy regulatory certification pending. Contact sales for availability and certification time lines.
3. Requires Mesh Networking kit SLWSTK6000A or SLWSTK6000B

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3. System Overview

3.1 Introduction

This section provides a brief overview of the MGM12P module architecture including both MCU and RF sub-systems. A detailed functional description of the EFR32MG12 SoC used inside the module is available in the *EFR32MG12 Mighty Gecko Datasheet* and *EFR32xG12 Wireless Gecko Reference Manual*. A block diagram of the EFR32MG12 SoC is shown in the figure below.

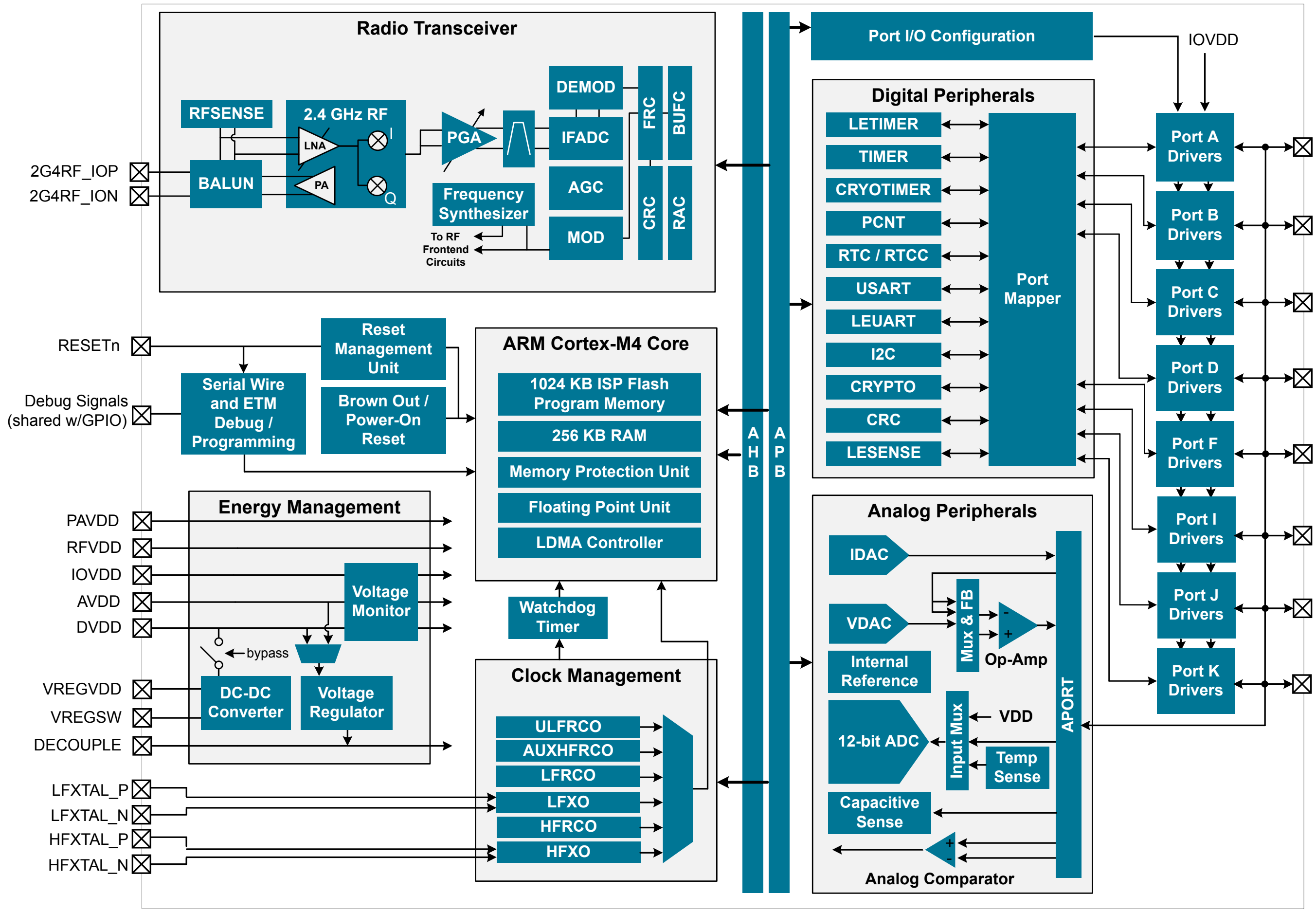

Figure 3.1. Detailed EFR32MG12 Block Diagram

3.2 Radio

The MGM12P modules feature a highly configurable radio transceiver that supports a wide range of wireless protocols including zigbee, Thread, and Bluetooth Low Energy.

3.2.1 Antenna Interface

The MGM12P module family includes options for either a high-performance, integrated chip-antenna (MGM12P-GA) or external antenna (MGM12P-GE) via a U.FL connector. The table below includes performance specifications for the integrated chip antenna.

Table 3.1. Antenna Efficiency and Peak Gain (MGM12P)

Parameter	With optimal layout	Note
Efficiency	-4 dB to -5 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Chapter for PCB layout and antenna integration guidelines for optimal performance.
Peak gain	1.0 dBi	

3.2.2 Packet and State Trace

The MGM12P Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The MGM12P has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

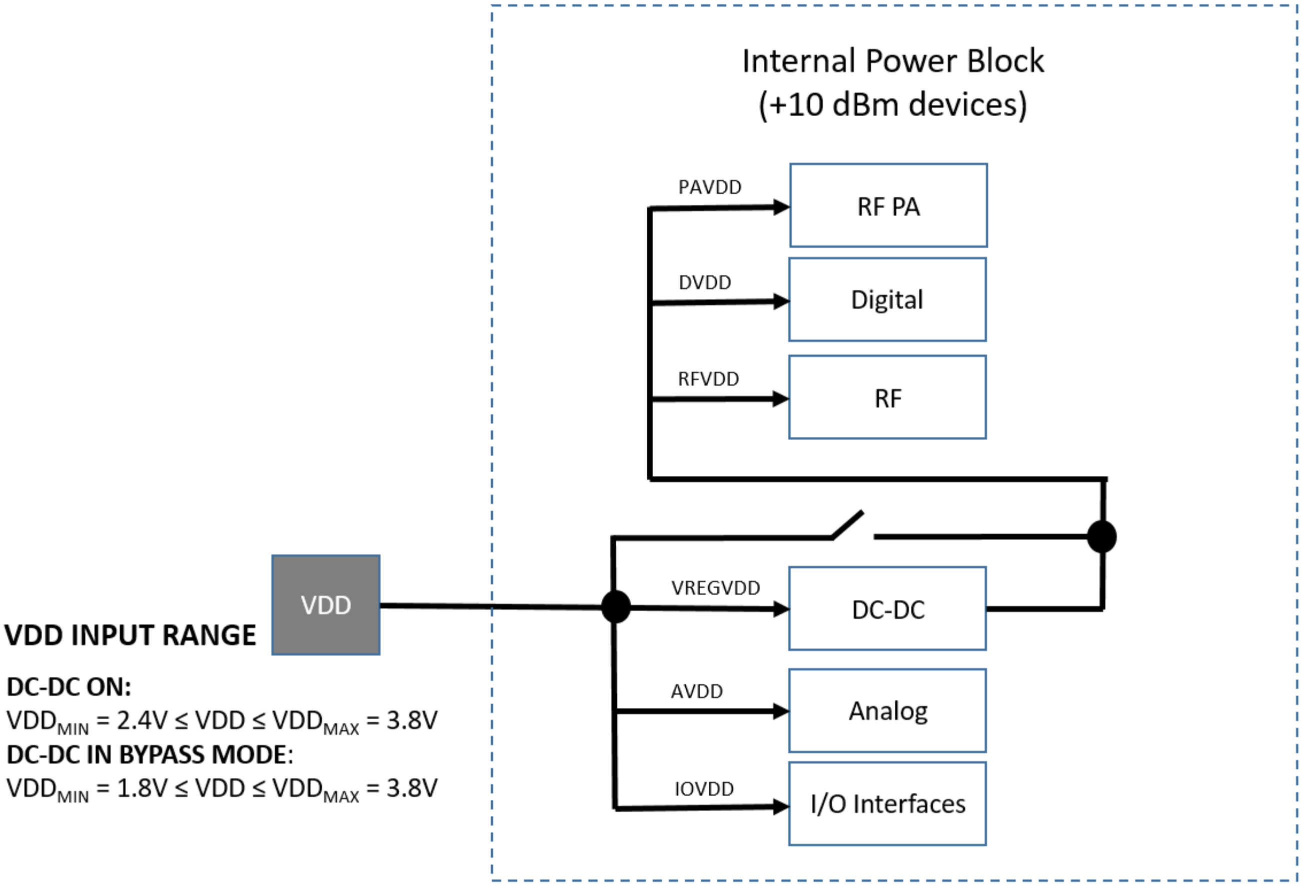

Figure 3.2. MGM12P Power Block for Modules (+10 dBm)

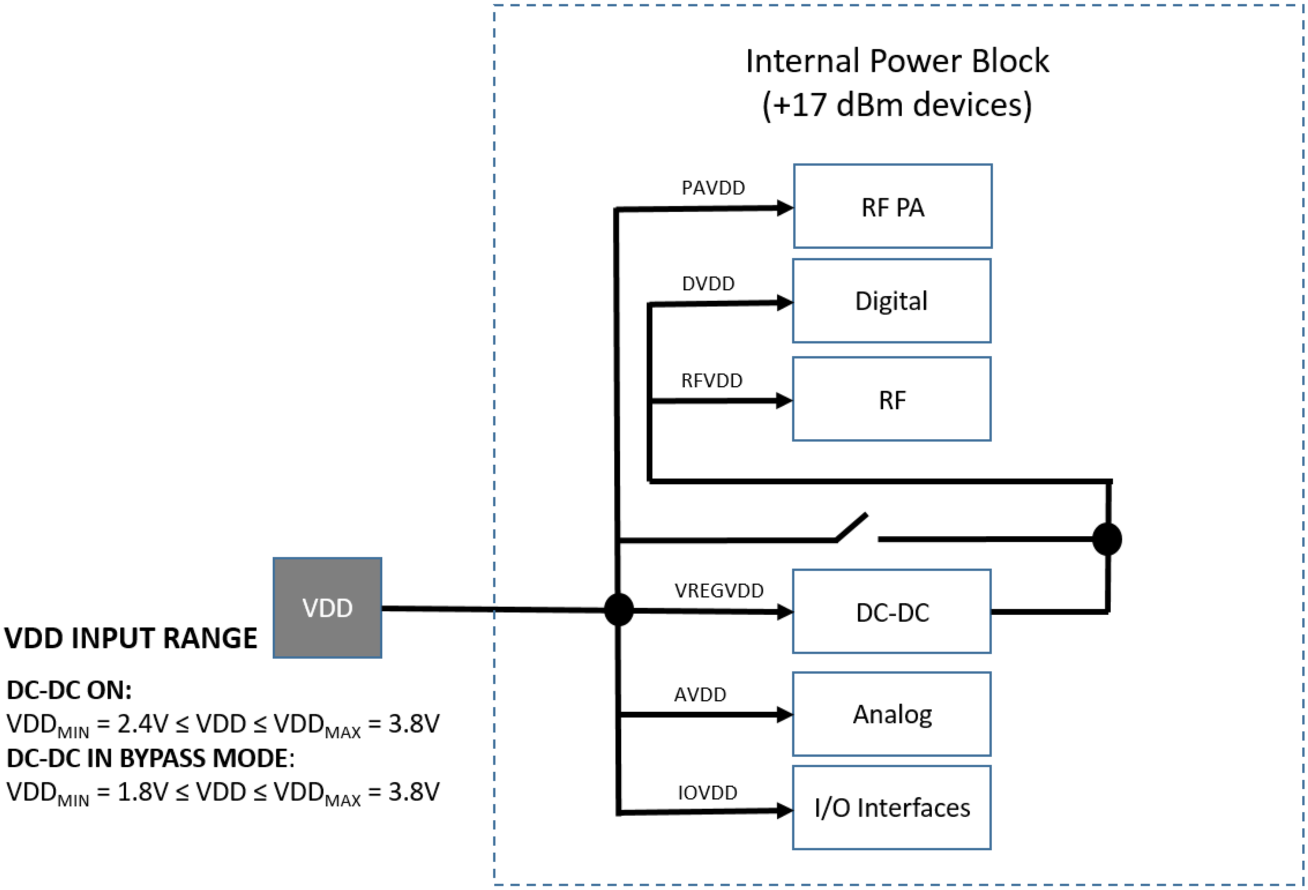

Figure 3.3. MGM12P Power Block for Modules (+17 dBm)

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2, and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The MGM12P has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.2. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	PCNT1
ADC0	PCNT2
LETIMER0	CSEN
LESENSE	DAC0
APORT	LEUART0
-	I2C0
-	I2C1
-	IDAC

3.4 General Purpose Input/Output (GPIO)

MGM12P has 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM12P. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators

The MGM12P fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM} provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement.

Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE^{TM} is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM12P. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 1024 KB flash program memory
- 256 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The MGM12P memory map is shown in the figures below.

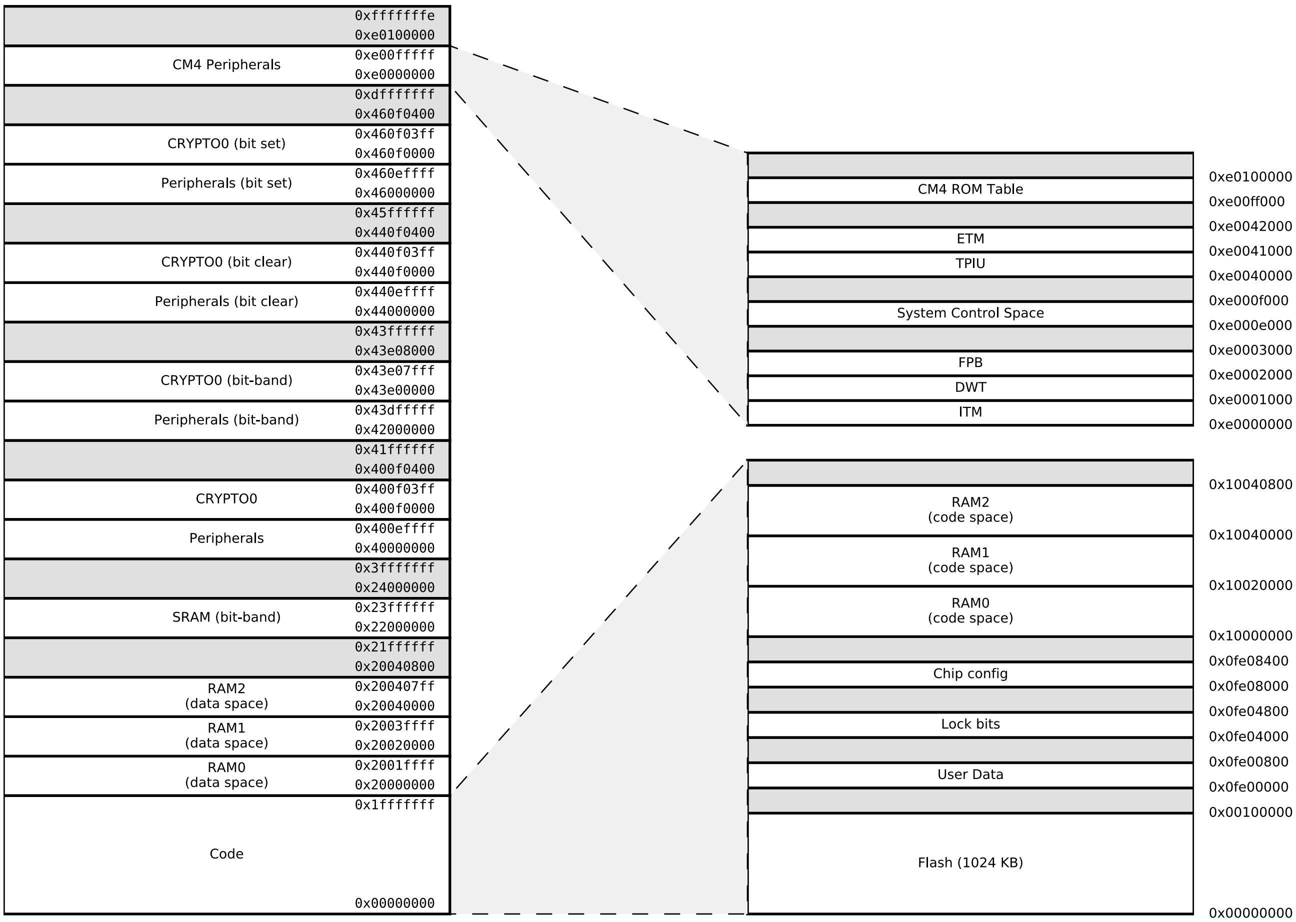

Figure 3.4. MGM12P Memory Map — Core Peripherals and Code Space

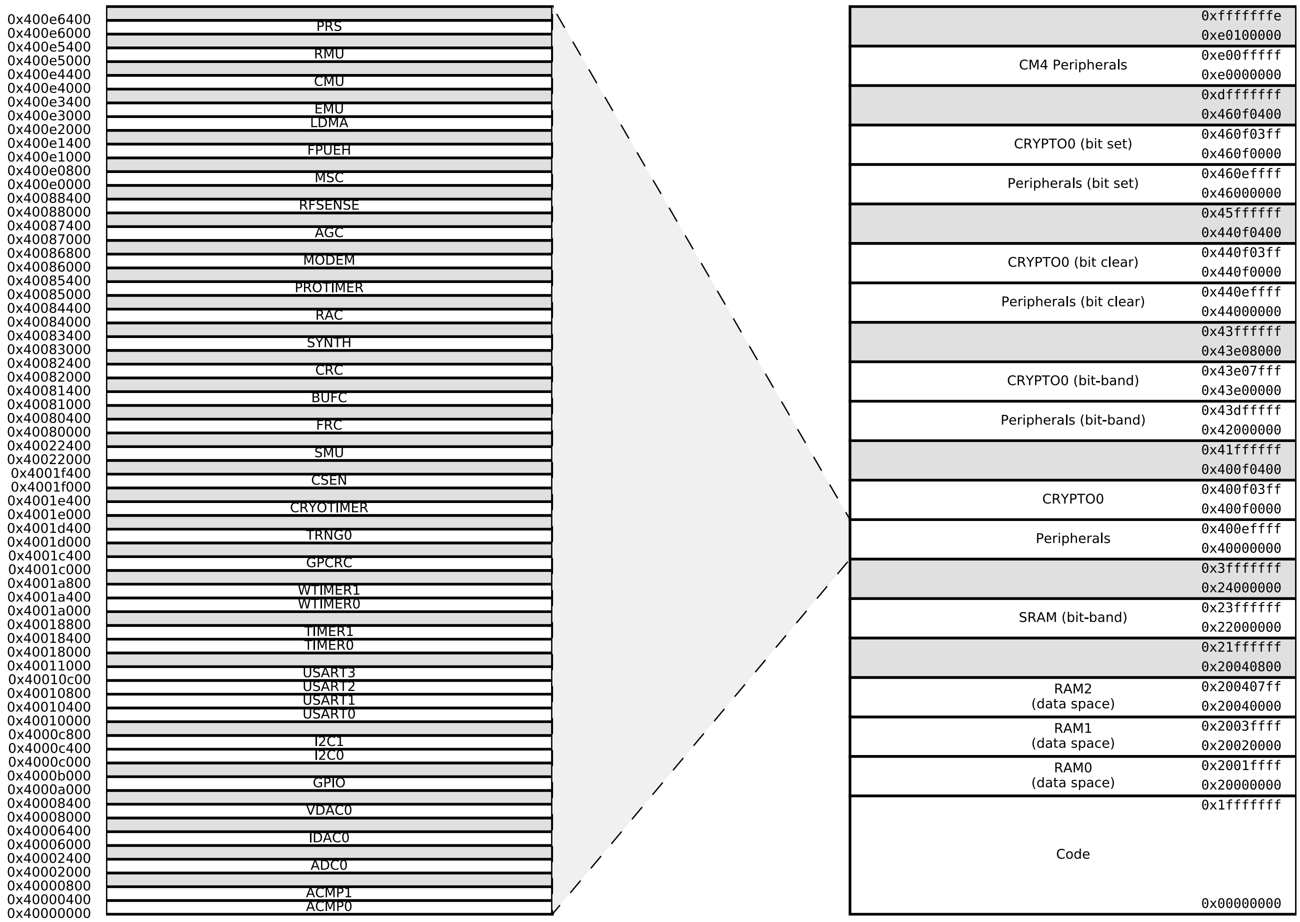

Figure 3.5. MGM12P Memory Map — Peripherals

3.13 Configuration Summary

The features of the MGM12P are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA SmartCard	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	IrDA I^2S SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Figure 3.2 MGM12P Power Block for Modules (+10 dBm) on page 9 and Figure 3.3 MGM12P Power Block for Modules (+17 dBm) on page 10 to see the relation between the modules external VDD pin and internal voltage supplies. The module has only one external power supply input (VDD).

Refer to 4.1.2 General Operating Conditions for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	85	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC Voltage on any over-voltage tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
			-0.3	—	IOVDD+0.3	V
Input RF level	$P_{RFMAX2G4}$		—	—	10	dBm
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Ambient temperature range	T_A	-G temperature grade	-40	25	85	°C
VDD supply voltage [1]	V_{VDD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass 50mA load	1.8	3.3	3.8	V
Core Clock Frequency	f_{CORE}	FWAIT = 1, VSCALE2	—	—	40	MHz
		FWAIT = 0, VSCALE0	—	—	20	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD}$ * R_{BYP_max}.

4.1.3 DC-DC Converter

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VDD}
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. In EMU_DCDCMISCCTRL register

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.4. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2].	I_{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	85	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	77	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	636	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1].	I_{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	95	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	95	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1155	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1].	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	101	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1155	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2].	I_{EM1_DCM}	38.4 MHz crystal[4]	—	59	—	µA/MHz
		38 MHz HFRCO	—	41	—	µA/MHz
		26 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	610	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2].	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	52	—	µA/MHz
		1 MHz HFRCO	—	587	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with votage scaling enabled, DCDC in LP mode. [3]	I_{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.62	—	μA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	2.72	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	2.02	—	μA
Current consumption in EM3 mode, with voltage scaling enabled.	I_{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.33	—	μA
Current consumption in EM4H mode, with voltage scaling enabled.	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.21	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.91	—	μA
		128 byte RAM retention, no RTCC	—	0.91	—	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.58	—	μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIM-SEL=1, ANASW=DVDD.
4. CMU_HFXOCTRL_LOWPOWER=0.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.4.2 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled). LNA in bypass.	I_{RX_ACTIVE}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.3	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	11.5	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	10.8	—	mA
Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled) LNA in bypass.	I_{RX_LISTEN}	1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	11.6	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	12.6	—	mA
		802.15.4, F = 2.4 GHz, No radio clock prescaling	—	12.3	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled) LNA in bypass.	I_{TX}	F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1	—	10	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	28	—	mA
		F = 2.4 GHz, CW, 10.5 dBm output power	—	37.4	—	mA
		F = 2.4 GHz, CW, 16.5 dBm output power, PAVDD connected directly to VDD	—	86	—	mA
		F = 2.4 GHz, CW, 19.5 dBm output power, PAVDD connected directly to VDD	—	131	—	mA

4.1.5 Wake Up Times

Table 4.6. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wakeup time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.1	—	μs
		Code execution from RAM	—	3.2	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.1	—	μs
		Code execution from RAM	—	3.2	—	μs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	80	—	μs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	291	—	μs
Time from release of reset source to first instruction ex-ecution.	t_{RESET}	Soft Pin Reset released	—	43	—	μs
		Any other reset released	—	350	—	μs
Power Mode Scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[2, 4]	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[2, 3]	—	4.3	—	

Note:

1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.

4.1.6 Brown Out Detector (BOD)

Table 4.7. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	1.3	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	1.53	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.7 Frequency Synthesizer

Table 4.8. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	f_{RANGE}	2400 - 2483.5 MHz	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	f_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Frequency deviation resolution with 38.4 MHz crystal	df_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	df_{MAX}	2400 - 2483.5 MHz	—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics