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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





MIC2101/02

38V, Synchronous Buck Controllers
Featuring Adaptive On-Time Control

Hyper Speed Control™ Family

General Description

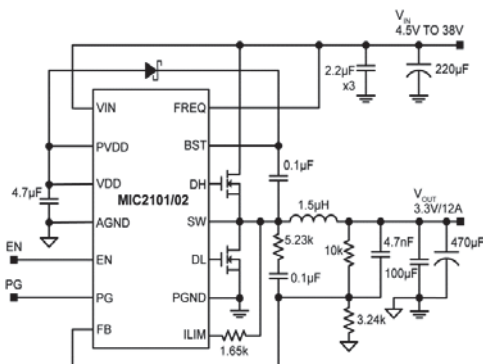
The Micrel MIC2101/02 are constant-frequency, synchronous buck controllers featuring a unique adaptive ON-time control architecture. The MIC2101/02 operates over an input supply range from 4.5V to 38V and can be used to supply up to 15A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of $\pm 1\%$. The device operates with programmable switching frequency from 200kHz to 600kHz.

Micrel's Hyper Light Load™ architecture provides the same high-efficiency and ultra-fast transient response as the Hyper Speed Control architecture under the medium to heavy loads, but also maintains high efficiency under light load conditions by transitioning to variable frequency, discontinuous-mode operation.

The MIC2101/02 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include under-voltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, fold-back current limit, "hiccup" mode short-circuit protection and thermal shutdown.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Typical Application



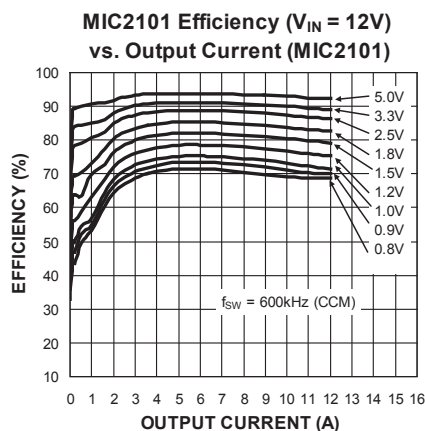
MIC2101/02 Wide Input, Hyper Light Load Buck Converter

Features

- Hyper Speed Control architecture enables:
 - High Delta V operation ($V_{IN} = 38V$ and $V_{OUT} = 1.2V$)
 - Any Capacitor™ stable
- 4.5V to 38V input voltage
- Adjustable output voltage from 0.8 V to 24V (also limited by duty cycle)
- 200kHz to 600kHz, programmable switching frequency
- Hyper Light Load Control (MIC2101)
- Hyper Speed Control (MIC2102)
- Enable input and Power Good output
- Built-in 5V regulator for single-supply operation
- Programmable current limit and fold-back "hiccup" mode short-circuit protection
- 5ms internal soft-start, internal compensation, and thermal shutdown
- Supports safe start-up into a pre-biased output
- $-40^{\circ}C$ to $+125^{\circ}C$ junction temperature range
- Available in 16-pin 3mm x 3mm QFN package

Applications

- Distributed power systems
- Networking/telecom Infrastructure
- Printers, scanners, graphic cards, and video cards



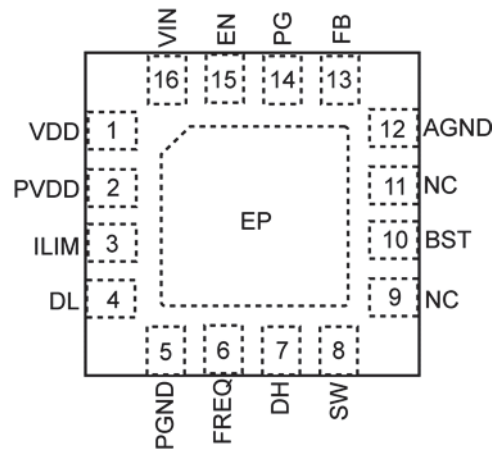
Hyper Speed Control, Hyper Light Load, and Any Capacitor are trademarks of Micrel, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

Ordering Information

Part Number	Switching Frequency	Features	Package	Junction Temperature Range	Lead Finish
MIC2101YML	200kHz to 600kHz	Hyper Light Load	16-Pin 3mm x 3mm QFN	-40°C to +125°C	Pb-Free
MIC2102YML	200kHz to 600kHz	Hyper Speed Control	16-Pin 3mm x 3mm QFN	-40°C to +125°C	Pb-Free

Pin Configuration



16-Pin 3mm x 3mm QFN (ML)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Internal +5V Linear Regulator Output. VDD is the internal supply bus for the device. A 4.7 μ F ceramic capacitor from VDD to AGND is required for decoupling. In the applications with VIN < +5.5V, VDD should be tied to VIN to by-pass the linear regulator.
2	PVDD	5V supply input for the low-side N-channel MOSFET driver, which can be tied to VDD externally. A 4.7 μ F ceramic capacitor from PVDD to PGND is recommended for decoupling.
3	ILIM	Current Limit Setting. Connect a resistor from SW to ILIM to set the over-current threshold for the converter.
4	DL	Low-Side Drive output. High-current driver output for external low-side MOSFET of a buck converter. The DL driving voltage swings from ground to VDD. Adding a small resistor between DL pin and the gate of the low-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
5	PGND	Power Ground. PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of low-side N-Channel external MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. The return path for the power ground should be as small as possible and separate from the signal ground (AGND) return path.
6	FREQ	Switching Frequency Adjust input. Tie this pin to VIN to operate at 600kHz and place a resistor divider to reduce the frequency.

Pin Configuration (Continued)

Pin Number	Pin Name	Pin Function
7	DH	High-Side Drive Output. High-current driver output for external high-side MOSFET of a buck converter. The DH driving voltage is floating on the switch node voltage (V_{SW}). Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
8	SW	Switch Node and Current-Sense input. High current output driver return. The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to the SW pin using a Kelvin connection.
9, 11	NC	No Connection.
10	BST	Voltage supply input for the high-side N-channel MOSFET driver, which can be powered by a bootstrapped circuit connected between VDD and SW, using a Schottky diode and a 0.1 μ F ceramic capacitor. Adding a small resistor at BST pin can slow down the turn-on speed of the high-side MOSFET.
12	AGND	Signal ground for VDD and the control circuitry, which is connected to thermal pad electronically. The signal ground return path should be separate from the power ground (PGND) return path.
13	FB	Feedback Input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage.
14	PG	Power Good Output. Open drain output, an external pull-up resistor to VDD or external power rails is required.
15	EN	Enable Input. A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shutdowns the regulator. In the disable mode, the VDD supply current for the device is minimized to 0.7mA typically. Do not pull EN pin to VDD/PVDD.
16	VIN	Supply Voltage. The VIN operating voltage range is from 4.5V to 38V. A 1 μ F ceramic capacitor from VIN to AGND is required for decoupling.
EP	ePad	Exposed Pad. Connect the EPAD to PGND plain on the PCB to improve the thermal performance.

Absolute Maximum Ratings⁽¹⁾

V_{IN}	-0.3V to +40V
V_{DD} , V_{PVDD}	-0.3V to +6V
V_{SW} , V_{FREQ} , V_{ILIM} , V_{EN}	-0.3V to ($V_{IN} + 0.3V$)
V_{BST} to V_{SW}	-0.3V to 6V
V_{BST}	-0.3V to 46V
V_{PG}	-0.3V to ($V_{DD} + 0.3V$)
V_{FB}	-0.3V to ($V_{DD} + 0.3V$)
PGND to AGND	-0.3V to +0.3V
Junction Temperature	+150°C
Storage Temperature (T_S)	-65°C to +150°C
Lead Temperature (soldering, 10s)	260°C
ESD Rating ⁽²⁾	ESD Sensitive

Operating Ratings⁽³⁾

Supply Voltage (V_{IN})	4.5V to 38V
Enable Input (V_{EN})	0V to V_{IN}
V_{SW} , V_{FREQ} , V_{ILIM} , V_{EN}	0V to V_{IN}
Junction Temperature (T_J)	-40°C to +125°C
Junction Thermal Resistance	
3mm x 3mm QFN-16 (θ_{JA})	50.8°C/W
3mm x 3mm QFN-16 (θ_{JC})	25.3°C/W

Electrical Characteristics⁽⁴⁾

$V_{IN} = 12V$, $V_{OUT} = 1.2V$; $V_{BST} - V_{SW} = 5V$; $T_A = 25^\circ C$, unless noted. **Bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (V_{IN}) ⁽⁵⁾		4.5		38	V
Quiescent Supply Current (MIC2101)	$V_{FB} = 1.5V$		400	750	μA
Quiescent Supply Current (MIC2102)	$V_{FB} = 1.5V$		2.1	3	mA
Shutdown Supply Current	SW unconnected, $V_{EN} = 0V$		0.1	10	μA
VDD Supply					
VDD Output Voltage	$V_{IN} = 7V$ to 38V, $I_{DD} = 10mA$	4.8	5.2	5.4	V
VDD UVLO Threshold	V_{DD} rising	3.8	4.2	4.6	V
VDD UVLO Hysteresis			400		mV
Load Regulation	$I_{DD} = 0$ to 40mA	0.6	2	3.6	%
Reference					
Feedback Reference Voltage	$T_J = 25^\circ C (\pm 1.0\%)$	0.792	0.8	0.808	V
	$-40^\circ C \leq T_J \leq 125^\circ C (\pm 2\%)$	0.784	0.8	0.816	
FB Bias Current	$V_{FB} = 0.8V$		5	500	nA
Enable Control					
EN Logic Level High		1.8			V
EN Logic Level Low				0.6	V
EN Hysteresis			200		mV
EN Bias Current	$V_{EN} = 12V$		6	30	μA

Notes:

- Exceeding the absolute maximum rating may damage the device.
- Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k Ω in series with 100pF.
- The device is not guaranteed to function outside operating range.
- Specification for packaged product only.
- The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH} .

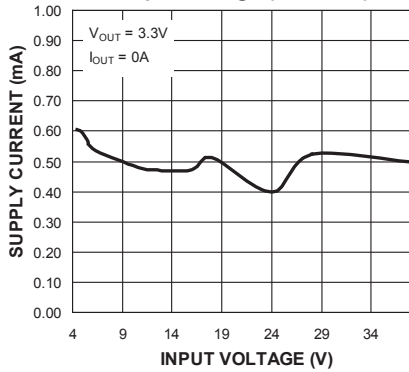
Electrical Characteristics⁽⁴⁾ (Continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$; $V_{BST} - V_{SW} = 5V$; $T_A = 25^\circ C$, unless noted. **Bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$.

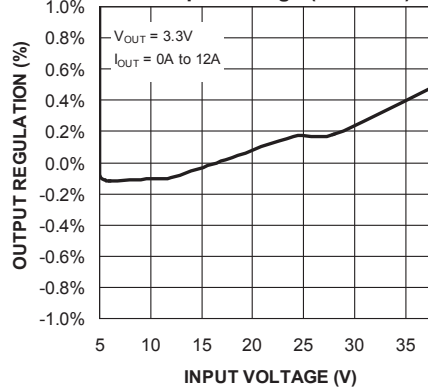
Parameter	Condition	Min.	Typ.	Max.	Units
Oscillator					
Switching Frequency	$V_{FREQ} = V_{IN}$	400	600	750	kHz
	$V_{FREQ} = 50\%V_{IN}$		300		
Maximum Duty Cycle			85		%
Minimum Duty Cycle	$V_{FB} > 0.8V$		0		%
Minimum Off-Time		140	200	260	ns
Soft-Start					
Soft-Start time			5		ms
Short-Circuit Protection					
Current-Limit Threshold	$V_{FB} = 0.79V$	-30	-14	0	mV
Short-Circuit Threshold	$V_{FB} = 0V$	-23	-7	9	mV
Current-Limit Source Current	$V_{FB} = 0.79V$	60	80	100	μA
Short-Circuit Source Current	$V_{FB} = 0V$	27	37	47	μA
FET Drivers					
DH, DL Output Low Voltage	$I_{SINK} = 10mA$			0.1	V
DH, DL Output High Voltage	$I_{SOURCE} = 10mA$	$V_{PVDD} - 0.1V$ or $V_{BST} - 0.1V$			V
DH On-Resistance, High State			2.1	3.3	Ω
DH On-Resistance, Low State			1.8	3.3	Ω
DL On-Resistance, High State			1.8	3.3	Ω
DL On-Resistance, Low State			1.2	2.3	Ω
SW, BST Leakage Current				50	μA
Power Good (PG)					
PG Threshold Voltage	Sweep V_{FB} from Low to High	85	90	95	$\%V_{OUT}$
PG Hysteresis	Sweep V_{FB} from High to Low		6		$\%V_{OUT}$
PG Delay Time	Sweep V_{FB} from Low to High		100		μs
PG Low Voltage	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1mA$		70	200	mV
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		160		$^\circ C$
Over-Temperature Shutdown Hysteresis			7		$^\circ C$

Typical Characteristics

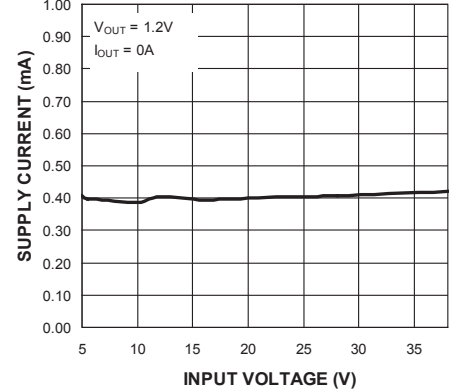
V_{IN} Operating Supply Current vs. Input Voltage (MIC2101)



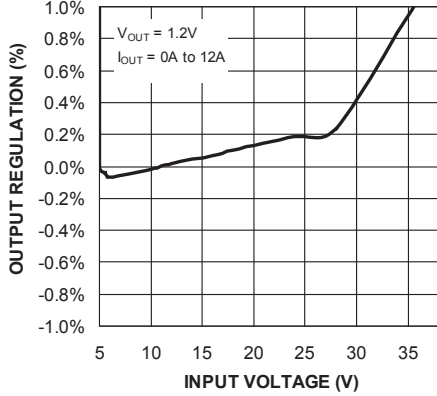
Output Regulation vs. Input Voltage (MIC2101)



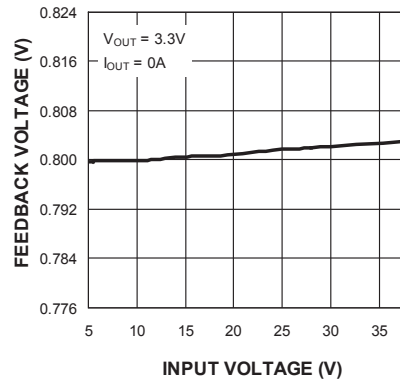
V_{IN} Operating Supply Current vs. Input Voltage (MIC2101)



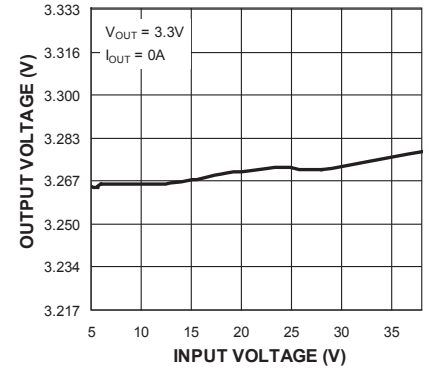
Output Regulation vs. Input Voltage (MIC2101)



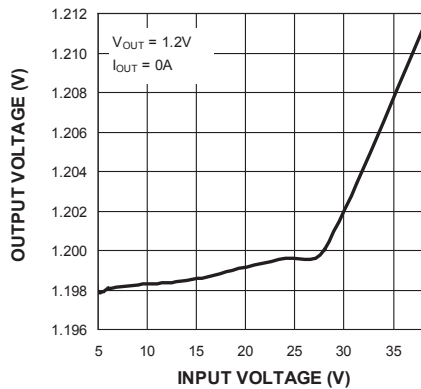
Feedback Voltage vs. Input Voltage (MIC2101)



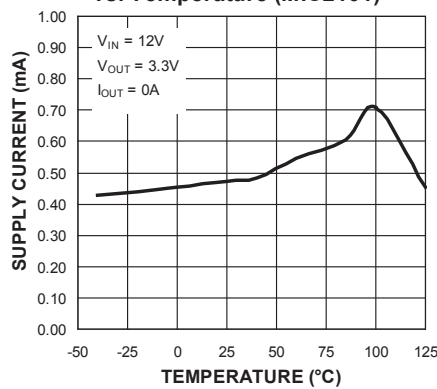
Output Voltage vs. Input Voltage (MIC2101)



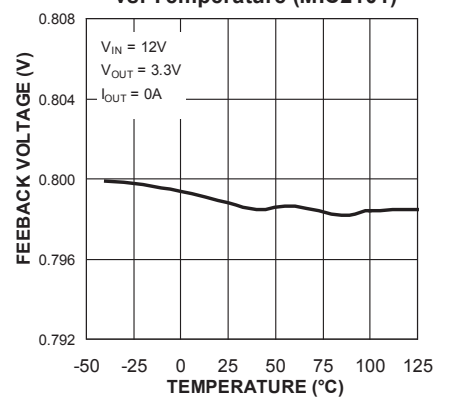
Output Voltage vs. Input Voltage (MIC2101)



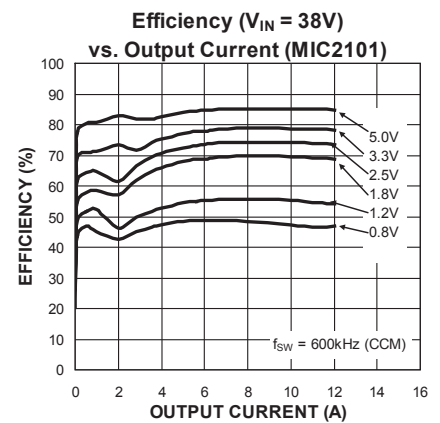
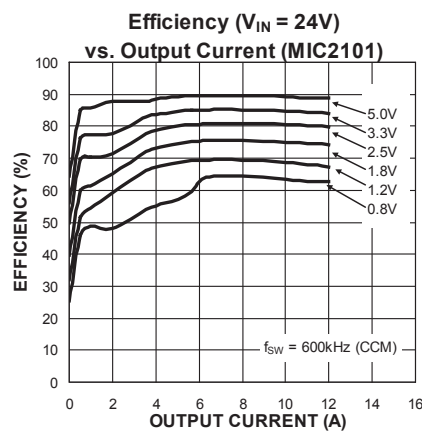
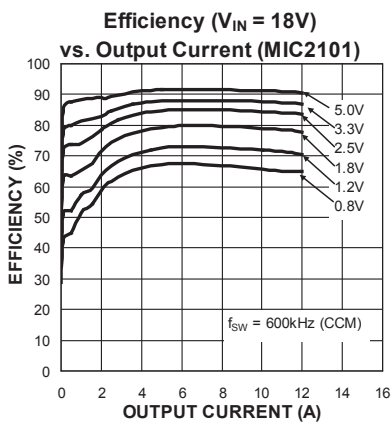
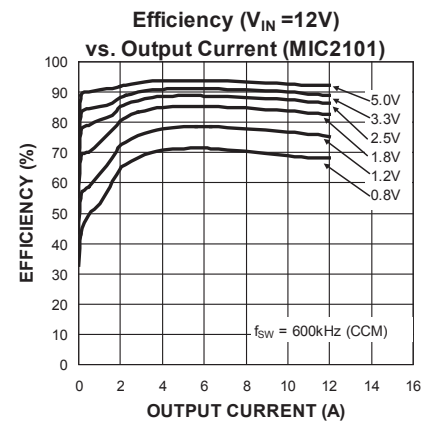
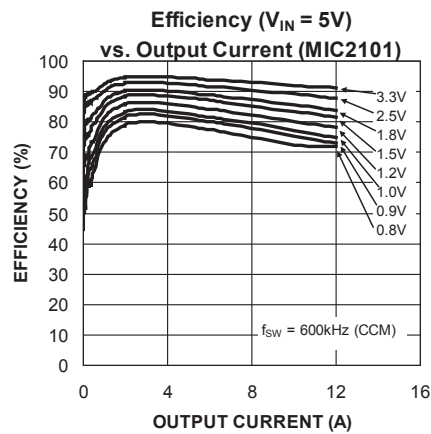
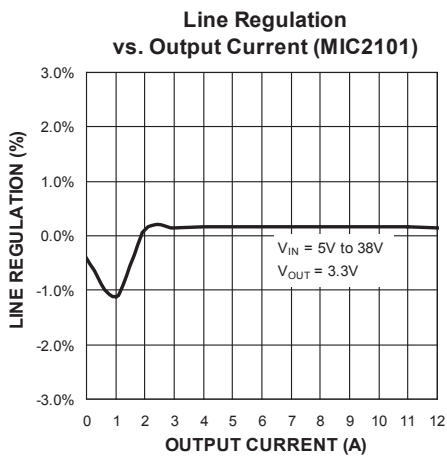
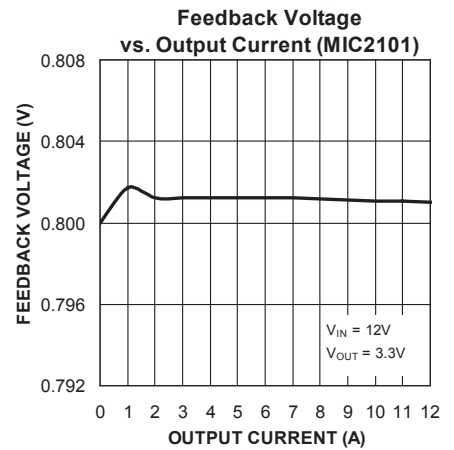
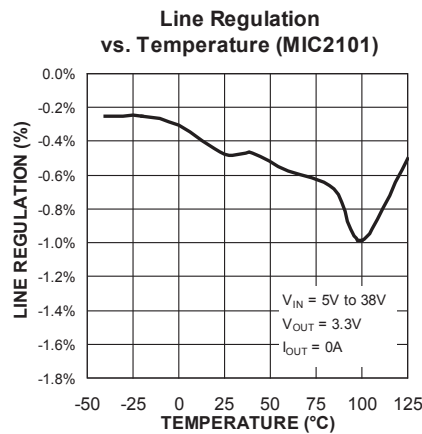
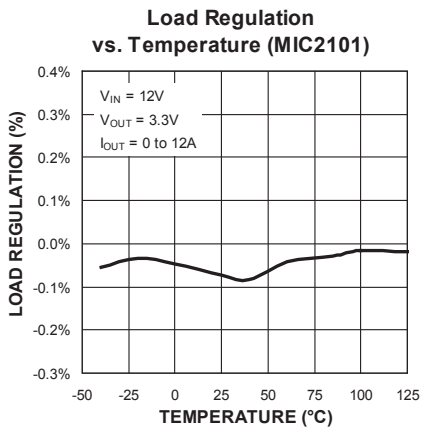
V_{IN} Operating Supply Current vs. Temperature (MIC2101)



Feedback Voltage vs. Temperature (MIC2101)

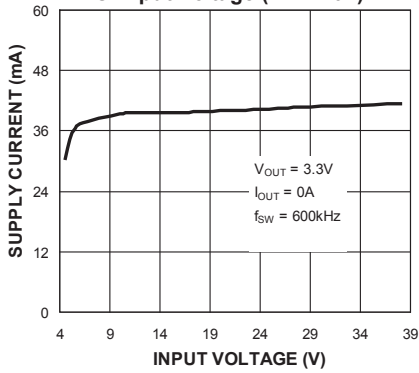


Typical Characteristics (Continued)

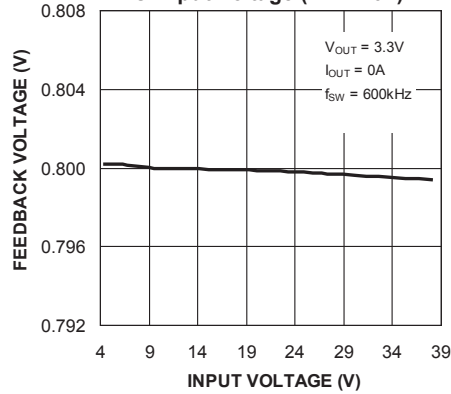


Typical Characteristics (Continued)

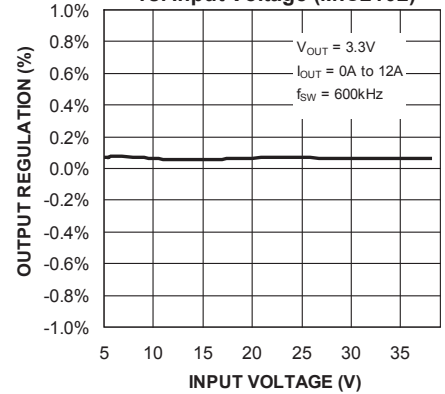
V_{IN} Operating Supply Current vs. Input Voltage (MIC2102)



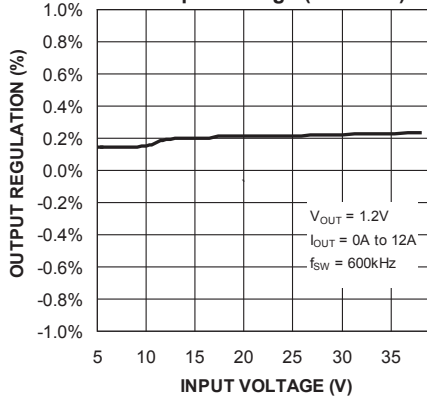
Feedback Voltage vs. Input Voltage (MIC2102)



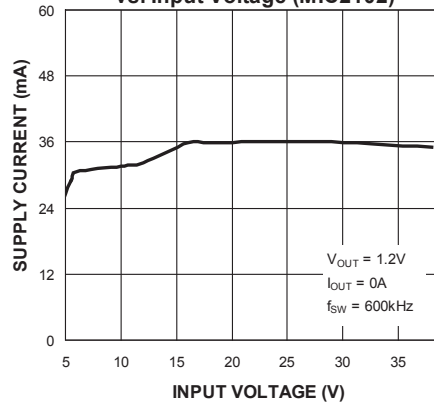
Output Regulation vs. Input Voltage (MIC2102)



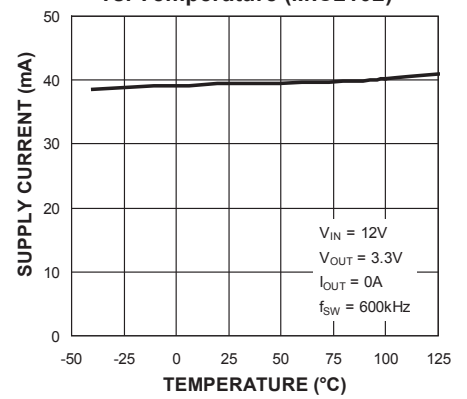
Output Regulation vs. Input Voltage (MIC2102)



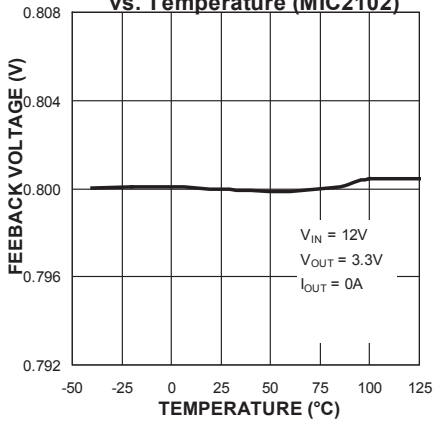
V_{IN} Operating Supply Current vs. Input Voltage (MIC2102)



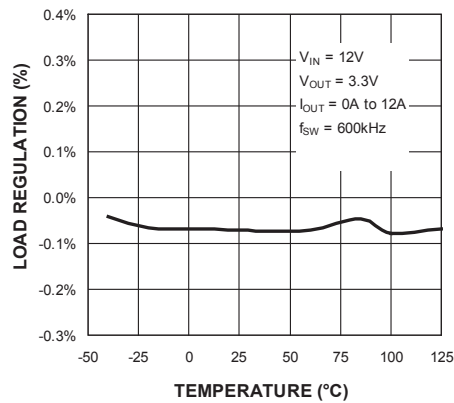
V_{IN} Operating Supply Current vs. Temperature (MIC2102)



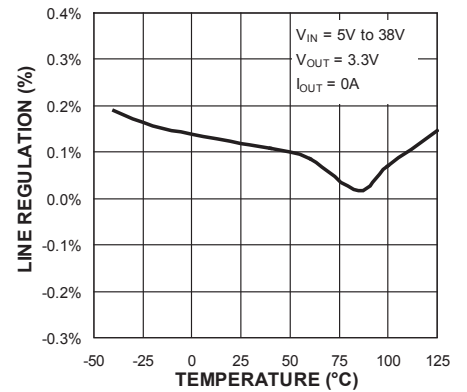
Feedback Voltage vs. Temperature (MIC2102)



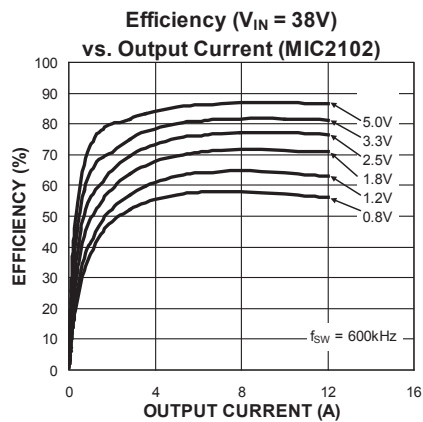
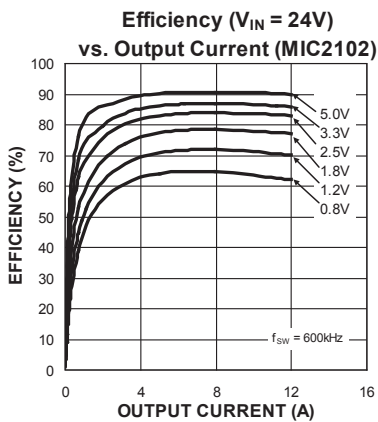
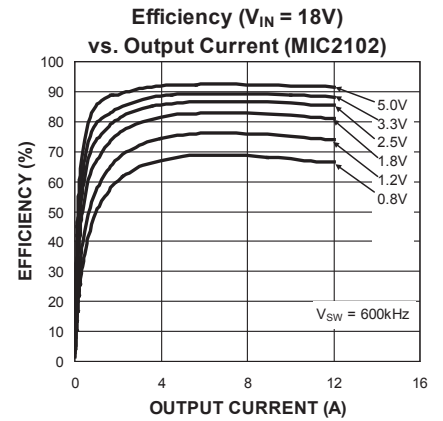
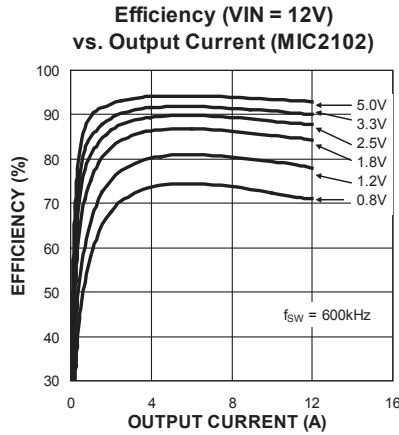
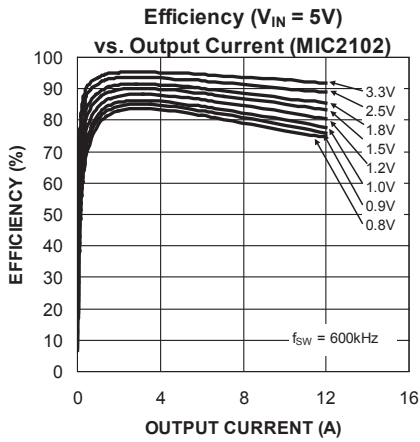
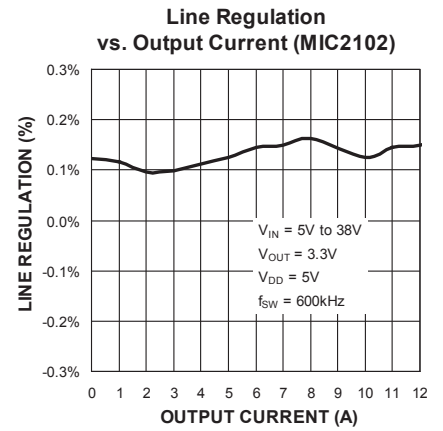
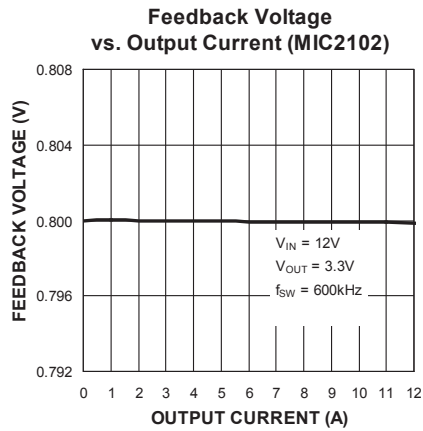
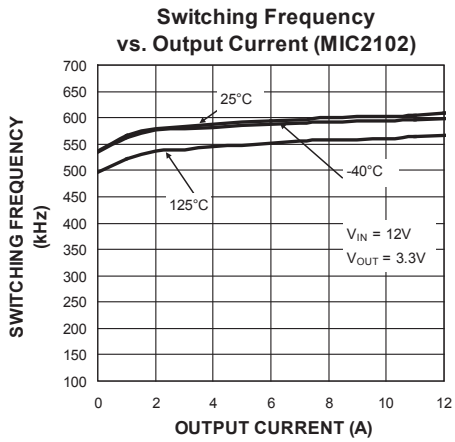
Load Regulation vs. Temperature (MIC2102)



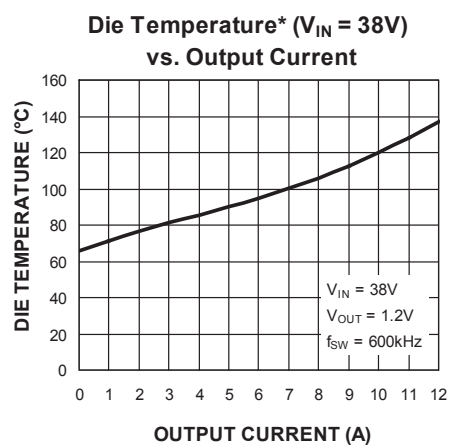
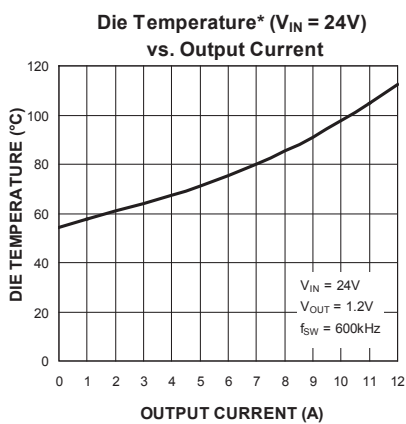
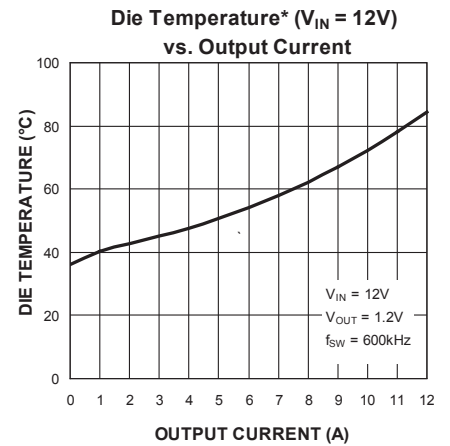
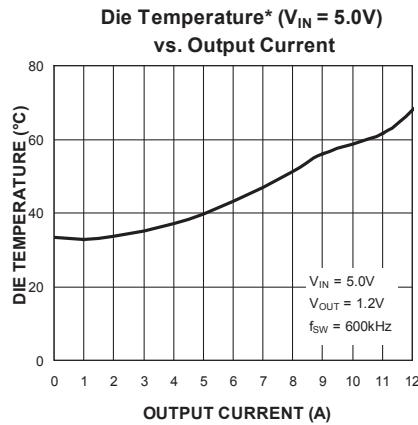
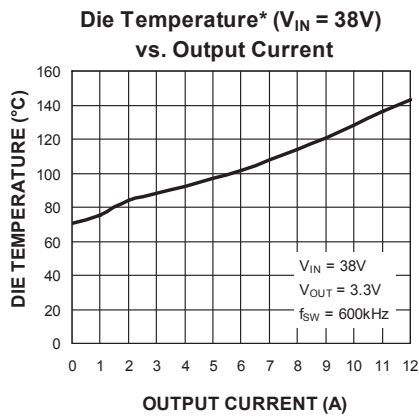
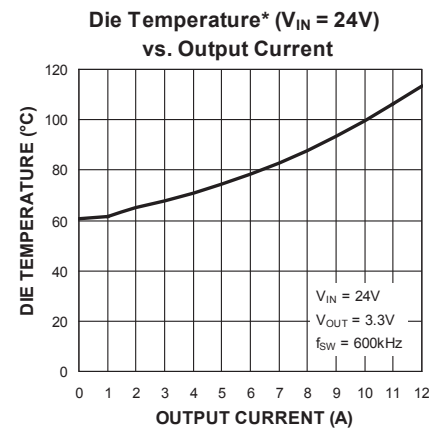
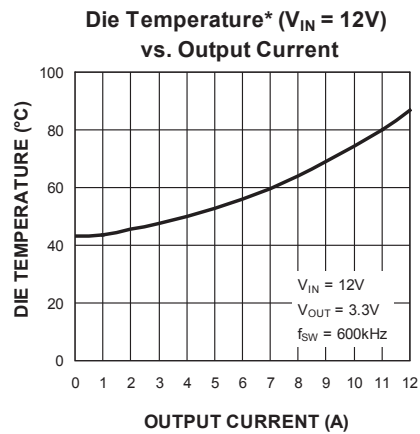
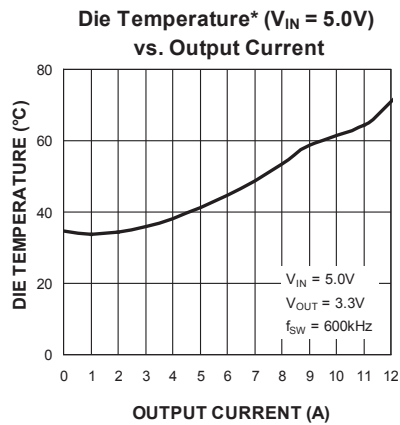
Line Regulation vs. Temperature (MIC2102)



Typical Characteristics (Continued)

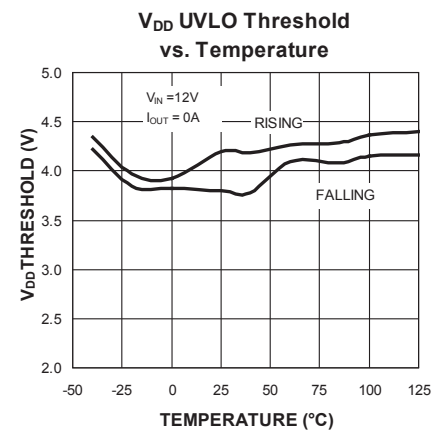
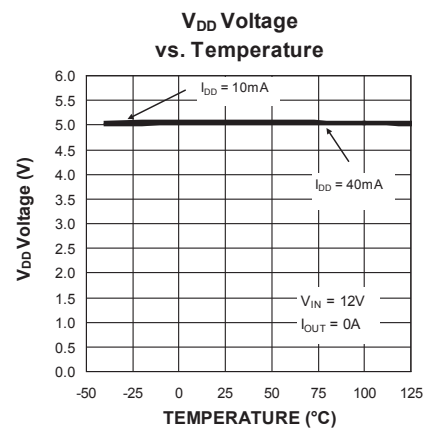
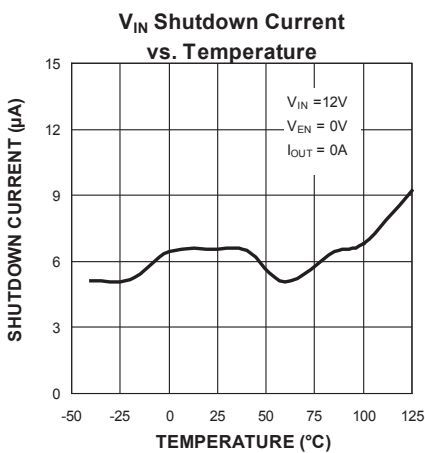
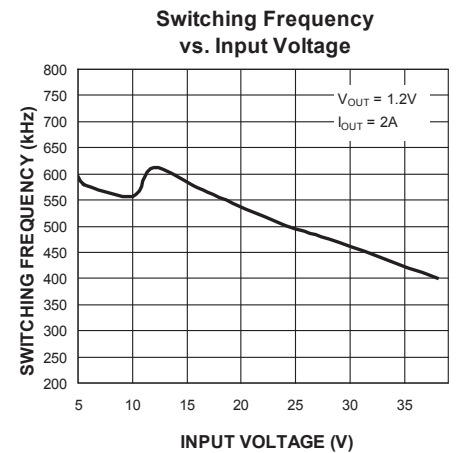
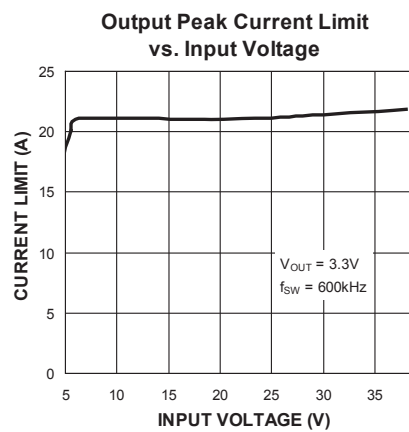
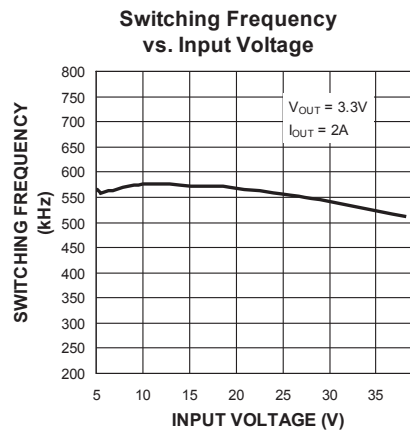
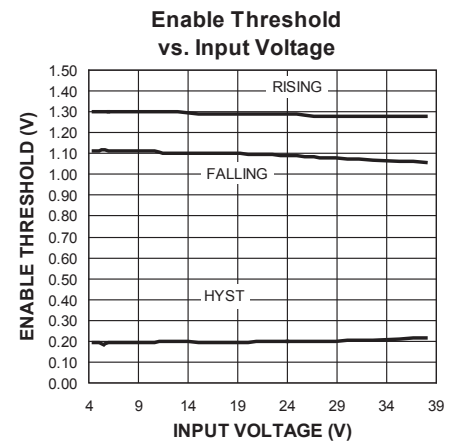
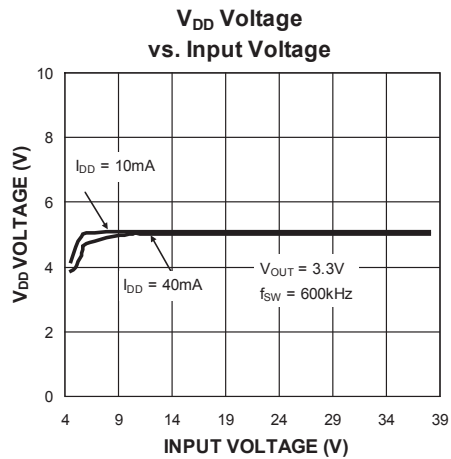
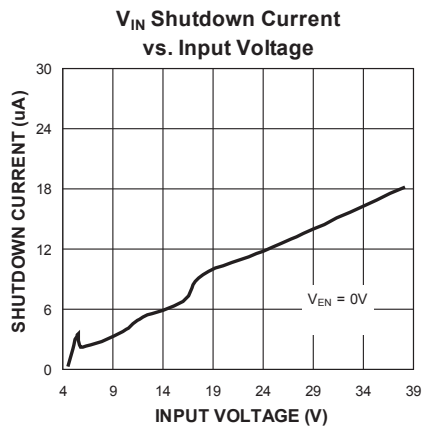


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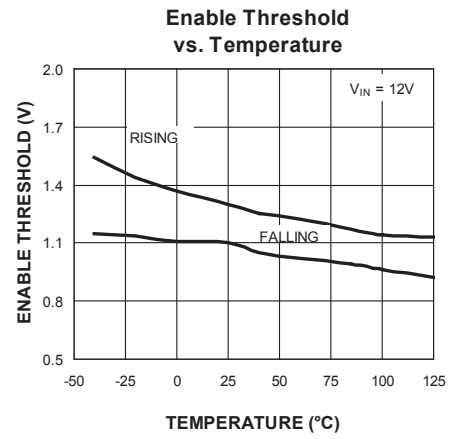
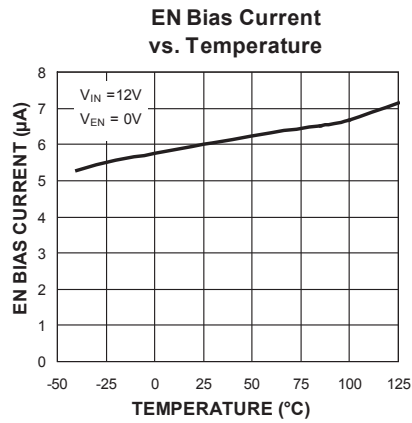
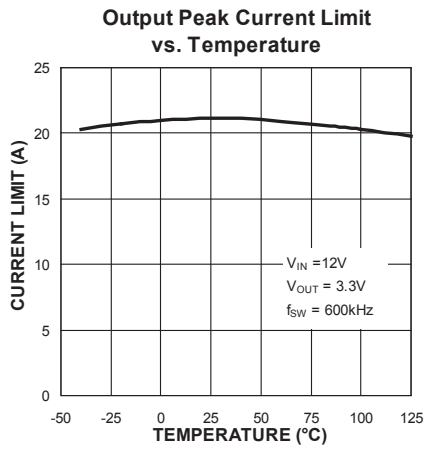


Case Temperature*: The temperature measurement was taken at the hottest point on the MIC2101/02 case mounted on a 5 square inch PCB, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

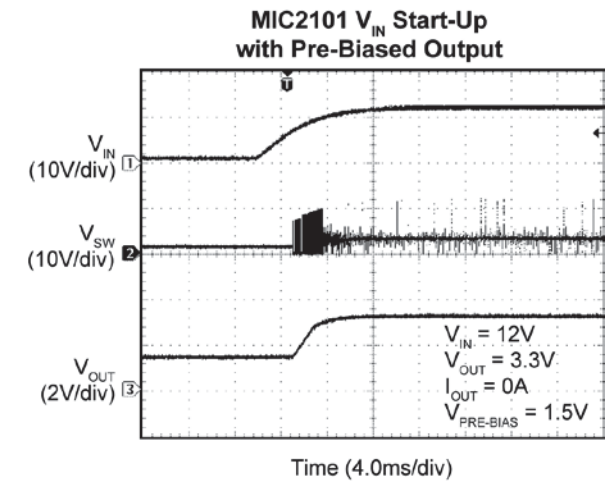
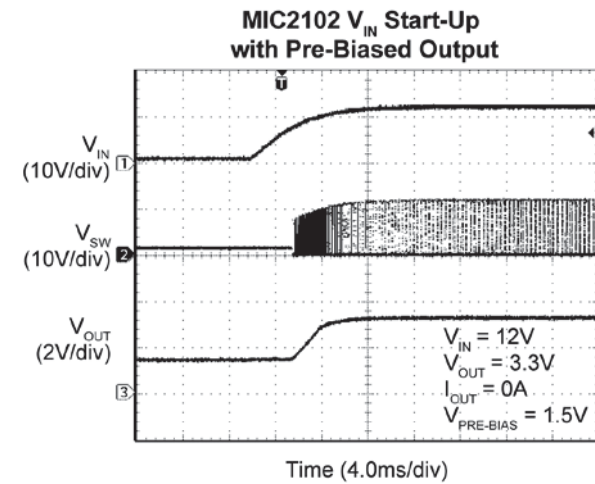
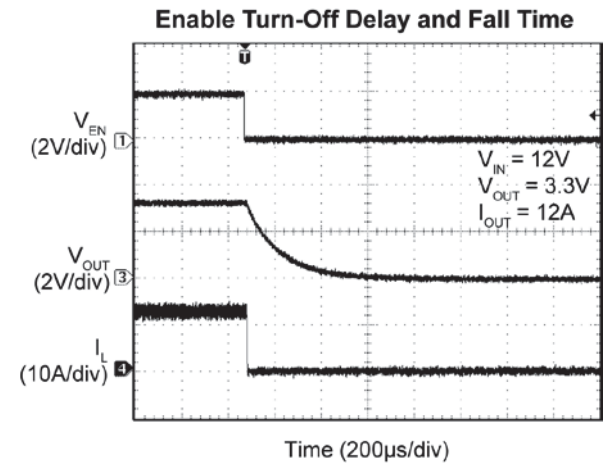
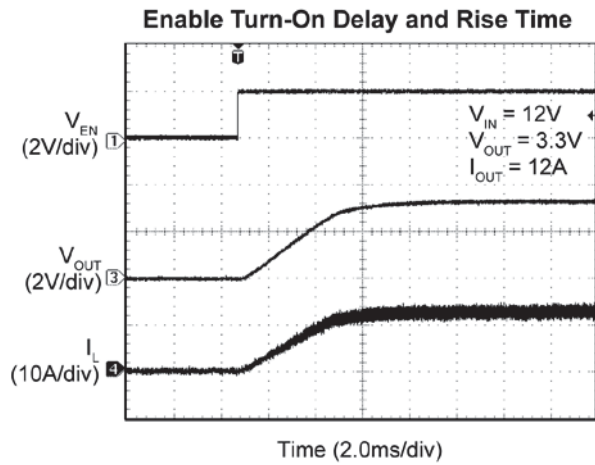
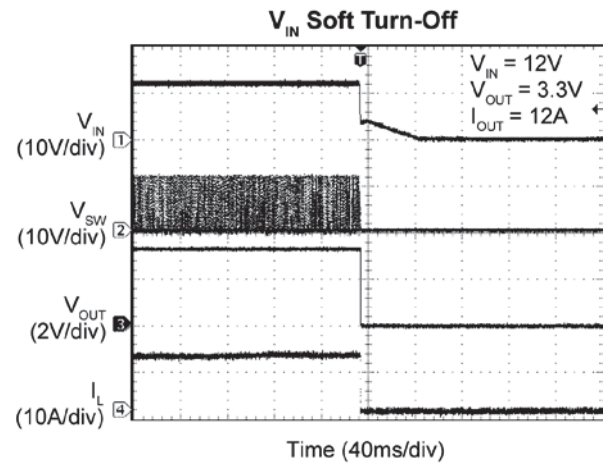
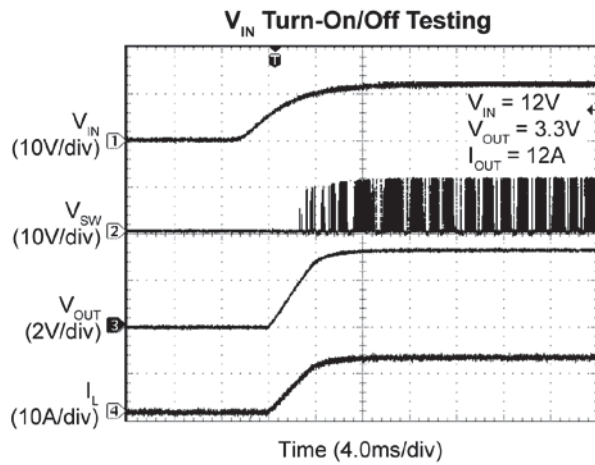
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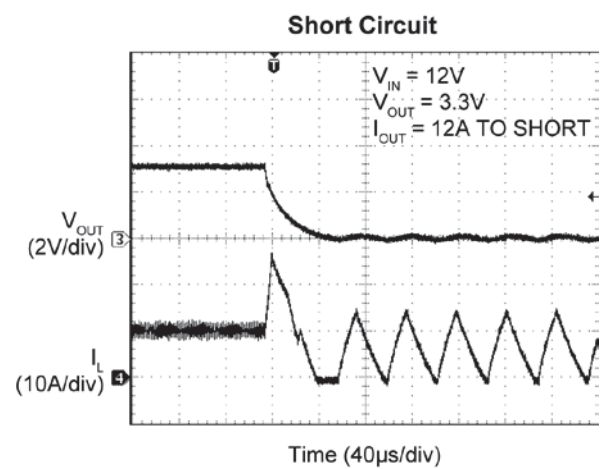
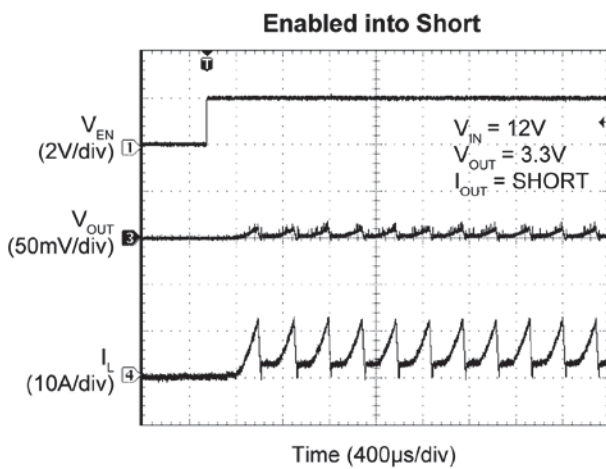
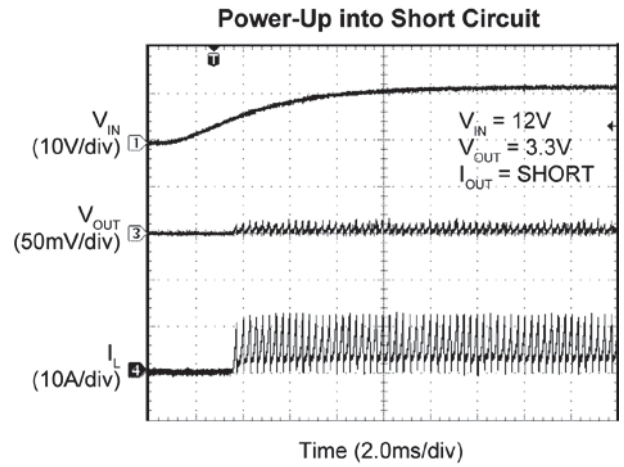
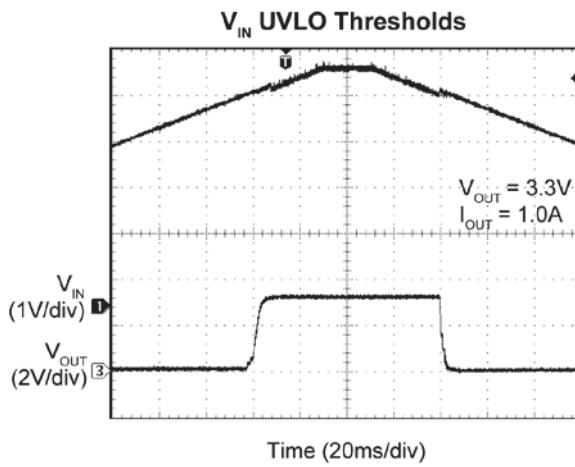
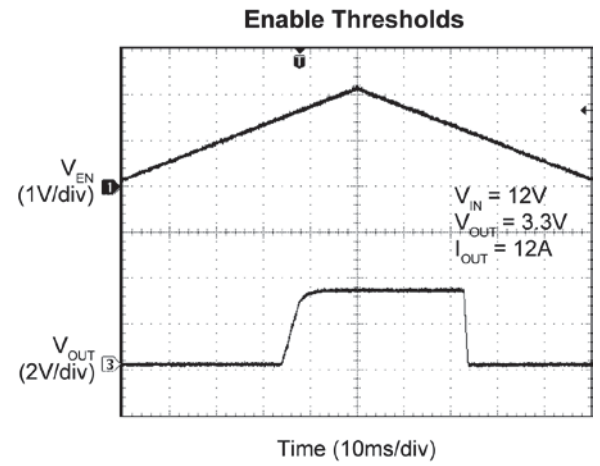
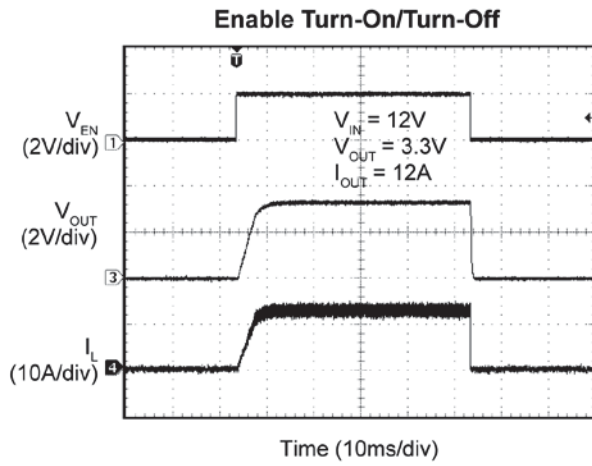
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Functional Characteristics

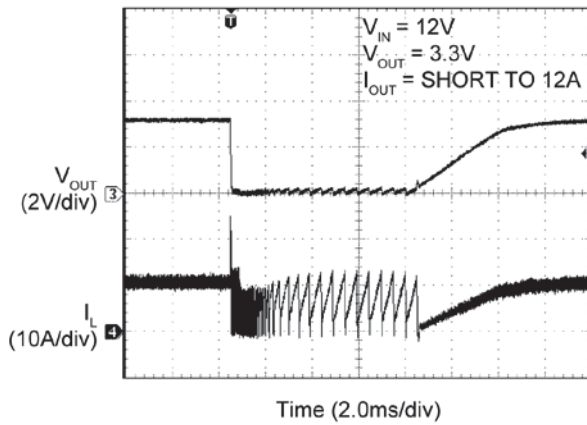


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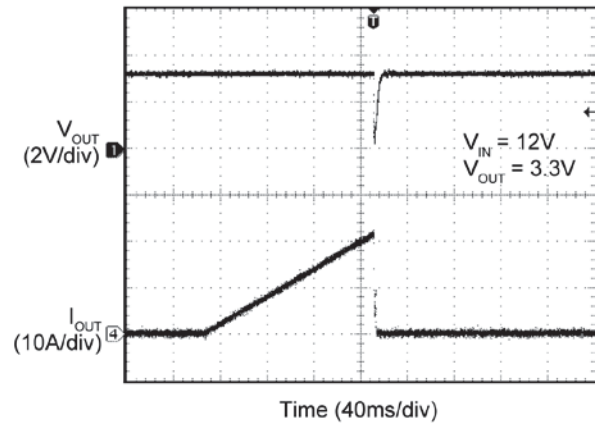


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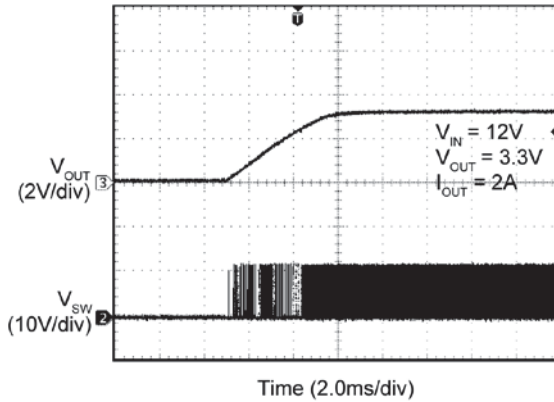
Output Recovery from Short Circuit



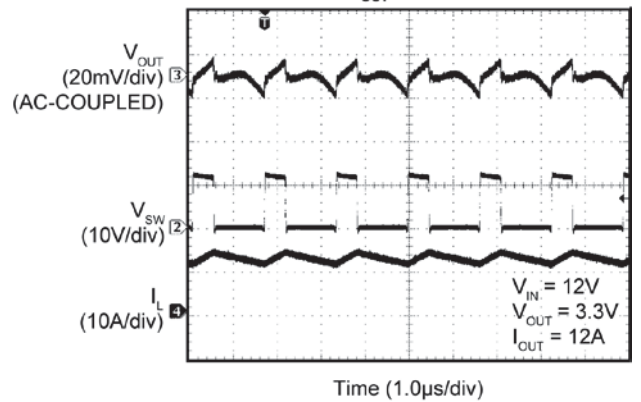
Output Peak Current-Limit Threshold



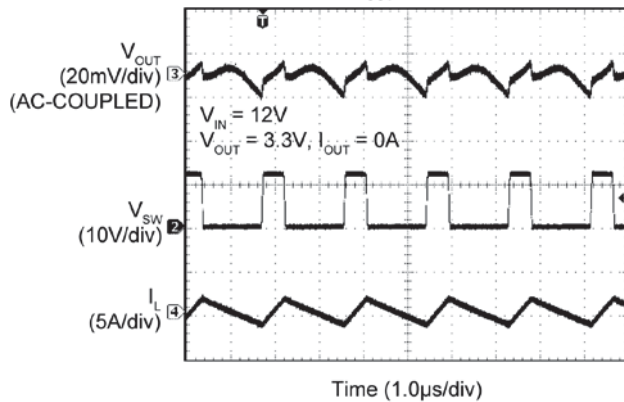
Output Recovery from Thermal Shutdown



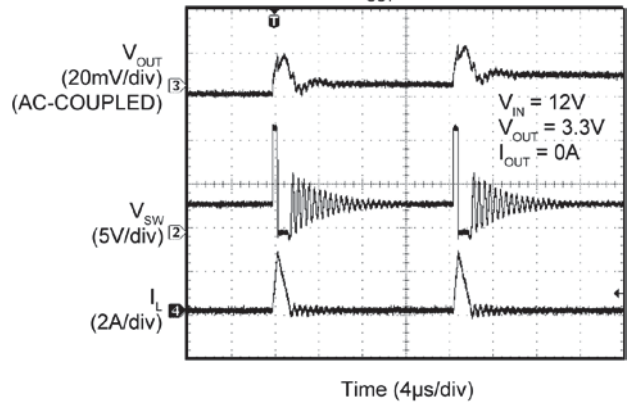
MIC2102 Switching Waveforms ($I_{OUT} = 12A$)



MIC2102 Switching Waveforms ($I_{OUT} = 0A$)

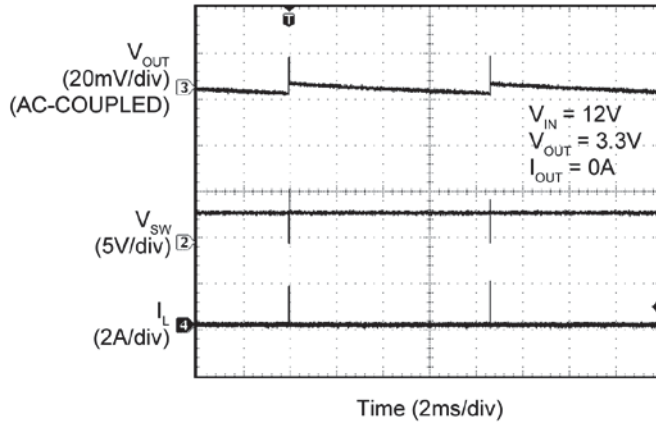


MIC2101 Switching Waveforms ($I_{OUT} = 0A$)

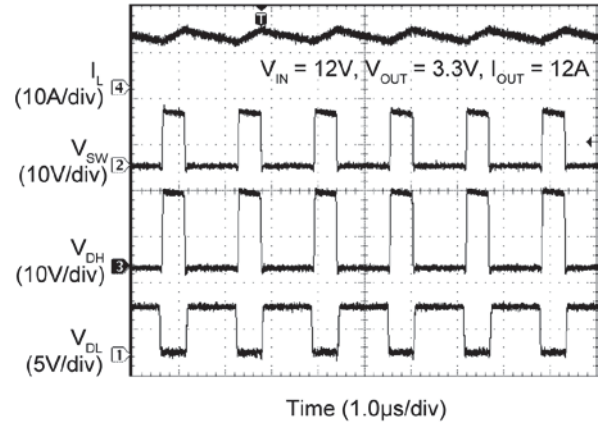


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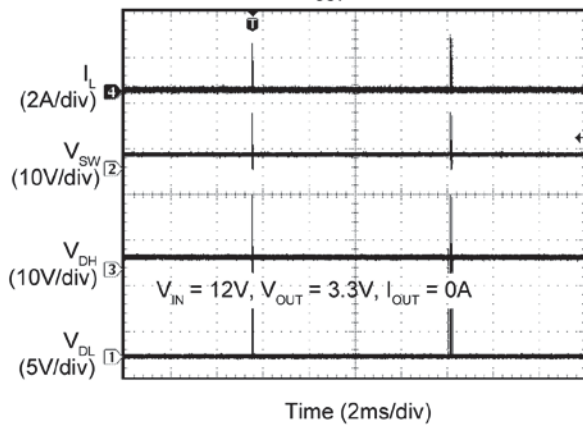
MIC2101 Switching Waveforms
($I_{OUT} = 0A$)



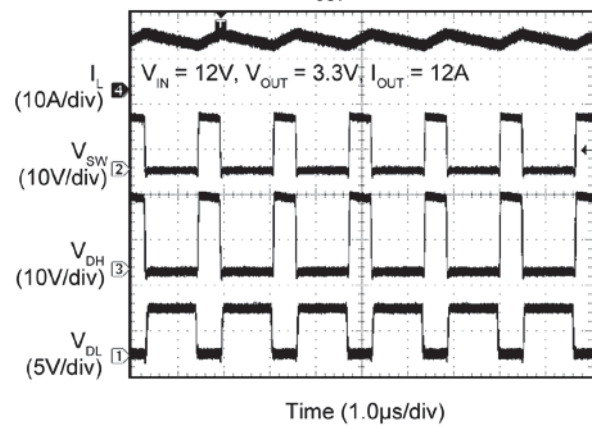
MIC2101 Switching Waveforms
($I_{OUT} = 12A$)



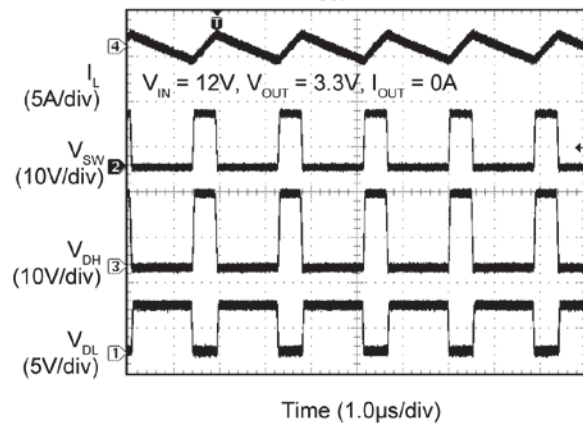
MIC2101 Switching Waveforms
($I_{OUT} = 0A$)



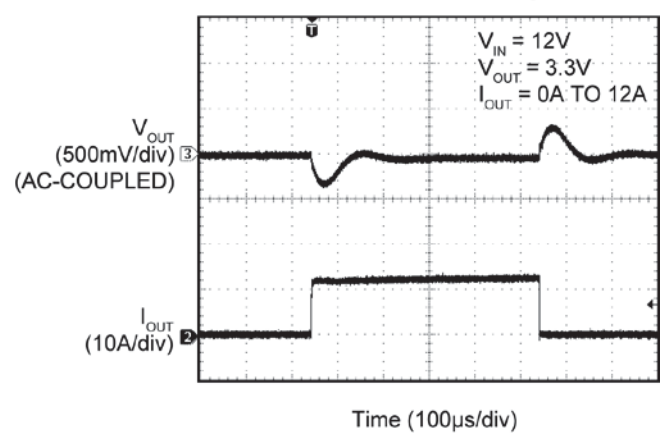
MIC2102 Switching Waveforms
($I_{OUT} = 12A$)



MIC2102 Switching Waveforms
($I_{OUT} = 0A$)

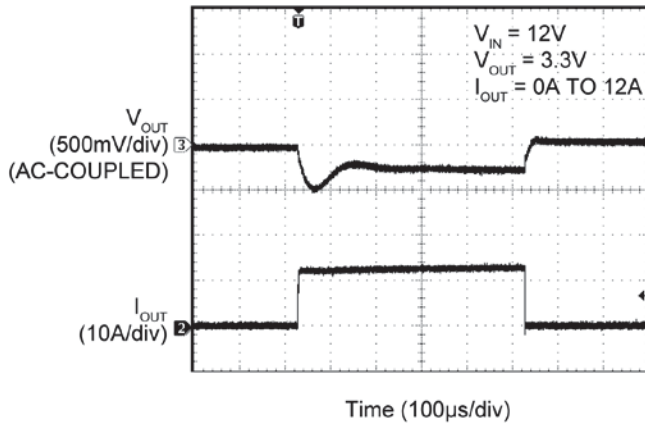


MIC2102 Transient Response

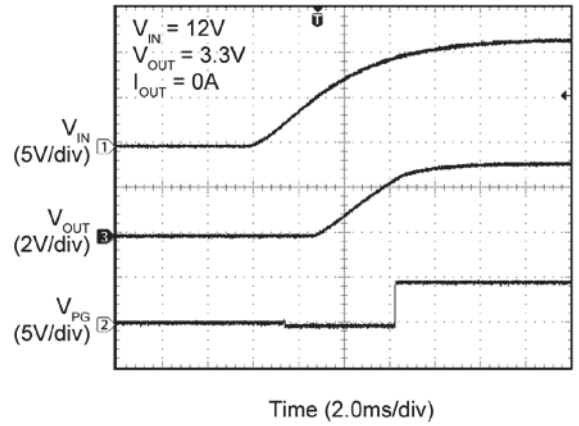


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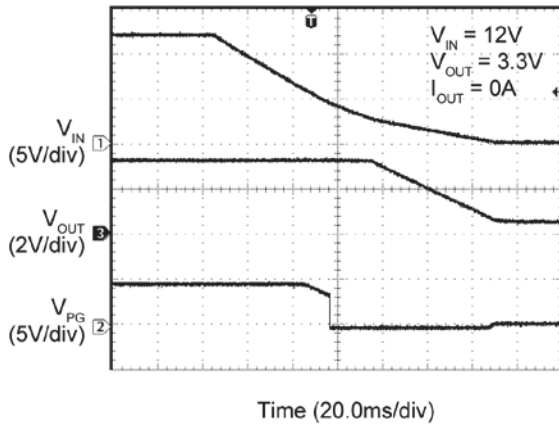
MIC2101 Transient Response



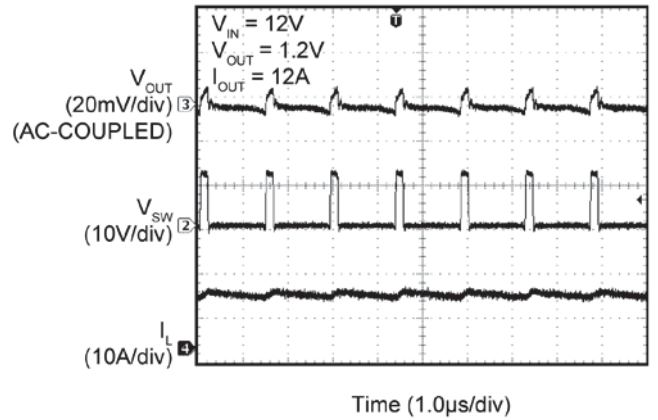
Power Good at V_{IN} Soft Turn-On



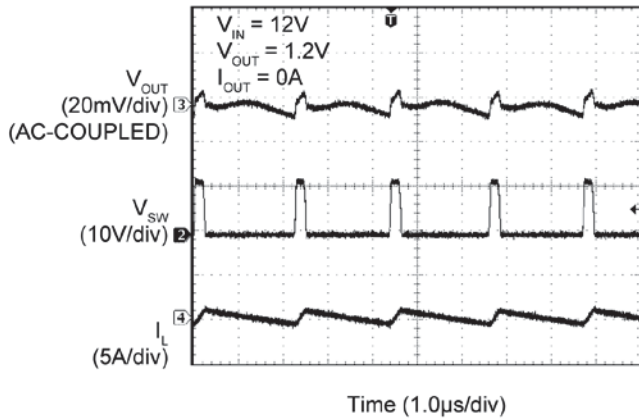
Power Good at V_{IN} Soft Turn-Off



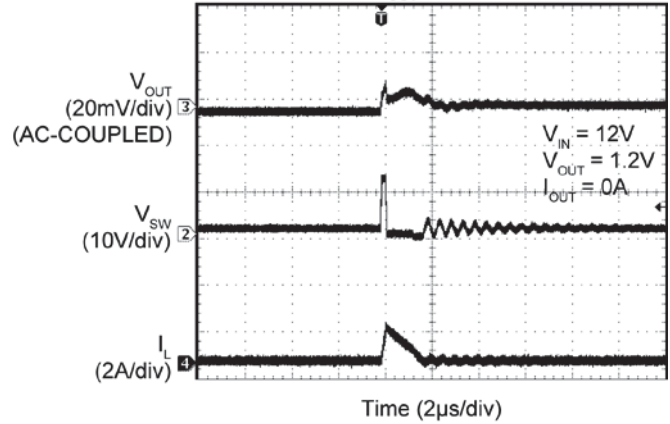
MIC2102 Switching Waveforms ($I_{OUT} = 12A$)



MIC2102 Switching Waveforms ($I_{OUT} = 0A$)

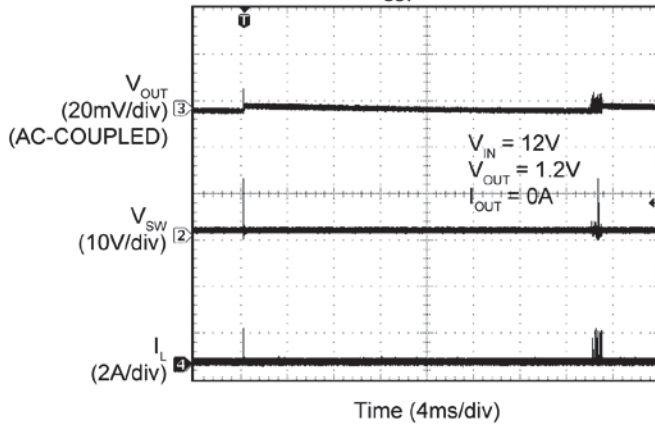


MIC2101 Switching Waveforms ($I_{OUT} = 0A$)

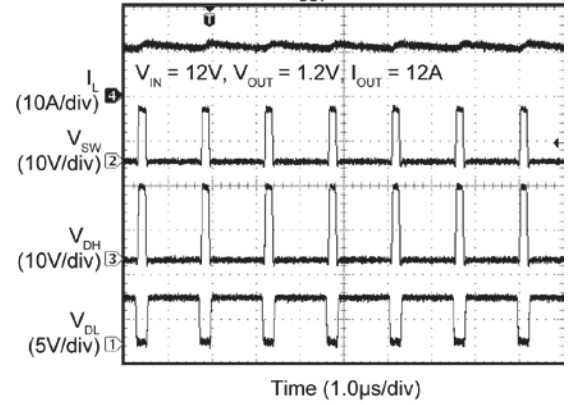


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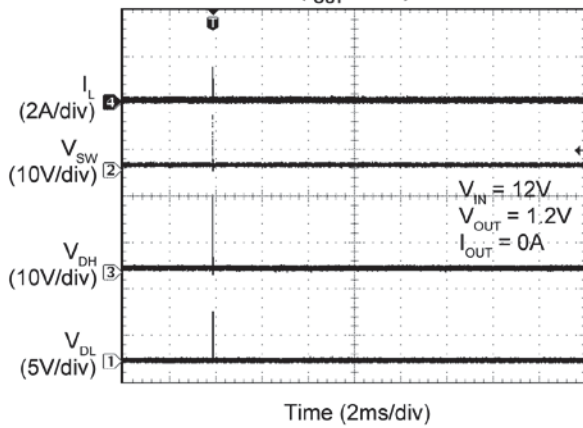
MIC2101 Switching Waveforms
($I_{OUT} = 0A$)



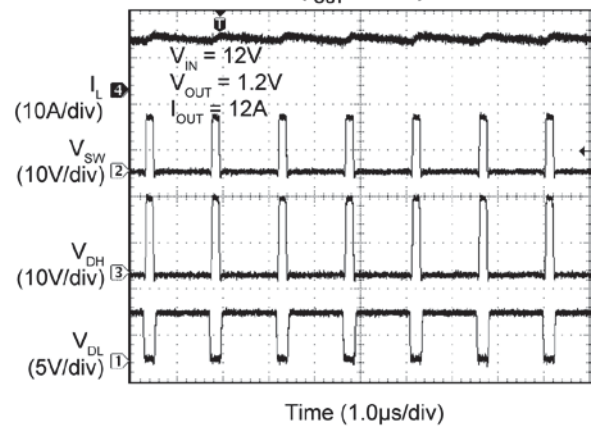
MIC2101 Switching Waveforms
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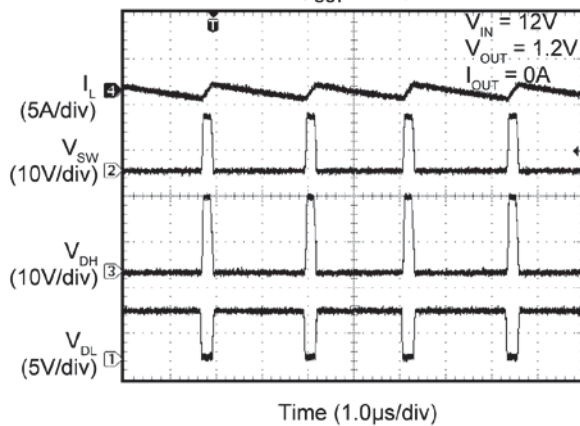
MIC2101 Switching Waveforms
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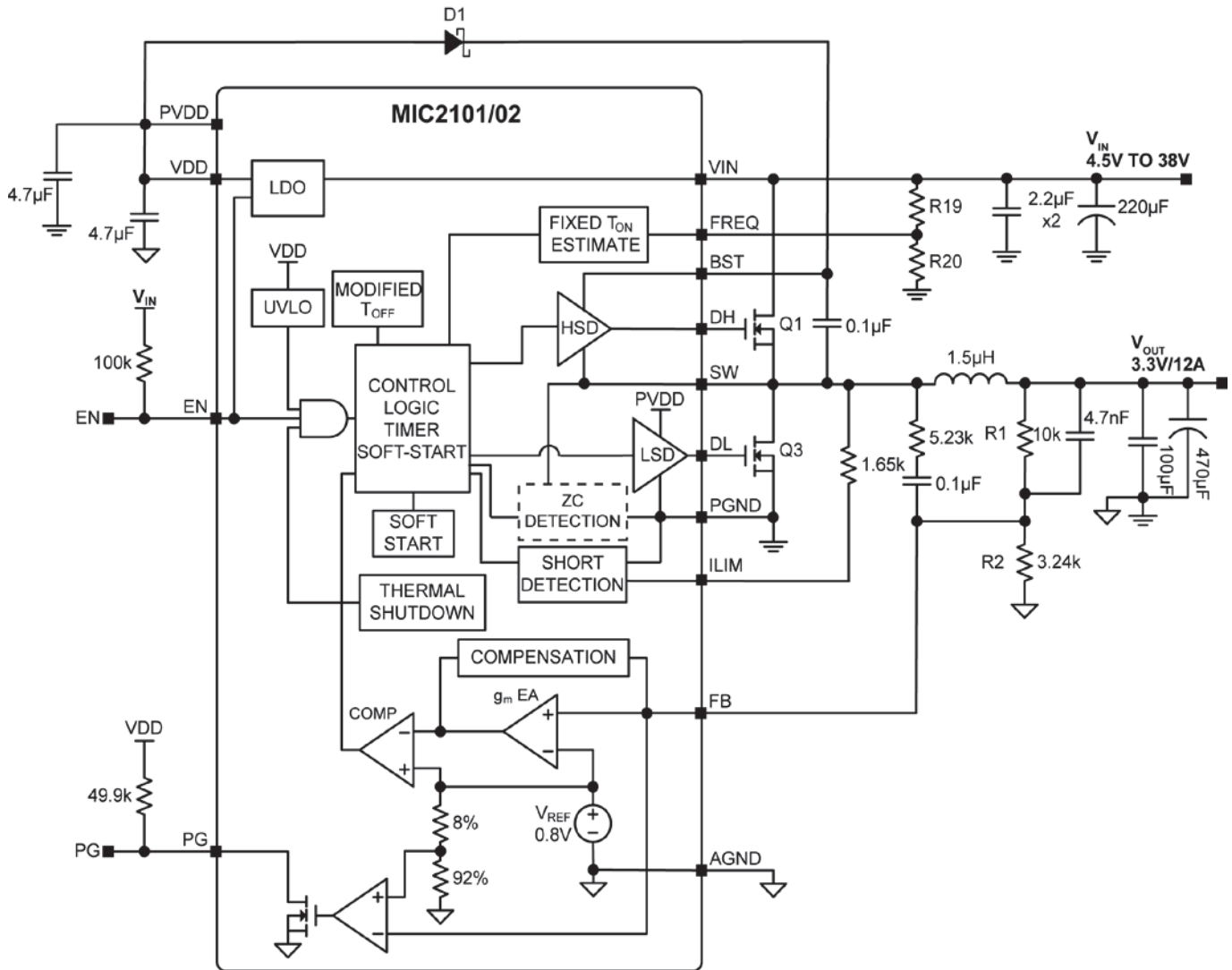
MIC2102 Switching Waveforms
($I_{OUT} = 12A$)



MIC2102 Switching Waveforms
($I_{OUT} = 0A$)



Functional Diagram



Note:
ZC Detection* – MIC2101 Only.

Figure 1. MIC2101/02 Functional Diagram

Functional Description

The MIC2101/02 are adaptive on-time synchronous buck controllers built for high-input voltage to low output voltage applications. It is designed to operate over a wide input voltage range from, 4.5V to 38V and the output is adjustable with an external resistive divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

Theory of Operation

Figure 1 illustrates the block diagram of the MIC2101/02. The output voltage is sensed by the MIC2101/02 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad \text{Eq. 1}$$

where V_{OUT} is the output voltage, V_{IN} is the power stage input voltage, and f_{SW} is the switching frequency.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 200ns, the MIC2101/02 control logic will apply the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200ns $t_{OFF(min)}$:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200ns}{t_S} \quad \text{Eq. 2}$$

where $t_S = 1/f_{SW}$. It is not recommended to use MIC2101/02 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC2101/02. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 2 shows the MIC2101/02 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF} , the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

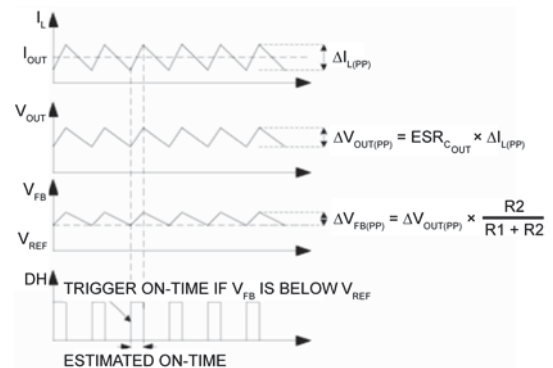


Figure 2. MIC2101/02 Control Loop Timing

Figure 3a shows the operation of the MIC2101/02 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF} . This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF} . Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2101/02 converter.

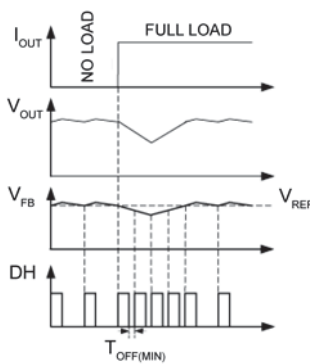


Figure 3a. MIC2101/02 Load Transient Response

Unlike true current-mode control, the MIC2101/02 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC2101/02 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV over full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to “Ripple Injection” subsection in *Application Information* for more details about the ripple injection technique.

Discontinuous Mode (MIC2101 only)

In continuous mode, the inductor current is always greater than zero; however, at light loads the MIC2101 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 3b. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC2101 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC2101 has a zero crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the $V_{FB} > 0.8V$ and the inductor current goes slightly negative, then the MIC2101 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC2101 goes into discontinuous mode, both LSD and HSD are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF} , then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 3b shows the control loop timing in discontinuous mode.

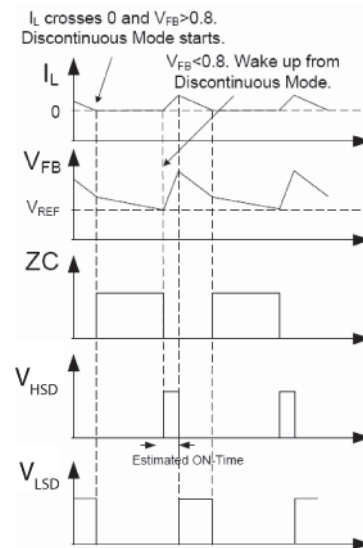


Figure 3b. MIC2101 Control Loop Timing (Discontinuous Mode)

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply

current during discontinuous mode is only about 400 μ A, allowing the MIC2101 to achieve high efficiency in light load applications.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2101/02 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC2101/02 uses the $R_{DS(ON)}$ and external resistor connected from ILIM pin to SW node to decide the current limit.

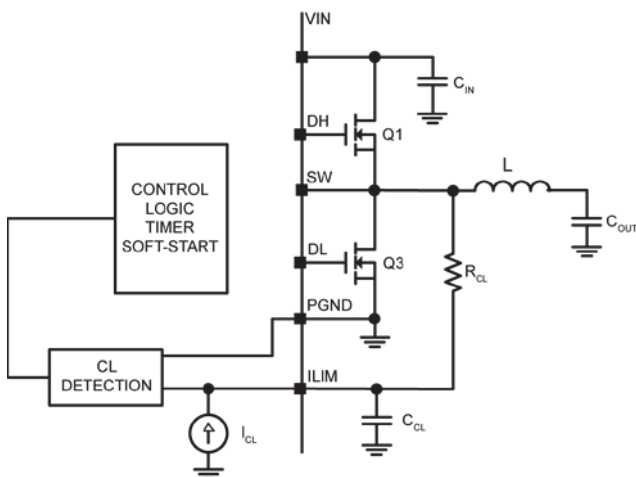


Figure 4. MIC2101/02 Current Limiting Circuit

In each switching cycle of the MIC2101/02 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage $V_{(ILIM)}$ is compared with the power ground (PGND) after a blanking time of 150ns. In this way the drop voltage over the resistor R_{CL} (V_{CL}) is compared with the drop over the bottom FET generating the short current limit.

The small capacitor (C_{CL}) connected from ILIM pin to PGND filters the switching node ringing during the off time allowing a better short limit measurement. The time constant created by R_{CL} and C_{CL} should be much less than the minimum off time.

The V_{CL} drop allows programming of short limit through the value of the resistor (R_{CL}). If the absolute value of the voltage drop on the bottom FET is greater than V_{CL} , in that case the $V_{(ILIM)}$ is lower than PGND and a short circuit event is triggered. A hiccup cycle to treat the short event is generated. The hiccup sequence including the soft start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short circuit current limit can be programmed by using the formula illustrated in Equation 3:

$$R_{CL} = \frac{(I_{CLIM} - \Delta_{PP} \times 0.5) \times R_{DS(ON)} + V_{CL}}{I_{CL}} \quad \text{Eq. 3}$$

Where I_{CLIM} = Desired current limit

Δ_{PP} = Inductor current peak-to-peak

$R_{DS(ON)}$ = On-resistance of low-side power MOSFET

V_{CL} = Current-limit threshold, the typical absolute value is 14mV in Electrical Characteristic table

I_{CL} = Current-limit source current, the typical value is 80 μ A in Electrical Characteristic table.

In case of hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft start is under the folded short limit, otherwise the supply will go in hiccup mode and may not be finishing the soft start successfully.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

MOSFET Gate Drive

The MIC2101/02 high-side drive circuit is designed to switch an N-Channel MOSFET. Figure 1 shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST} . This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN} . Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1 μ F to 1 μ F is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. $\Delta BST = 10\text{mA} \times 3.33\mu\text{s}/0.1\mu\text{F} = 333\text{mV}$. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G , which is in series with C_{BST} , can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} - V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

Setting the Switching Frequency

The MIC2101/02 are adjustable-frequency, synchronous buck controllers featuring a unique adaptive on-time control architecture. The switching frequency can be adjusted between 200kHz and 600kHz by changing the resistor divider network consisting of R19 and R20.

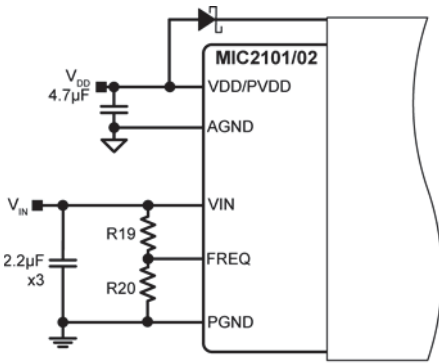


Figure 5. Switching Frequency Adjustment

The following formula gives the estimated switching frequency:

$$f_{SW_ADJ} = f_O \times \frac{R20}{R19 + R20} \quad \text{Eq. 4}$$

Where f_O = Switching Frequency when R19 is 100k and R20 being open, f_O is typically 600kHz. For more precise setting, it is recommended to use the following graph:

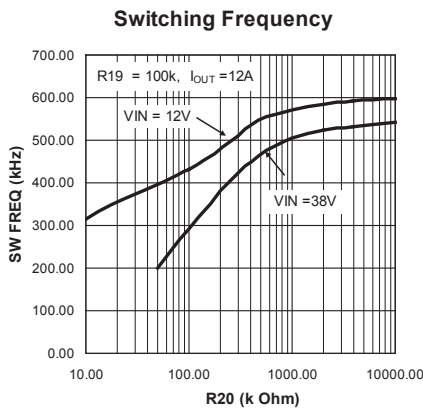


Figure 6. Switching Frequency vs. R20

MOSFET Selection

The MIC2101/02 controllers work from input voltages of

4.5V to 38V and has internal 5V V_{DD} LDO. This internal V_{DD} LDO provides power to turn the external N-Channel power MOSFETs for the high-side and low-side switches. For applications where $V_{DD} < 5V$, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when $V_{DD} > 5V$; logic-level MOSFETs, whose operation is specified at $V_{GS} = 4.5V$ must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2101/02 gate-drive circuit. At 600kHz switching frequency, the gate charge can be a significant source of power dissipation in the MIC2101/02. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[HIGH-SIDE]}(AVG) = Q_G \times f_{SW} \quad \text{Eq. 5}$$

where:

$I_{G[HIGH-SIDE]}(avg)$ = Average high-side MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{DD}$.

f_{SW} = Switching Frequency

The low-side MOSFET is turned on and off at $V_{DS} = 0$ because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at $V_{DS} = 0$ instead of gate charge.

For the low-side MOSFET:

$$I_{G[\text{LOW-SIDE}]}(\text{AVG}) = C_{\text{ISS}} \times V_{\text{GS}} \times f_{\text{SW}} \quad \text{Eq. 6}$$

Since the current from the gate drive comes from the V_{DD} , the power dissipated in the MIC2101/02 due to gate drive is:

$$P_{\text{GATEDRIVE}} = V_{\text{DD}} \times (I_{G[\text{HIGH-SIDE}]}(\text{AVG}) + I_{G[\text{LOW-SIDE}]}(\text{AVG})) \quad \text{Eq. 7}$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{\text{DS(ON)}} \times Q_{\text{G}}$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2101/02. Also, the $R_{\text{DS(ON)}}$ of the low-side MOSFET will determine the current-limit value. Please refer to “Current Limit” subsection in *Functional Description* for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD} . A safety factor of 20% should be added to the $V_{\text{DS(MAX)}}$ of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{\text{CONDUCTION}}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{\text{SW}} = P_{\text{CONDUCTION}} + P_{\text{AC}} \quad \text{Eq. 8}$$

$$P_{\text{CONDUCTION}} = I_{\text{SW(RMS)}}^2 \times R_{\text{DS(ON)}} \quad \text{Eq. 9}$$

$$P_{\text{AC}} = P_{\text{AC(off)}} + P_{\text{AC(on)}} \quad \text{Eq. 10}$$

where:

$R_{\text{DS(ON)}}$ = On-resistance of the MOSFET switch

D = Duty Cycle = $V_{\text{OUT}} / V_{\text{HSD}}$

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_{\text{T}} = \frac{C_{\text{ISS}} \times V_{\text{IN}} + C_{\text{OSS}} \times V_{\text{HSD}}}{I_{\text{G}}} \quad \text{Eq. 11}$$

where:

C_{ISS} and C_{OSS} are measured at $V_{\text{DS}} = 0$

I_{G} = Gate-drive current

The total high-side MOSFET switching loss is:

$$P_{\text{AC}} = (V_{\text{HSD}} + V_{\text{D}}) \times I_{\text{PK}} \times t_{\text{T}} \times f_{\text{SW}} \quad \text{Eq. 12}$$

where:

t_{T} = Switching transition time

V_{D} = Body diode drop (0.5V)

f_{SW} = Switching Frequency

The high-side MOSFET switching losses increase with the switching frequency and the input voltage V_{HSD} . The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.