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MIC2164/-2/-3/C

Synchronous Buck Controllers featuring Adaptive On-Time Control 28V Input, Constant Frequency

Hyper Speed Control™ Family

General Description

The Micrel MIC2164/-2/-3/C are constant-frequency, synchronous buck controllers featuring adaptive on-time control. The MIC2164/-2/-3/C are the first products in the new Hyper Speed Control™ family of buck controllers introduced by Micrel.

The MIC2164/-2/-3/C controllers operate over an input supply range of 3V to 28V, and are independent of the IC supply voltage. The devices are capable of supplying 25A output current. While the MIC2164 operates at 300kHz, the MIC2164-2 operates at 600kHz, and the MIC2164-3 operates at 1MHz.

A unique Hyper Speed Control architecture allows for ultra-fast transient response while reducing the output capacitance and also makes High VIN/Low VOUT operation possible. The MIC2164/-2/-3/C controllers utilizes an architecture which is adaptive TON ripple controlled. A UVLO feature is provided to ensure proper operation under power-sag conditions to prevent the external power MOSFET from overheating. A soft start feature is provided to reduce the inrush current. Foldback current limit and "hiccup" mode short-circuit protection ensure FET and load protection.

The MIC2164/-2/-3/C controllers are available in a 10-pin MSOP (MAX1954A-compatible) package with a junction operating range from –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Hyper Speed Control™

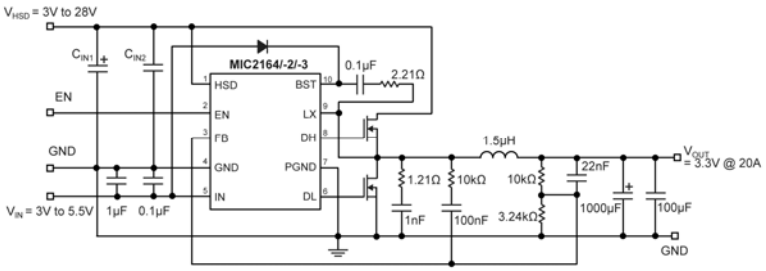
Features

- Hyper Speed Control architecture enables high delta V operation (V_{HSD} = 28V and V_{OUT} = 0.8V) and smaller output capacitors than competitors
- 3V to 28V input voltage
- Any Capacitor™ stable (Zero ESR to high ESR)
- 25A output current capability
- 300kHz/600kHz/1MHz switching frequency
- Adaptive on-time mode control
- Adjustable output from 0.8V to 5.5V with ±1% (MIC2164/-2/-3) or ±3% (MIC2164C) FB accuracy
- Up to 95% efficiency
- Foldback current-limit, "hiccup" mode short-circuit protection, thermal shutdown, and safe pre-bias startup
- 6ms Internal soft start
- –40°C to +125°C junction temperature range
- Available in 10-pin MSOP package

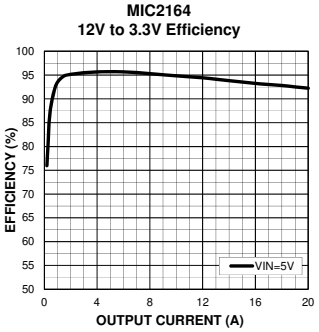
Applications

- Set-top box, gateways and routers
- Printers, scanners, graphic cards and video cards
- Telecommunication, PCs and servers

Typical Application



MIC2164/-2/-3/C Synchronous Controllers Featuring Adaptive On-Time Control



Hyper Speed Control and Any Capacitor are trademarks of Micrel, Inc.

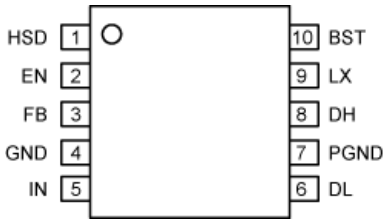
Ordering Information

Part Number	Voltage[1]	Switching Frequency	Accuracy	Junction Temperature Range	Package	Lead Finish
MIC2164YMM	Adjustable	300kHz	±1%	–40° to +125°C	10-pin MSOP	Pb-Free
MIC2164-2YMM	Adjustable	600kHz	±1%	–40° to +125°C	10-pin MSOP	Pb-Free
MIC2164-3YMM	Adjustable	1MHz	±1%	–40° to +125°C	10-pin MSOP	Pb-Free
MIC2164CYMM	Adjustable	270kHz	±3%	–40° to +125°C	10-pin MSOP	Pb-Free

Note:

1. Other voltages are available. Contact Micrel for details.

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	HSD	High-Side N-MOSFET Drain Connection (input): Power to the drain of the external high-side N-channel MOSFET. The HSD operating voltage range is from 3V to 28V. Input capacitors between HSD and the power ground (PGND) are required.
2	EN	Enable (input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high or floating = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 0.8mA).
3	FB	Feedback (input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
4	GND	Signal ground. GND is the ground path for the device input voltage VIN and the control circuitry. The loop for the signal ground should be separate from the power ground (PGND) loop.
5	IN	Input Voltage (input): Power to the internal reference and control sections of the MIC2164/-2/-3. The IN operating voltage range is from 3V to 5.5V. A 1µF and 0.1µF ceramic capacitors from IN to GND are recommended for clean operation.
6	DL	Low-Side Drive (output): High-current driver output for external low-side MOSFET. The DL driving voltage swings from ground-to-IN.
7	PGND	Power Ground. PGND is the ground path for the MIC2164/-2/-3 buck converter power stage. The PGND pin connects to the sources of low-side N-Channel MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (GND) loop.
8	DH	High-Side Drive (output): High-current driver output for external high-side MOSFET. The DH driving voltage is floating on the switch node voltage (LX). It swings from ground to VIN minus the diode drop. Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFETs can slow down the turn-on and turn-off time of the MOSFETs.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
9	LX	Switch Node and Current Sense input: High current output driver return. The LX pin connects directly to the switch node. Due to the high speed switching on this pin, the LX pin should be routed away from sensitive nodes. LX pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to LX using a Kelvin connection.
10	BST	Boost (output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the IN pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the LX pin. Adding a small resistor in series with the boost capacitor can slow down the turn-on time of high-side N-Channel MOSFETs.

Absolute Maximum Ratings[2]

IN, FB, EN to GND ..... –0.3V to +6V
BST to LX ..... –0.3V to +6V
BST to GND ..... –0.3V to +37V
DH to LX ..... –0.3V to (V_{BST} + 0.3V)
DL, COMP to GND ..... –0.3V to (V_{IN} + 0.3V)
HSD to GND ..... –0.3V to 31V
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C

Operating Ratings[3]

Input Voltage (V_{IN}) ..... 3.0V to 5.5V
Supply Voltage (V_{HSD}) ..... 3.0V to 28V
Operating Temperature Range ..... –40°C to +125°C
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
MSOP (θ_{JA}) ..... 130.5°C/W
Continuous Power Dissipation (T_A = 70°C) 421mW
(derate 5.6mW/°C above 70°C)

Electrical Characteristics[5]

$V_{BST} – V_{LX}$ = 5V; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +125°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
General					
Operating Input Voltage (V_{IN})[6]		**3.0**		**5.5**	V
HSD Voltage Range (V_{HSD})		**3.0**		**28**	V
Quiescent Supply Current	(V_{FB} = 1.5V, output switching but excluding external MOSFET gate current)		1.4	**3.0**	mA
Standby Supply Current[7]	V_{IN} = V_{BST} = 5.5V, V_{HSD} = 28, LX = unconnected, EN = GND		0.8	**2**	mA
Under-Voltage Lockout Trip Level		**2.4**	2.7	**3**	V
UVLO Hysteresis			50		mV
DC-DC Controller					
Output-Voltage Adjust Range (V_{OUT})		**0.8**		**5.5**	V
Error Amplifier					
FB Regulation Voltage	0°C ≤ T_J ≤ 85°C	**-1**		**1**	%
	–40°C ≤ T_J ≤ 125°C	**-2**		**2**	
	T_J = 25°C (MIC2164C)	-3		3	
FB Input Leakage Current			5	**500**	nA
Current-Limit Threshold	V_{FB} = 0.8V	**103**	130	**162**	mV
	V_{FB} = 0V	**19**	48	**77**	
	V_{FB} = 0.8V (MIC2164C)	**95**	130	**170**	
	V_{FB} = 0V (MIC2164C)	**15**	48	**80**	

Notes:

2. Exceeding the absolute maximum ratings may damage the device.
3. The device is not guaranteed to function outside its operating ratings.
4. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.
6. The application is fully functional at low IN (supply of the control section) if the external MOSFETs have enough low voltage V_{TH}.
7. The current will come only from the internal 100kΩ pull-up resistor sitting on the EN Input and tied to IN.
8. Measured in test mode.
9. Measured at DH. The maximum duty cycle is limited by the fixed mandatory off time T_{OFF} of 363ns typical.

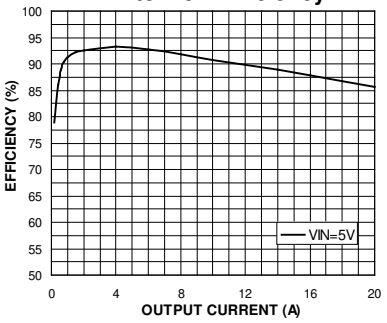
Electrical Characteristics[5] (Continued)

$V_{BST} - V_{LX}$ = 5V; T_A = 25°C, **bold** values indicate –40°C≤ T_A ≤ +125°C, unless noted.

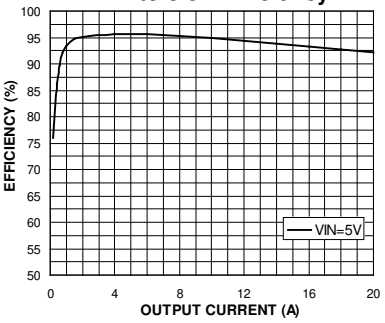
Parameter	Condition	Min.	Typ.	Max.	Units
Soft-Start					
Soft-Start Period			6		ms
Oscillator					
Switching Frequency[8]	MIC2164C MIC2164 MIC2164-2 MIC2164-3	**0.202** **0.225** **0.45** **0.75**	0.27 0.3 0.6 1	**0.338** **0.375** **0.75** **1.25**	MHz
Maximum Duty Cycle[9]	MIC2164/ MIC2164C MIC2164-2 MIC2164-3		87 74 66		%
Minimum Duty Cycle	Measured at DH, V_{FB} = 1V		0		%
FET Drives					
DH, DL Output Low Voltage	I_{SINK} = 10mA			**0.1**	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA	V_{IN} – 0.1V or V_{BST} – 0.1V			V
DH On-Resistance, High State			2.1	**3.3**	Ω
DH On-Resistance, Low State			1.8	**3.3**	Ω
DL On-Resistance, High State			1.8	**3.3**	Ω
DL On-Resistance, Low State			1.2	**2.3**	Ω
LX Leakage Current	V_{LX} = 28V, V_{IN} = 5.5V,V_{BST} = 33.5V			**50**	µA
HSD Leakage Current	V_{LX} = 28V, V_{IN} = 5.5V,V_{BST} = 33.5V			**20**	µA
Thermal Protection					
Over-Temperature Shutdown			155		°C
Over-Temperature Shutdown Hysteresis			10		°C
Shutdown Control					
EN Logic Level Low	3V < V_{IN} <5.5V	**0.4**	0.8		V
EN Logic Level High	3V < V_{IN} <5.5V		0.9	**1.2**	V
EN Pull-Up Current			50		µA

Typical Characteristics

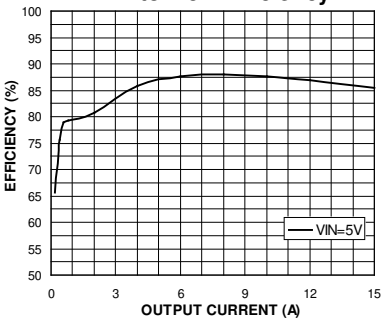
MIC2164
12V to 1.5V Efficiency



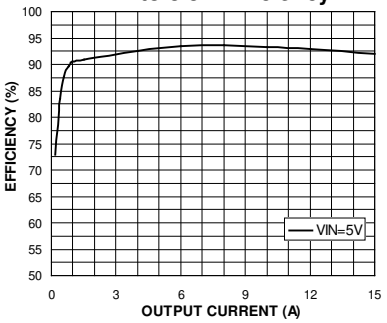
MIC2164
12V to 3.3V Efficiency



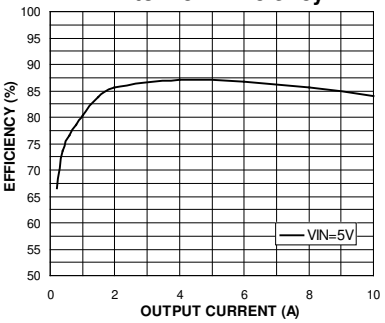
MIC2164-2
12V to 1.5V Efficiency



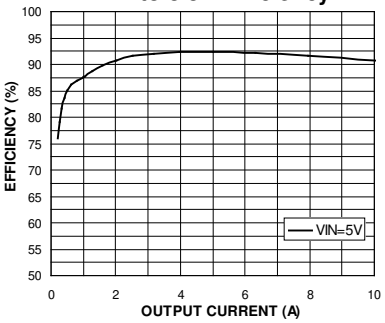
MIC2164-2
12V to 3.3V Efficiency



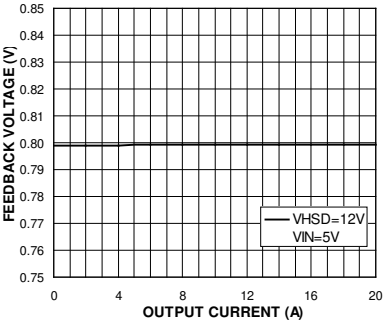
MIC2164-3
12V to 1.5V Efficiency



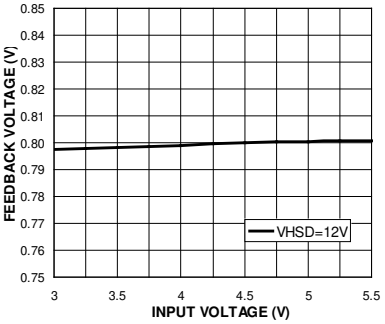
MIC2164-3
12V to 3.3V Efficiency



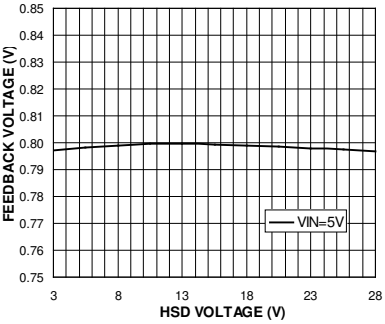
Feedback Voltage vs. Load



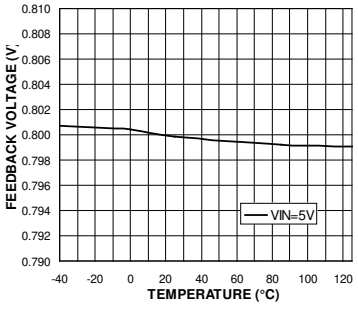
Feedback Voltage
vs. Input Voltage



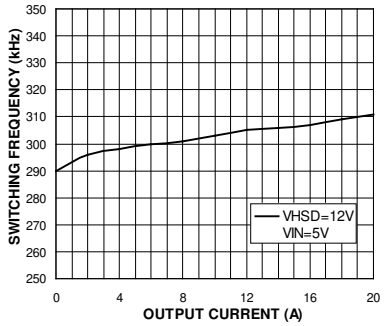
Feedback Voltage
vs. HSD Voltage



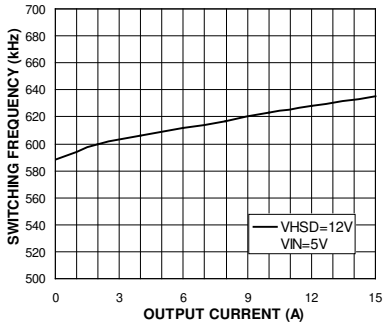
Feedback Voltage
vs. Temperature



MIC2164
Switching Frequency vs. Load

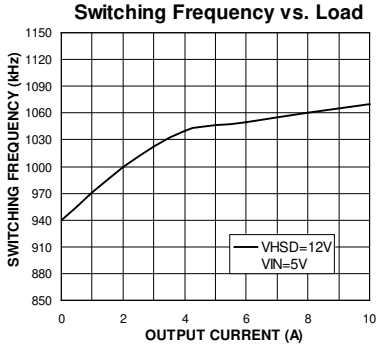


MIC2164-2
Switching Frequency vs. Load

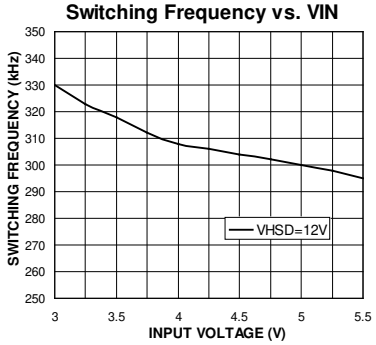


Typical Characteristics (Continued)

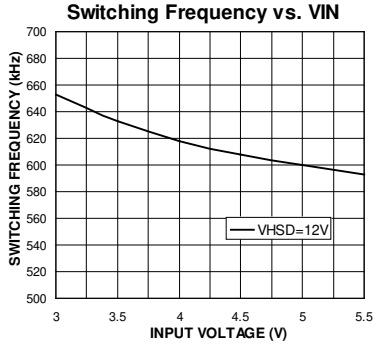
MIC2164-3 Switching Frequency vs. Load



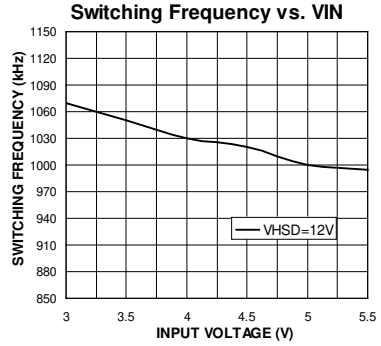
MIC2164 Switching Frequency vs. VIN



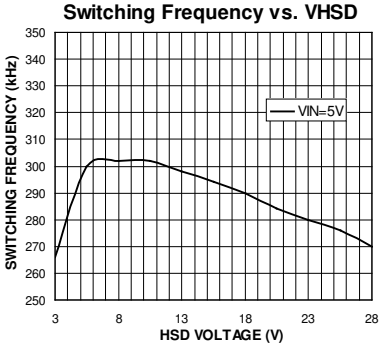
MIC2164-2 Switching Frequency vs. VIN



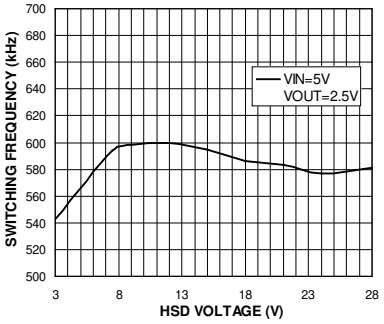
MIC2164-3 Switching Frequency vs. VIN



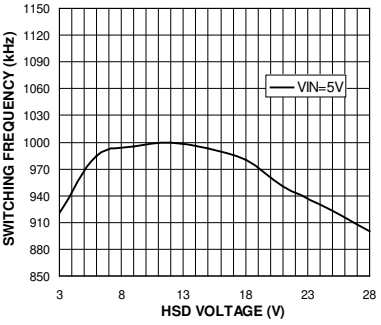
MIC2164 Switching Frequency vs. VHSD



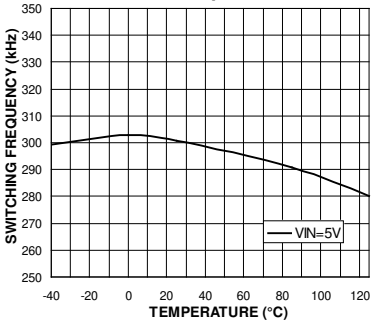
MIC2164-2 Switching Frequency vs. VHSD



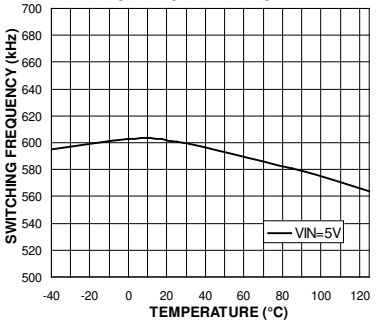
MIC2164-3 Switching Frequency vs. VHSD



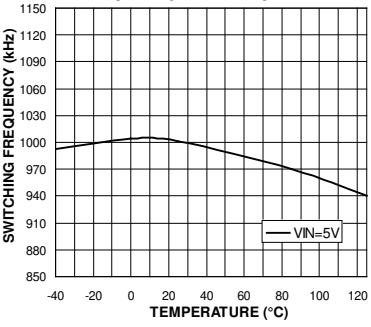
MIC2164 Switching Frequency vs. Temperature



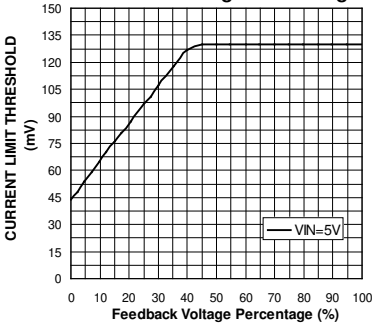
MIC2164-2 Switching Frequency vs. Temperature



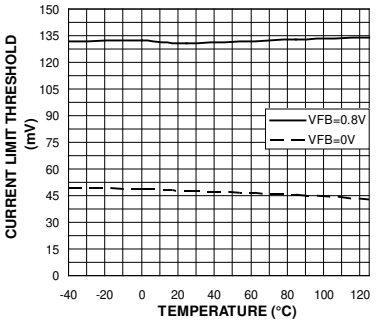
MIC2164-3 Switching Frequency vs. Temperature



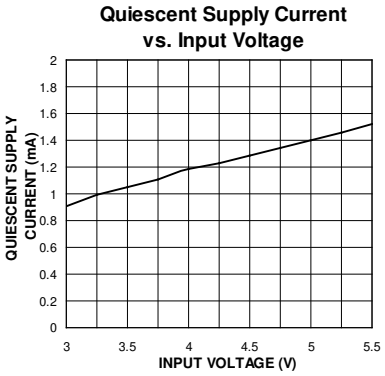
Current Limit Threshold vs. Feedback Voltage Percentage



Current Limit Threshold vs. Temperature

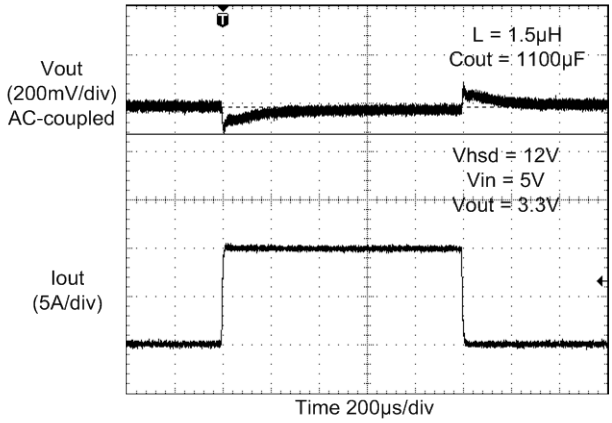


Typical Characteristics (Continued)

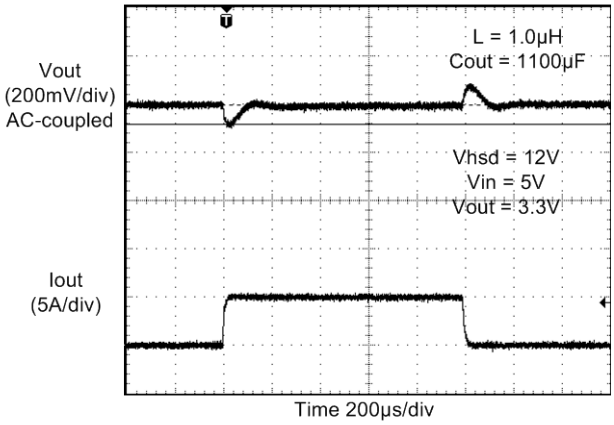


Functional Characteristics

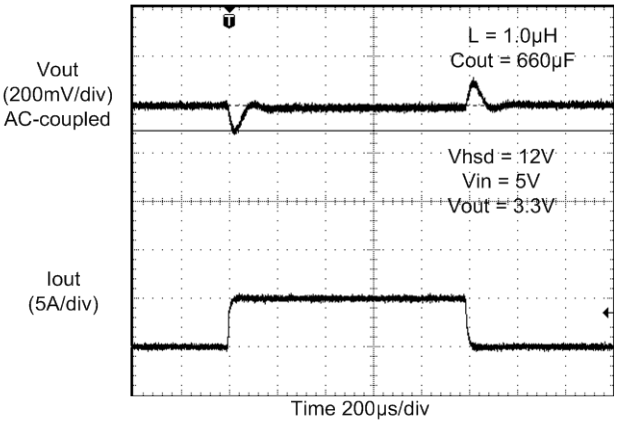
MIC2164 Load Transient



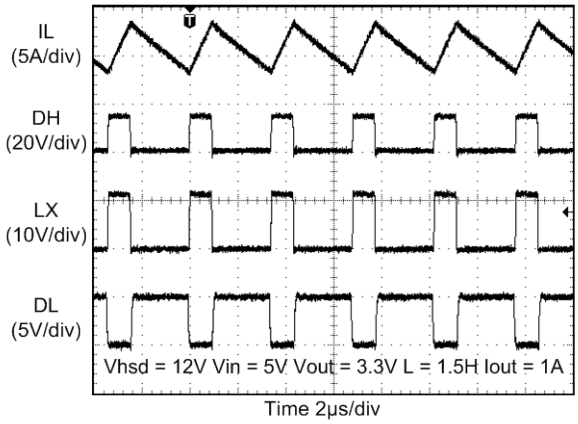
MIC2164-2 Load Transient



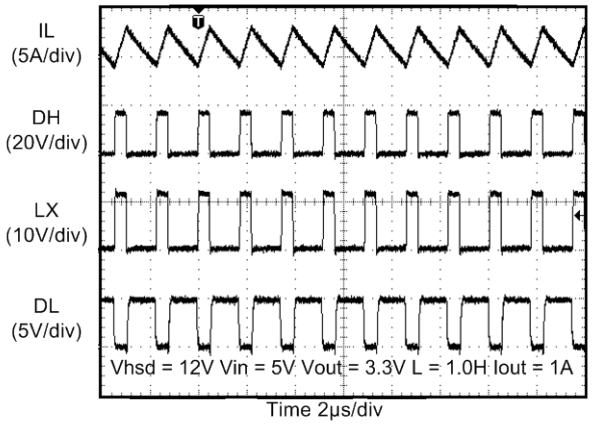
MIC2164-3 Load Transient



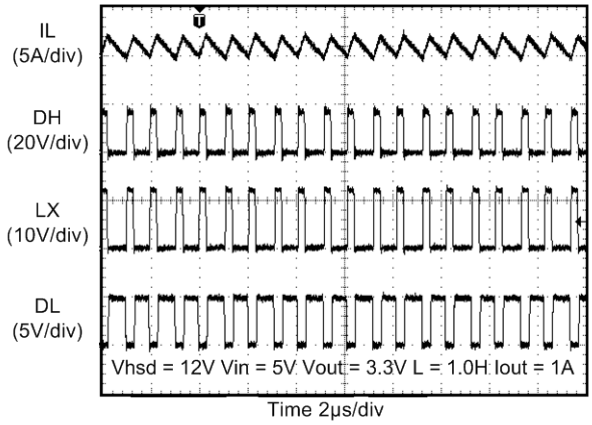
MIC2164 Switching Waveforms (Light Load)



MIC2164-2 Switching Waveforms (Light Load)

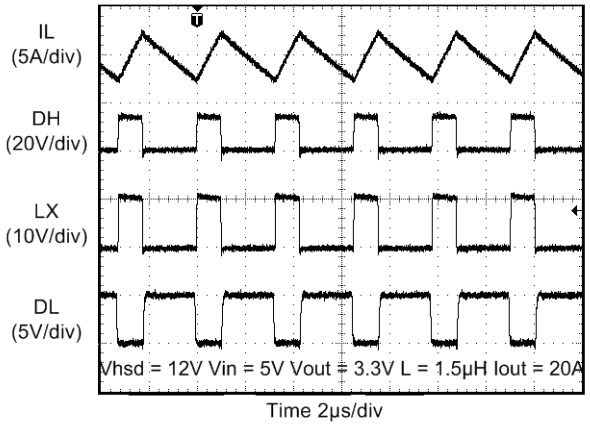


MIC2164-3 Switching Waveforms (Light Load)

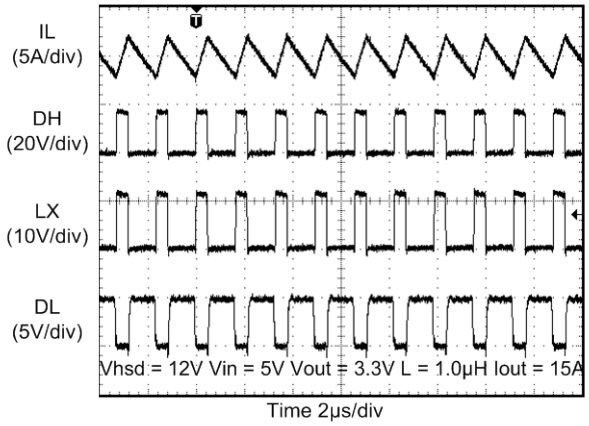


Functional Diagram (Continued)

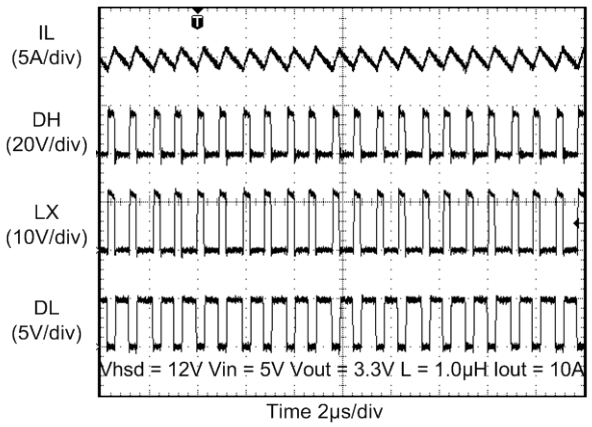
MIC2164 Switching Waveforms (Heavy Load)



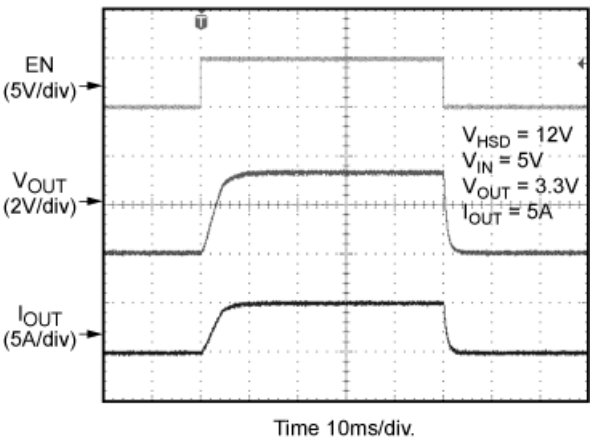
MIC2164-2 Switching Waveforms (Heavy Load)



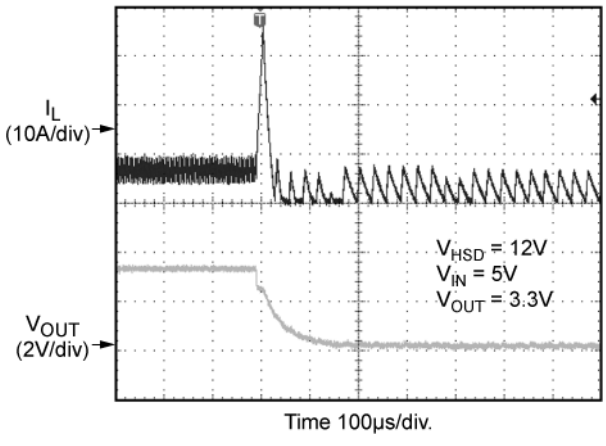
MIC2164-3 Switching Waveforms (Heavy Load)



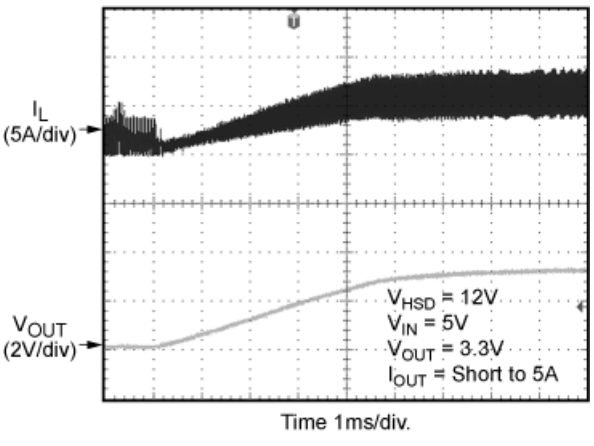
Power-Up/Power-Down



Short Circuit

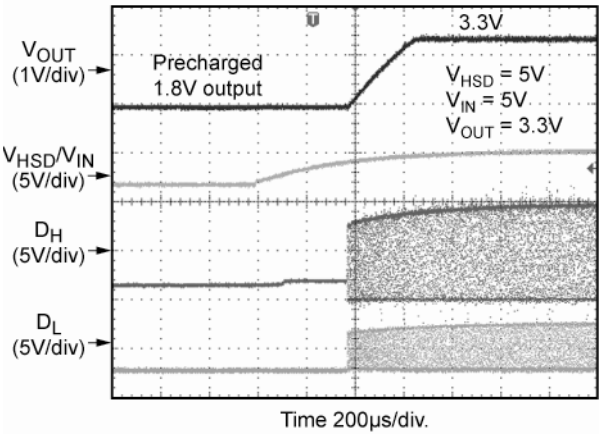


Short Circuit Recovery

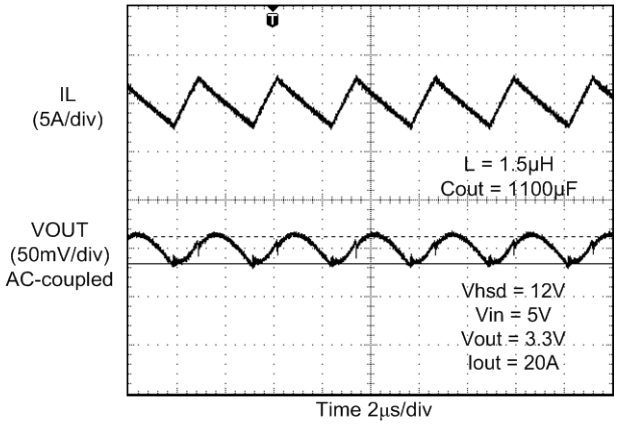


Functional Characteristics (Continued)

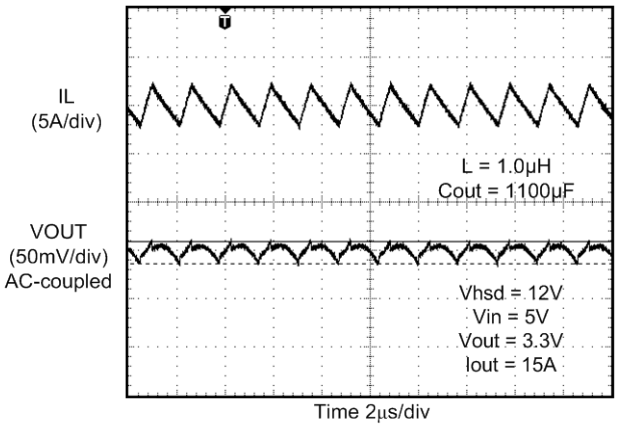
Start-Up with Prebias V_{OUT}



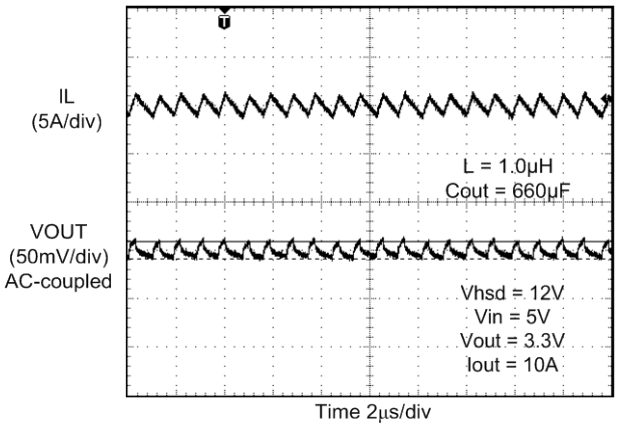
MIC2164 Output Voltage Ripple



MIC2164-2 Output Voltage Ripple



MIC2164-3 Output Voltage Ripple



Functional Diagram

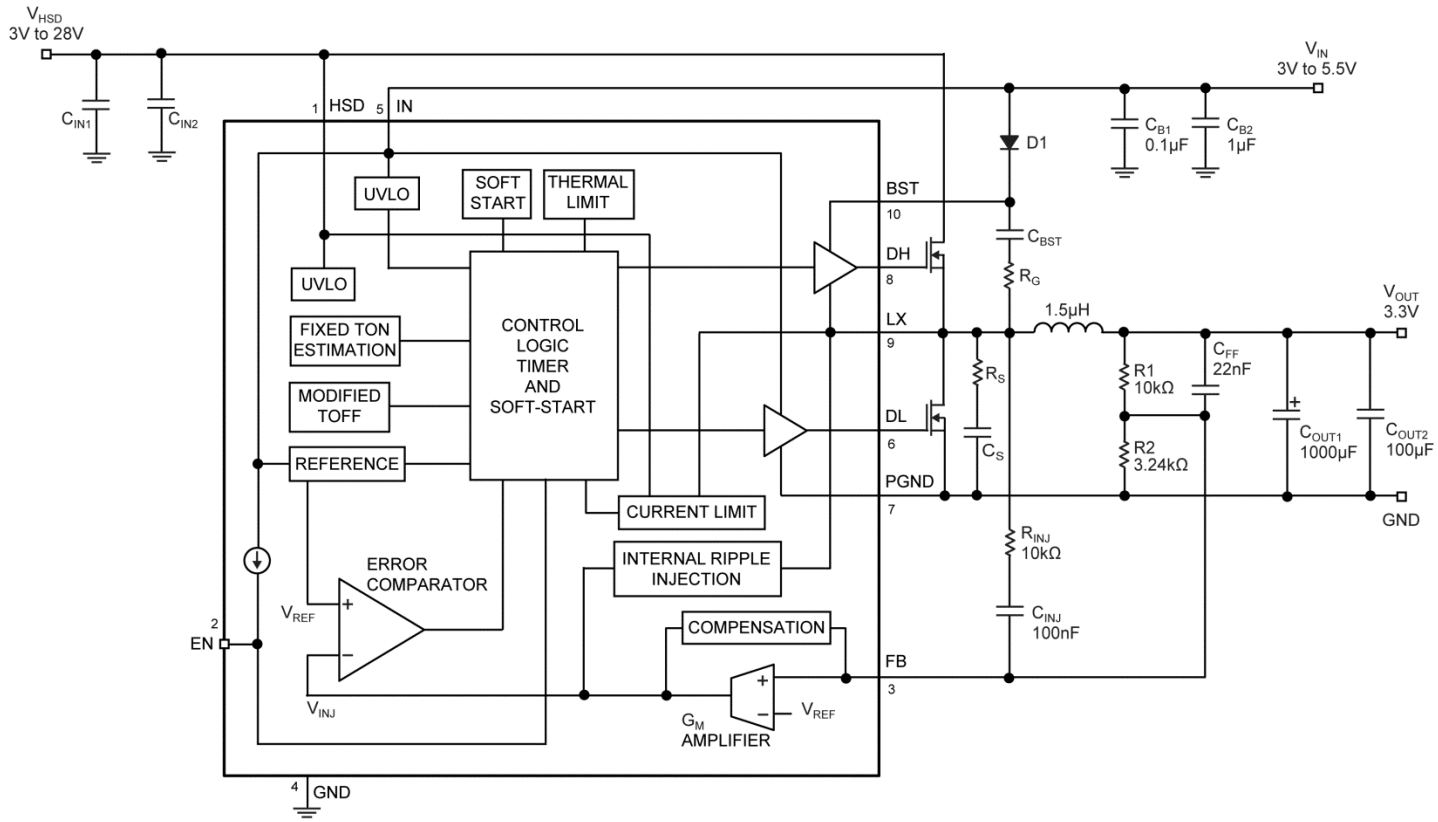


Figure 1. MIC2164/-2/-3 Block Diagram

Functional Description

The MIC2164/-2/-3 are parts of an adaptive on-time synchronous buck controller family built for low cost and high performance. They are designed for a wide input voltage range, from 3V to 28V, and high output power buck converters. An estimated-ON-time method is applied to the MIC2164/-2/-3 to obtain a constant switching frequency and to simplify the control compensation. The over-current protection is implemented without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

Figure 1 illustrates the block diagram for the control loop. The output voltage variation will be sensed by the MIC2164/-2/-3 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage VREF at the error comparator through a low gain transconductance (g_m) amplifier, the amplifier improves the MIC2164/-2/-3 converter output voltage regulation. If the FB voltage decreases and the output of the gm amplifier is below 0.8V, The error comparator will trigger the control logic and generate an ON-time period, in which DH pin is logic high and DL pin is logic low. The ON-time period length is predetermined by the "FIXED TON ESTIMATION" circuitry:

$$T_{ON(estimated)} = \frac{V_{OUT}}{V_{HSD} \times f_{sw}} \qquad \textbf{Eq. 1}$$

where V_{OUT} is the output voltage, V_{HSD} is the power stage input voltage, and f_{SW} is the switching frequency (300kHz for MIC2164, 600kHz for MIC2164-2, and 1MHz for MIC2164-3).

When the MIC2164/-2/-3 enters the OFF-time period, the DH pin becomes logic low and the DL pin is logic high. In most cases, the OFF-time period length is dependent on the FB voltage. When the FB voltage decreases and the output voltage of the g_m amplifier drops below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period, determined by the FB voltage, is less than the minimum OFF time ($T_{OFF(min)}$), which is about 363ns typical, then the MIC2164/-2/-3 control logic will apply the $T_{OFF(min)}$ instead. $T_{OFF(min)}$ is required by the BST charging.

The maximum duty cycle is obtained from the 363ns $T_{OFF(min)}$:

$$Dmax = \frac{T_S - T_{OFF(min)}}{T_S} = 1 - \frac{363ns}{T_S} \qquad \textbf{Eq.2}$$

where $T_S = 1/f_{SW}$.

It is not recommended to use MIC2164/-2/-3 with an OFF time close to $T_{OFF(min)}$ at the steady state. Also, as V_{OUT} increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC2164/-2/-3 should be limited to 5.5V. If a higher output voltage is required, use the MIC2176 instead. Please refer to "Setting Output Voltage" subsection in *Application Information* for more details.

The estimated-ON-time method results in a constant switching frequency in MIC2164/-2/-3. The actual ON time is varied with the different rising and falling time of the external MOSFETs. Therefore, the type of the external MOSFETs, the output load current, and the control circuitry power supply V_{IN} will modify the actual ON time and the switching frequency. Also, the minimum T_{ON} results in a lower switching frequency in the high V_{HSD} and low V_{OUT} applications, such as 24V to 1.0V MIC2164-3 application. The minimum T_{ON} measured on the MIC2164 evaluation board is about 138ns. During the load transient, the switching frequency is changed due to the varying OFF time.

To illustrate the control loop, the steady-state scenario and the load transient scenario are analyzed. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the FB voltage. Figure 2 shows the MIC2164/-2/-3 control loop timing during the steady-state. During the steady-state, the g_m amplifier senses the FB voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON time is predetermined by the estimation. The ending of OFF time is controlled by the FB voltage. At the valley of the FB voltage ripple, which is below than V_{REF}, OFF period ends and the next ON-time period is triggered through the control logic circuitry.

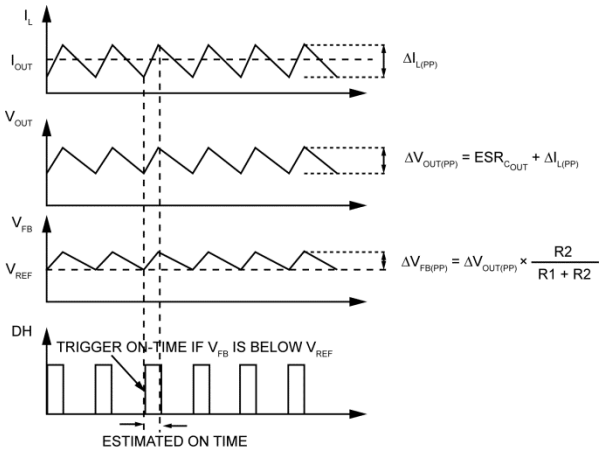


Figure 2. MIC2164/-2/-3 Control Loop Timing

Figure 3 shows the load transient scenario of the MIC2164/-2/-3 converter. The output voltage will drop due to a sudden load increase, which causes the FB voltage to be less than V_{REF}. This will cause the error comparator to the trigger ON-time period. At the end of the ON-time period a minimum OFF time, $T_{OFF(min)}$, is generated to charge the BST since the FB voltage is still below the V_{REF}. The next ON-time period is triggered due to the low FB voltage. The switching frequency changes during the load transient. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC2164/-2/-3 converter.

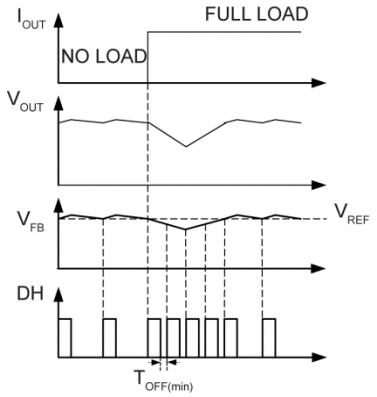


Figure 3. MIC2164/-2/-3 Load-Transient Response

Unlike the current-mode control, MIC2164/-2/-3 uses the output voltage ripple, which is proportional to the inductor current ripple if the ESR of the output capacitor is large enough, to trigger an ON-time period. The predetermined ON time makes the MIC2164/-2/-3 control loop have an advantage as the adaptive on-time mode control. The slope compensation, which is necessary for the current-mode control, is not required in the MIC2164/-2/-3 family.

The MIC2164/-2/-3 family has its own stability concern. the FB voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the gm amplifier and the error comparator. The recommended minimum FB voltage ripple is 20mV. If a low ESR output capacitor is selected, then the FB voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the FB voltage ripple are not in phase with the inductor current ripple if the ESR of the output capacitor is very low. Therefore, the ripple injection is required for a low ESR output capacitor. Please refer to “Ripple Injection” subsection in “Application Information” for more details about the ripple injection.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

MIC2164/-2/-3 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6ms with a 9.7mV step. The output voltage is controlled to increase slowly by a stair-case V_{REF} ramp. Once the soft-start ends, the related circuitry is disabled to reduce the current consumption. To make the soft-start function behavior correctly, the V_{IN} should not be powered up before V_{HSD}.

Current Limit

The MIC2164/-2/-3 uses the $R_{DS(ON)}$ of the low-side power MOSFET to sense over-current conditions. The lower-side MOSFET is used because it displays much lower parasitic oscillations during switching then the high-side MOSFET. Using the low-side MOSFET $R_{DS(ON)}$ as a current sense is an excellent method for circuit protection. This method will avoid adding cost, board space and power losses taken by discrete current sense resistors.

In each switching cycle of the MIC2164/-2/-3 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage is compared with a current-limit threshold voltage V_{CL} after a blanking time of 150ns. If the sensed voltage is over V_{CL}, which is 130mV typical at 0.8V feedback voltage, the MIC2164/-2/-3 turns off the high-side MOSFET and a soft-start sequence is trigged. This mode of operation is called the “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The current limit threshold V_{CL} has a fold back characteristics related to the FB voltage. Please refer to the *Typical Characteristics* for the curve of V_{CL} vs. FB voltage. The circuit in Figure 4 illustrates the MIC2164/-2/-3 current limiting circuit.

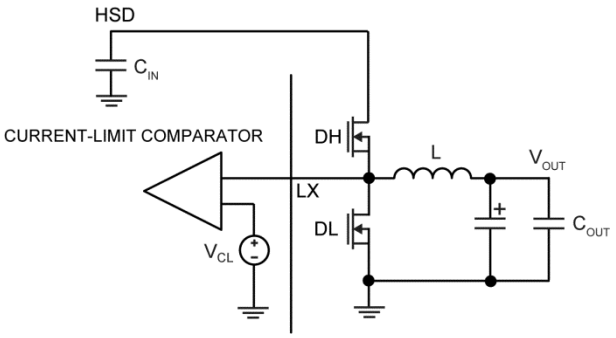


Figure 4 MIC2164/-2/-3 Current Limiting Circuit

Using the typical V_{CL} value of 130mV, the current limit value is roughly estimated as:

$$I_{CL} \approx \frac{130mV}{R_{DS(ON)}} \quad \textbf{Eq. 3}$$

For designs where the current ripple is significant compared to the load current (I_{OUT}), or for low duty cycle operation, calculating the current limit (I_{CL}) should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 150ns.

$$I_{CL} = \frac{130mV}{R_{DS(ON)}} + \frac{V_{OUT} * T_{DLY}}{L} - \frac{\Delta I_{L(pp)}}{2} \quad \textbf{Eq. 4}$$

$$\Delta I_{L(pp)} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \textbf{Eq. 5}$$

where

V_{OUT} = The output voltage

T_{DLY} = Current limit blanking time, 150ns typical

$\Delta_{IL(pp)}$ = Inductor current ripple peak-to-peak value

D = Duty Cycle

f_{SW} = Switching frequency

The MOSFET $R_{DS(ON)}$ varies 30 to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect LX pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

MOSFET Gate Drive

The MIC2164/-2/-3 high-side drive circuit is designed to switch an N-Channel MOSFET. Figure 1 shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. The C_{BST} capacitor is charged while the low-side MOSFET is on and the voltage on the LX pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the LX pin increases to approximately V_{HSD}. Diode D1 is reversed biased and the C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF capacitor is sufficient to hold the gate voltage with minimal droop for the power stroke, high-side switching cycle, (i.e. ΔBST = 10mA x 3.33µs/0.1µF = 333mV) for MIC2164. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor (R_G), which is in series with C_{BST}, can slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the supply voltage (V_{IN}). The nominal low-side gate drive voltage is V_{IN} and the nominal high-side gate drive voltage is approximately $V_{IN} - V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. There is a delay for approximately 30ns between the high-side and low-side driver transitions, which used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

MOSFET Selection

The MIC2164/-2/-3 controller operates between power stage input voltages of 3V to 28V, and has an external 3V to 5.5V V_{IN} to turn the external N-Channel which powers the MOSFETs for the high- and low-side switches. For applications where V_{IN} < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for a 2.5V V_{GS}. For applications where V_{IN} > 5V, the logic-level MOSFETs with a V_{GS} of 4.5V must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles such as 12V to 1.8V conversion. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2164/-2/-3 gate-drive circuit. At 300kHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2164/-2/-3. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side]}(avg) = Q_G \times f_{SW} \quad \textbf{Eq. 6}$$

where:

$I_{G[high\text{-}side]}(avg)$ = Average high-side MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{IN}$.

f_{SW} = Switching Frequency

The low-side MOSFET is turned on and off at V_{DS} = 0 because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using CISS at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low\text{-}side]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad \textbf{Eq. 7}$$

Since the current from the gate drive comes from the VIN, the power dissipated in the MIC2164/-2/-3 due to gate drive is:

$$P_{GATEDRIVE} = V_{IN} \cdot (I_{G[high\text{-}side]}(avg) + I_{G[low\text{-}side]}(avg)) \quad \textbf{Eq. 8}$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2164/-2/-3. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current limit value. Please refer to "Current Limit" subsection is "Functional Description" for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD}. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad \textbf{Eq. 9}$$

$$P_{CONDUCTION} = I_{SW(RMS)}^{2} * R_{DS(ON)} \quad \textbf{Eq. 10}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad \textbf{Eq. 11}$$

where:

$R_{DS(ON)}$ = on-resistance of the MOSFET switch

D = Duty Cycle = V_{OUT} / V_{HSD}

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{IN} + C_{OSS} \times V_{HSD}}{I_G} \quad \textbf{Eq. 12}$$

where:

C_{ISS} and C_{OSS} are measured at $V_{DS} = 0$

I_G = gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{HSD} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad \textbf{Eq. 13}$$

where:

t_T = Switching transition time

V_D = Body diode drop (0.5V)

f_{SW} = Switching Frequency

The high-side MOSFET switching losses increase with the switching frequency and the input voltage V_{HSD}. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by the equation below:

$$L = \frac{V_{OUT} \times (V_{HSD(max)} - V_{OUT})}{V_{HSD(max)} \times f_{SW} \times 20\% \times I_{OUT(max)}} \quad \textbf{Eq. 14}$$

where:

f_{SW} = switching frequency

20% = ratio of AC ripple current to DC output current

$V_{HSD(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{HSD(max)} - V_{OUT})}{V_{HSD(max)} \times f_{SW} \times L} \quad \textbf{Eq. 15}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(PK)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(PP)} \quad \textbf{Eq. 16}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad \textbf{Eq. 17}$$

Maximizing efficiency requires both the proper selection of core material and the minimizing of the winding resistance. The high frequency operation of the MIC2164/-2/-3 requires the use of ferrite materials for all but the most cost sensitive applications.

Low-cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized even at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTORCu} = I_{L(RMS)}^2 \times R_{WINDING} \quad \textbf{Eq. 18}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING} = R_{WINDING(20°C`)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad \textbf{Eq. 19}$$

where:
T_H = temperature of wire under full load
$T_{20°C}$ = ambient temperature
$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAPS. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad \textbf{Eq. 20}$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \cdot f_{SW} \cdot 8}\right)^2 + \left(\Delta I_{L(PP)} \cdot ESR_{COUT}\right)^2} \quad \textbf{Eq. 21}$$

where:
D = Duty cycle
C_{OUT} = Output capacitance value
f_{SW} = Switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, MIC2164/-2/-3 requires at least 20mV peak-to-peak ripple at the FB pin to make the gm amplifier and the error comparator to behavior properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor C_{OUT} should be much smaller than the ripple caused by the output capacitor ESR. If low ESR capacitors are selected as the output capacitors, such as ceramic capacitors, a ripple injection method is applied to provide the enough FB voltage ripples. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad \textbf{Eq. 22}$$

The power dissipated in the output capacitor is:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT} \quad \textbf{Eq. 23}$$

Input Capacitor Selection

The input capacitor for the power stage input V_{HSD} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush cu

+rrents without voltage de-rating. The input voltage ripple will primarily depend upon the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN} \quad \textbf{Eq. 24}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1 - D)} \quad \textbf{Eq. 25}$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN} \quad \textbf{Eq. 26}$$

External Schottky Diode (Optional)

An external freewheeling diode, which is generally not necessary, can be used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically 30ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)} = I_{OUT} \cdot 2 \cdot 30ns \cdot f_{SW} \quad \textbf{Eq. 27}$$

The reverse voltage requirement of the diode is:

$$V_{DIODE(rrm)} = V_{HSD}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F \quad \textbf{Eq. 28}$$

where, V_F = forward voltage at the peak diode current.

The external Schottky diode is not necessary for the circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease the high frequency noise. If the MOSFET body diode is then used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending upon the circuit components and operating conditions, an external Schottky diode will give a ½ to 1% improvement in efficiency.

Ripple Injection

The minimum FB voltage ripple requested by the MIC2164/-2/-3 gm amplifier and error comparator is 20mV (100mV maximum). However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as 1V output, the output voltage ripple is only 10mV to 20mV, and the FB voltage ripple is less than 20mV. If the FB voltage ripple is so small that the g_m amplifier and error comparator could not sense it, then the MIC2164/-2/-3 will lose control and the output voltage will not be regulated. In order to have some amount of FB voltage ripple, the ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the FB voltage ripple:

1. Enough ripple at the FB voltage due to the large ESR of the output capacitors.

As shown in Figure 5, the converter is stable without any adding in this situation. The FB voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \cdot ESR_{C_{OUT}} \cdot \Delta I_{L(pp)} \quad \textbf{Eq. 29}$$

where ΔIL(pp) is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the FB voltage due to the small ESR of the output capacitors.

The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 6. The typical C_{ff} value is between 1nF to 100nF. With the feedforward capacitor, the FB voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \cdot \Delta I_{L(pp)} \quad \textbf{Eq. 30}$$

3. Invisible ripple at the FB voltage is due to the very low ESR of the output capacitors.

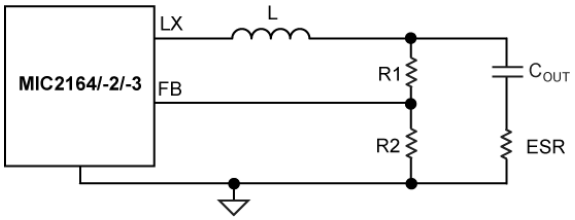


Figure 5. Enough Ripple at FB

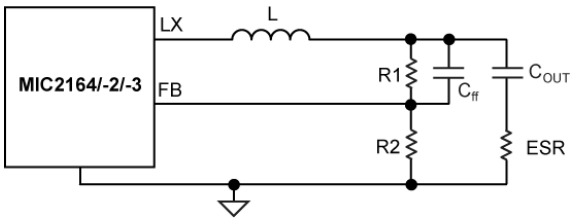


Figure 6. Inadequate Ripple at FB

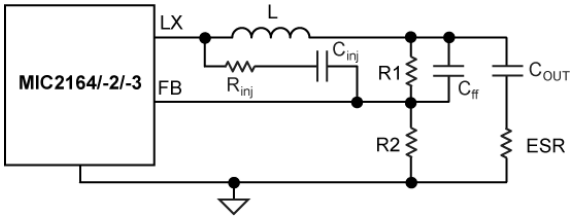


Figure 7. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node LX via a resistor Rinj and a capacitor Cinj, as shown in Figure 7. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{HSD} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau}$$

$$K_{div} = \frac{R1//R2}{Rinj + R1//R2}$$

Eq. 31

where

V_{HSD} = Power stage input voltage at HSD pin

D = Duty Cycle

f_{SW} = switching frequency

$\tau = (R1 // R2 // Rinj) \cdot Cff$

In the formula (29) and (30), it is assumed that the time constant associated with Cff must be much greater than the switching period:

$$\frac{1}{fsw \times \tau} = \frac{T}{\tau} << 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a Cff of 1nF to 100nF can easily satisfy the large time constant consumption. Also, a 100nF injection capacitor Cinj is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select Cff to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of Cff is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select Rinj according to the expected feedback voltage ripple. According to Equation 30:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{HSD}} \cdot \frac{f_{SW} \cdot \tau}{D \cdot (1-D)}$$

Eq. 32

Then the value of Rinj is obtained as:

$$R_{inj} = (R1 // R2) \cdot \left(\frac{1}{K_{div}} - 1\right)$$

Eq. 33

Step 3. Select Cinj as 100nF, which could be considered as short for a wide range of the frequencies.

(30)

Setting Output Voltage

The MIC2164/-2/-3 requires two resistors to set the output voltage, as shown in Figure 8:

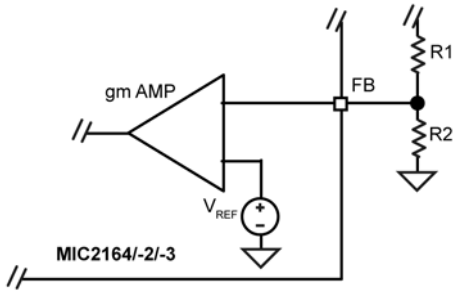


Figure 8. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2})$$

Eq. 34

where V_{REF} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

Eq. 35

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC2164/-2/-3, as shown in Figure 7. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} is increased, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected back as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC2164/-2/-3 should be limited to 5.5V to avoid this problem. If a higher output voltage is required, use the MIC2176 instead.

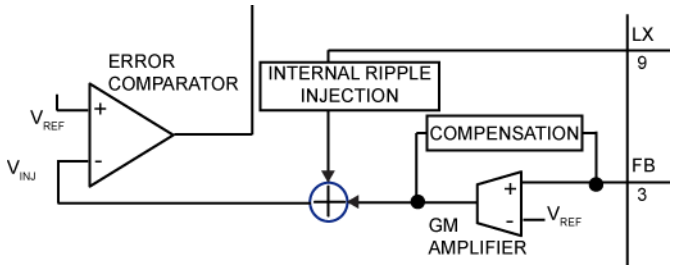


Figure 9. Internal Ripple Injection

PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2164/-2/-3 converter.

IC

- Place the IC and MOSFETs close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the HSD input capacitor next.
- Place the HSD input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Keep both the HSD and PGND connections short.
- Place several vias to the ground plane close to the HSD input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.
- An additional Tantalum or Electrolytic bypass input capacitor of 22uF or higher is required at the input power connection.
- The 1µF and 0.1µF capacitors, which connect to the V_{IN} terminal, must be located right at the IC. The V_{IN} terminal is very noise sensitive and placement of the capacitor is very critical. Connections must be made with wide trace.

Inductor

- Keep the inductor connection to the switch node (LX) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (LX) away from the feedback (FB) pin.
- The LX pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

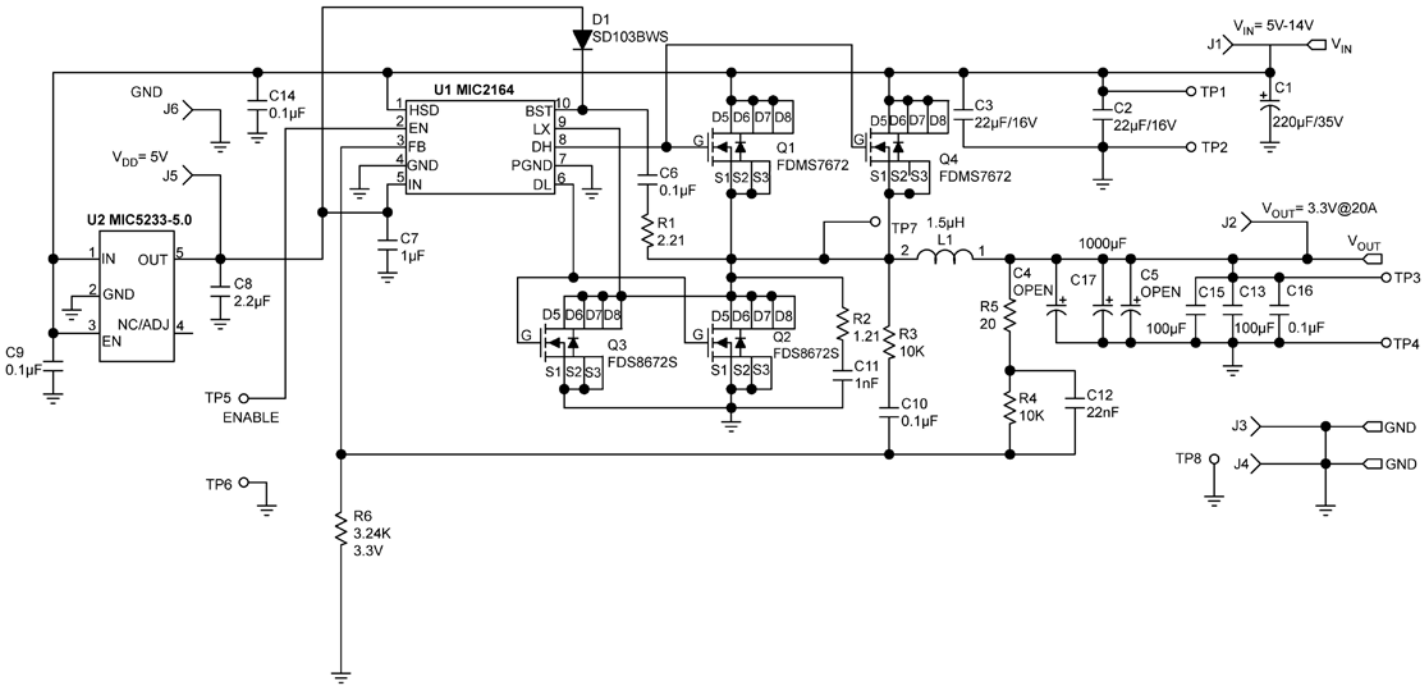
Schottky Diode (Optional)

- Place the Schottky diode on the same side of the board as the MOSFETs and HSD input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s cathode connection to the switch node (LX) must be keep as short as possible.

RC Snubber

- Place the RC snubber on the same side of the board and as close to the MOSFETs as possible.

Evaluation Board Schematic



Schematic of MIC2164 20A Evaluation Board

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	B41125A7227M	EPCOS[10]	220µF Aluminum Capacitor, SMD, 35V	1
	222215095001E3	Vishay[11]		
C2,C3	1210YD226KAT2A	AVX[12]	22µF Ceramic Capacitor, X5R, Size 1210, 16V	2
	GRM32ER61C226KE20L	Murata[13]		
	C3225X5R1C226K	TDK[14]		
C6, C9, C10, C14, C16	06035C104KAT2A	AVX	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	5
	GRM188R71H104KA93D	Murata		
	C1608X7R1H104K	TDK		
C7	0805ZD105KAT2A	AVX	1µF Ceramic Capacitor, X5R, Size 0805, 10V	1
	GRM219R61A105KC01D	Murata		
	C2012X5R1A105K	TDK		
C8	0805ZC225MAT2A	AVX	2.2µF Ceramic Capacitor, X7R, Size 0805, 10V	1
	GRM21BR71A225KA01L	Murata		
	C2012X7R1A225K	TDK		
C11	06035C102KAT2A	AVX	1nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H102KA01D	Murata		
	C1608X7R1H102K	TDK		
C12	06035C223KAZ2A	AVX	22nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H223K	Murata		
	C1608X7R1H223K	TDK		
C13, C15	12106D107MAT2A	AVX	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	2
	GRM32ER60J107ME20L	Murata		
C17	16ME1000WG	SANYO[15]	1000µF Aluminum Capacitor, 16V	1
D1	SD103BWS-7	Diodes Inc[16]	Small Signal Schottky Diode	1
	SD103BWS	Vishay		
L1	CDEP147NP-1R5M	Sumida[17]	1.5µH Inductor, 27.2A Saturation Current	1
Q1, Q4	FDMS7672	Fairchild[18]	30V N-Channel MOSFET 6.9mΩ $R_{DS(ON)}$ @ 4.5V	2
Q2, Q3	FDS8672S	Fairchild	30V N-Channel MOSFET 7mΩ $R_{DS(ON)}$ @ 4.5V	2

Notes:

10. EPCOS: www.epcos.com.
11. Vishay: www.vishay.com.
12. AVX: www.avx.com.
13. Murata: www.murata.com.
14. TDK: www.tdk.com.
15. Sanyo: www.sanyo.com.
16. Diodes Inc: www.diodes.com.
17. Sumida: www.sumida.com.
18. Fairchild: www.fairchildsemi.com.

Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R1	CRCW06032R21FKEA	Vishay/Dale	2.21Ω Resistor, Size 0603, 1%	1
R2	CRCW06031R21FKEA	Vishay/Dale	1.21Ω Resistor, Size 0603, 1%	1
R3,R4	CRCW060310K0FKEA	Vishay/Dale	10kΩ Resistor, Size 0603, 1%	2
R5	CRCW060320R0FKEA	Vishay/Dale	20Ω Resistor, Size 0603, 1%	1
R6	CRCW06033K24FKEA	Vishay/Dale	3.24kΩ Resistor, Size 0603, 1%	1
U1	**MIC2164YMM**	**MICREL INC[19]**	**300kHz Buck Controller**	**1**
U2[20]	**MIC5233-5.0YM5**	**MICREL INC**	**LDO**	**1**

Notes:

19. **Micrel, Inc.: www.micrel.com.**
20. Optional: Required if 5V supply is not available in the system.