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MIC2225

2MHz 600mA Synchronous Buck Regulator with 300mA LDO

General Description

The Micrel MIC2225 is a dual output regulator featuring a high efficiency 2MHz PWM synchronous buck (step-down) regulator and a 300mA LDO. The MIC2225 is an ultra-low noise, small size, and high efficiency solution for portable power applications, providing core and I/O supply rails for applications like application processors, camera DSPs and multimedia chipsets.

In PWM mode, the MIC2225 operates with a constant 2MHz frequency. The MIC2225 switching regulator operates from 2.7V to 5.5V input and features internal power MOSFETs that can supply up to 600mA output current in PWM mode.

The MIC2225 is available in the 10-pin 2mm x 2mm Thin MLF[®] package with a junction operating range from -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

DC-DC Converter

- 2.7 to 5.5V supply voltage
- 2MHz PWM mode
- Output current to 600mA
- >95% efficiency
- 100% maximum duty cycle
- Fixed output voltage option down to 1V
- Ultra-fast transient response
- Stable with 2.2 μ F ceramic output capacitor
- Fully integrated MOSFET switches
- Micropower shutdown (1mA in shutdown)
- Thermal shutdown and current limit protection
- Pb-free 10-pin 2mm x 2mm Thin MLF[®] package
- -40°C to +125°C junction temperature range

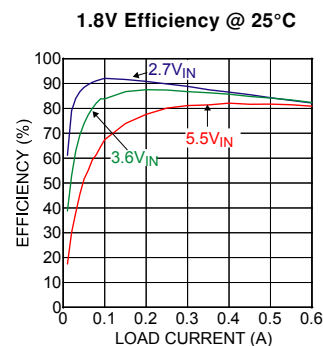
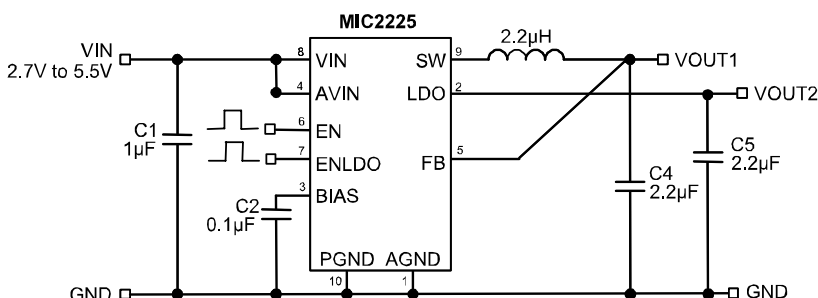
LDO

- V_{IN} range 2.7V to 5.5V
- 300mA output current
- Output voltage down to 0.8V
- Thermal shutdown protection
- Current limit protection

Applications

- Cellular phones
- PDAs
- USB peripherals

Typical Application



MLF and MicroLeadFrame are registered trademarks of Amkor Technology, Inc.

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Ordering Information

Part Number	Marking Code	Voltage*	Temperature Range	Package	Lead Finish
MIC2225-4KYMT	4TK	1.2V/2.6V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-4MYMT	4TM	1.2V/2.8V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-4OYMT	4TO	1.2V/2.9V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-4SYMT	4TS	1.2V/3.3V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-G4YMT	GT4	1.8V/1.2V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-GFYMT	GTF	1.8V/1.5V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-GJYMT	GTJ	1.8V/2.5V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free
MIC2225-GMYMT	GTM	1.8V/2.8V	-40° to +125°C	10-Pin 2x2 Thin MLF®	Pb-Free

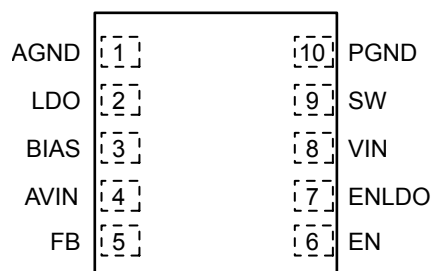
Note:

MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Other voltage options available. Please contact Micrel for details.

* Refers to nominal output voltage of DC/DC and LDO respectively.

Pin Configuration



10-Pin 2mm x 2mm Thin MLF® (MT)

Pin Description

Pin Number	Pin Name	Pin Function
1	AGND	Analog (signal) Ground.
2	LDO	LDO Output (Output): Connect to a 2.2 μ F output capacitor.
3	BIAS	Internal circuit bias supply. Must be de-coupled to signal ground with a 0.1 μ F capacitor and should not be loaded.
4	AVIN	Analog Supply Voltage (Input): Supply voltage for the analog control circuitry and LDO input power. Requires bypass capacitor to GND. It must be tied to VIN.
5	FB	Feedback. Input to the error amplifier. For the Adjustable option, connect to the external resistor divider network to set the output voltage. For fixed output voltage options, connect to V _{OUT} and an internal resistor network sets the output voltage.
6	EN	Enable (Input). Logic low will shut down the switching regulator reducing the quiescent current to less than 5 μ A.
7	ENLDO	Enable LDO (Input): Logic low will shut down the LDO, reducing the quiescent current to less than 5 μ A.
8	VIN	Supply Voltage (Input): Supply voltage for the internal switches and drivers.
9	SW	Switch (Output): Internal power MOSFET output switches.
10	PGND	Power Ground.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{IN}).....	+6V
Output Switch Voltage (V_{SW}).....	+6V
Output Switch Current (I_{SW}).....	1A
Logic Input Voltage (V_{EN}, V_{LOWQ}).....	-0.3V to V_{IN}
Storage Temperature (T_s).....	-60°C to +150°C
ESD Rating ⁽³⁾	2kV

Operating Ratings⁽²⁾

Supply Voltage (V_{IN}).....	+2.7V to +5.5V
Logic Input Voltage (V_{EN}, V_{LOWQ}).....	-0.3V to V_{IN}
Junction Temperature (T_J).....	-40°C to +125°C
Junction Thermal Resistance Thin MLF-10L (θ_{JA}).....	90°C/W

Electrical Characteristics DC/DC⁽⁴⁾

$V_{EN} = V_{IN} = 3.6V$, $L = 2.2\mu H$; $C_{OUTDC/DC} = 2.2\mu F$, $C_{LDO} = 2.2\mu F$; $I_{OUTDC/DC} = 100mA$; $C_{BIAS} = 0.1\mu F$

$V_{ENLDO} = 0V$; $T_J = 25^\circ C$, **bold** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$; unless noted.

Parameter	Condition	Min	Typ	Max	Units
UVLO Threshold	Rising input voltage during turn-on	2.45	2.55	2.65	V
UVLO Hysteresis			70		mV
Switcher Ground Pin Current	ENLDO = 0V, $V_{FB} = GND$; $I_L = 0mA$		850	1100	μA
LDO Ground Pin Current	EN = 0V		67	110	μA
Ground Pin Current in Shutdown	EN +ENLDO = 0V		0.2	5	μA
Over-temperature Shutdown			160		$^\circ C$
Over-temperature Shutdown Hysteresis			23		$^\circ C$
Enable Input Voltage	Logic Low			0.2	V
	Logic High	1.0			V
Enable Input Current	$V_{IL} \leq 0.2V$		0.1	1	μA
	$V_{IH} \geq 1.0V$		0.1	1	μA
Turn-on Time	$I_{LOAD} = 5mA$		50		μs
Fixed Output Voltages	Nominal V_{OUT} tolerance $I_o = 50mA$	-2		+2	%
		-3		+3	%
Current Limit in PWM Mode	$V_{FB} = 0.9 * V_{NOM}$	0.675	0.95		A
Output Voltage Line Regulation	$V_{IN} = 2.7V$ to $5.5V$, $I_{LOAD} = 100mA$		0.12	1	% %
Output Voltage Load Regulation	$20mA < I_{LOAD} < 300mA$		0.2	1.5	%
Maximum Duty Cycle	$V_{FB} \leq 0.4V$	100			%
PWM Switch ON-Resistance	$I_{SW} = 150mA$; $V_{FB} = 0.7V_{FB_NOM}$ $I_{SW} = -150mA$; $V_{FB} = 1.1V_{FB_NOM}$		0.4		Ω
			0.4		Ω
Oscillator Frequency		1.8	2	2.2	MHz

Electrical Characteristics LDO⁽⁴⁾

$C_{OUTLDO} = 2.2\mu\text{F}$, $I_{OUTLDO} = 100\mu\text{A}$; $T_J = 25^\circ\text{C}$, **bold** values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$; unless noted.

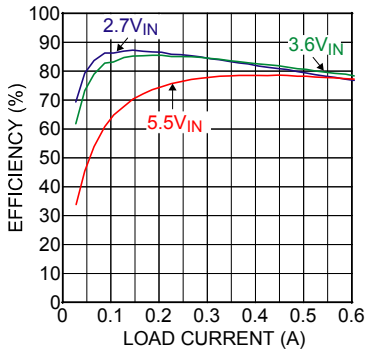
Parameter	Condition	Min	Typ	Max	Units
Input Voltage		2.7		5.5	V
Output Voltage Accuracy	Variation from nominal V_{OUT}	-2.0		+2.0	%
	Variation from nominal V_{OUT} ; -40°C to $+125^\circ\text{C}$	-3.0		+3.0	%
Line Regulation	$V_{IN} = V_{OUT} + 1\text{V}$ to 5.5V ; $I_{OUT} = 100\mu\text{A}$		0.2		%
Turn-on Time	$I_{LOAD} = 300\text{mA}$		30		μs
Load Regulation	$I_{OUT} = 100\mu\text{A}$ to 300mA @ $V_{IN} = V_{OUT} + 1$		0.70		%
Dropout Voltage, Note 5	$I_{OUT} = 300\text{mA}$ @ $V_{IN} = 2.7\text{V}$		210		mV
Ripple Rejection	$f = 1\text{kHz}$; $C_{OUT} = 2.2\mu\text{F}$		43		dB
	$f = 20\text{kHz}$; $C_{OUT} = 2.2\mu\text{F}$		17		dB
Current Limit	$V_{OUT} = 0\text{V}$	400			mA
Output Voltage Noise	$C_{OUT} = 2.2\mu\text{F}$, 10Hz to 100kHz		470		μV_{RMS}

Notes:

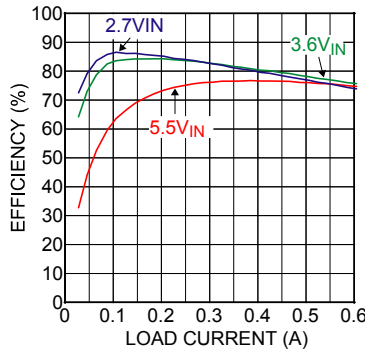
- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
- Specification for packaged product only.
- Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value that is initially measured at a 1V differential. For outputs below 2.7V, the dropout voltage is the input-to-output voltage differential with a minimum input voltage of 2.7V.

Typical Characteristics (DC-DC)

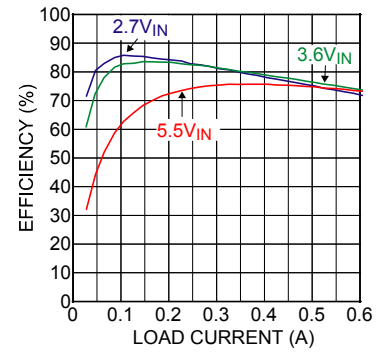
1.2V Efficiency @ -40°C



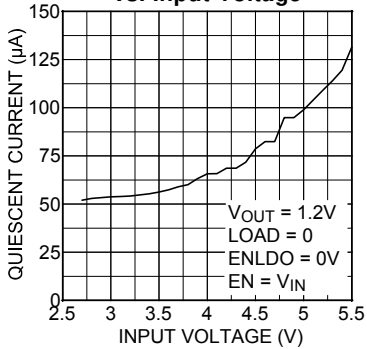
1.2V Efficiency @ 25°C



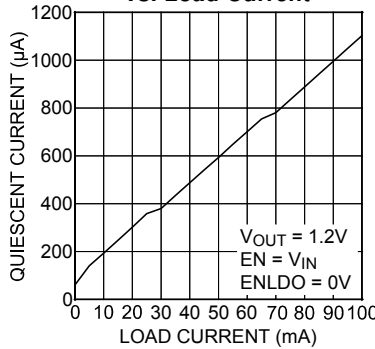
1.2V Efficiency @ 70°C



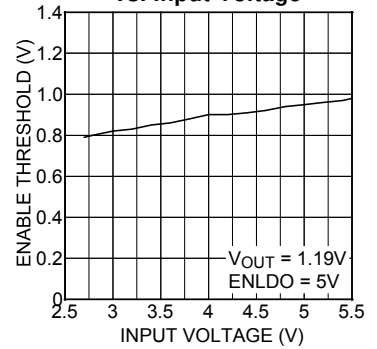
Quiescent Current vs. Input Voltage



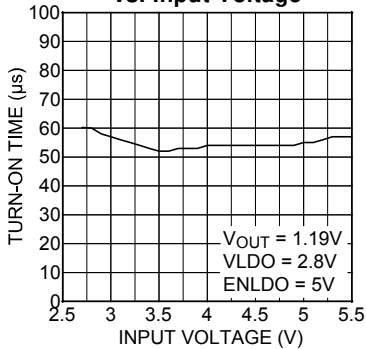
Quiescent Current vs. Load Current



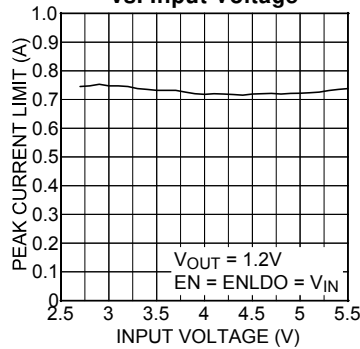
Enable Threshold vs. Input Voltage



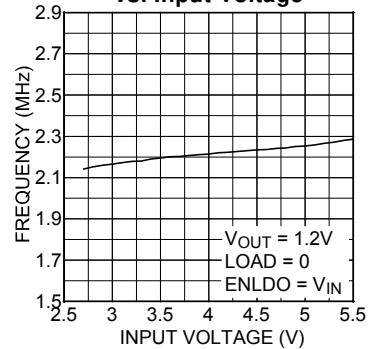
Turn-On Time vs. Input Voltage



Peak Current Limit vs. Input Voltage

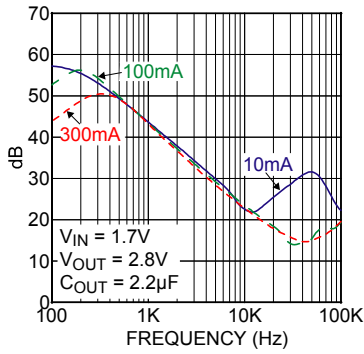


Frequency vs. Input Voltage

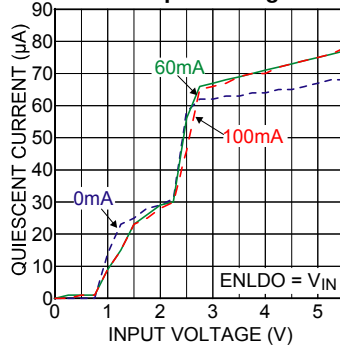


Typical Characteristics (LDO)

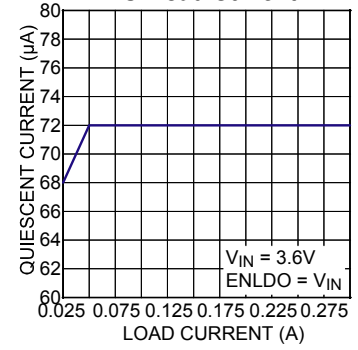
PSRR



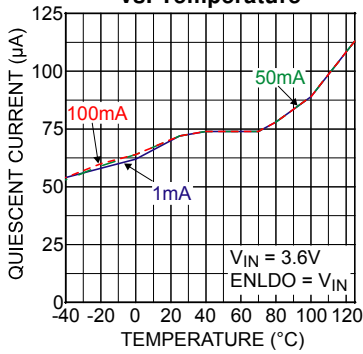
Quiescent Current vs. Input Voltage



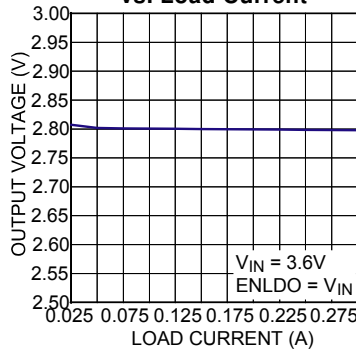
Quiescent Current vs. Load Current



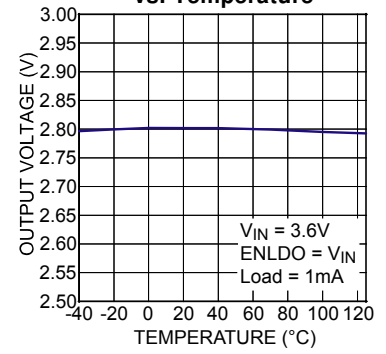
Quiescent Current vs. Temperature



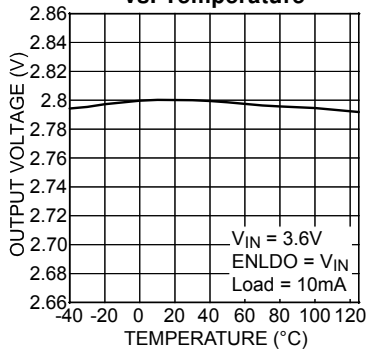
Output Voltage vs. Load Current



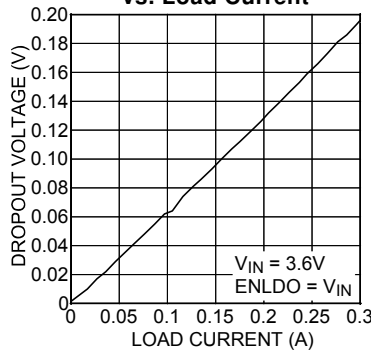
Output Voltage vs. Temperature



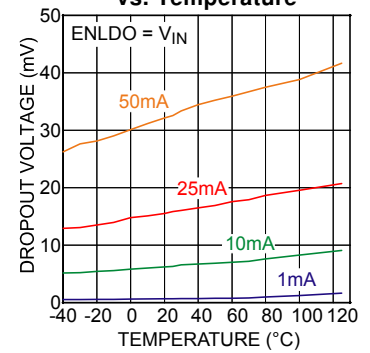
Output Voltage vs. Temperature



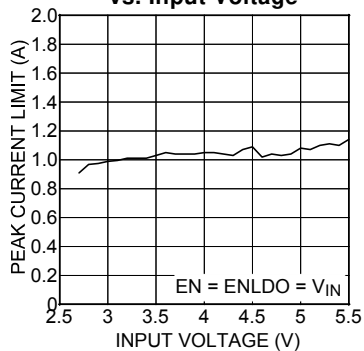
Dropout Voltage vs. Load Current



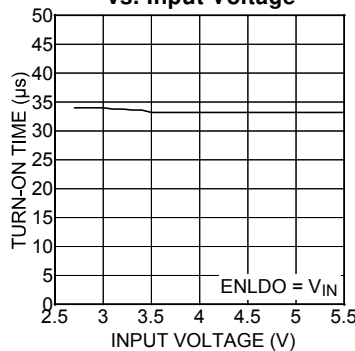
Dropout Voltage vs. Temperature



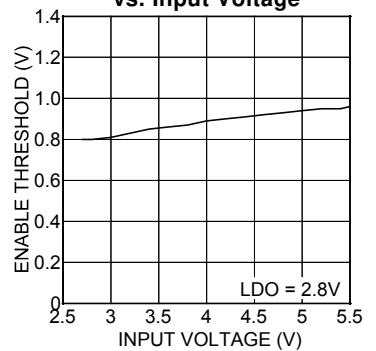
Peak Current Limit vs. Input Voltage



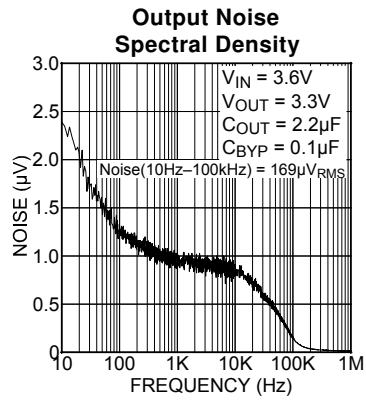
Turn-On Time vs. Input Voltage



Enable Threshold vs. Input Voltage

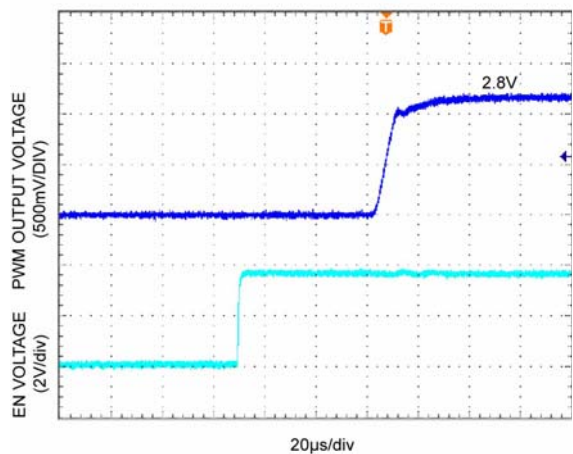


Typical Characteristics (LDO) continued

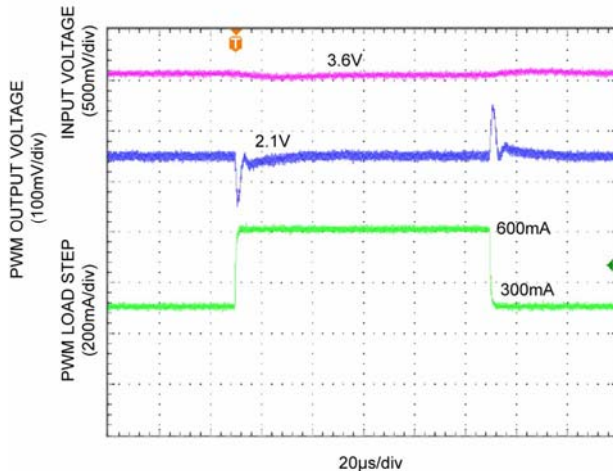


Functional Characteristics

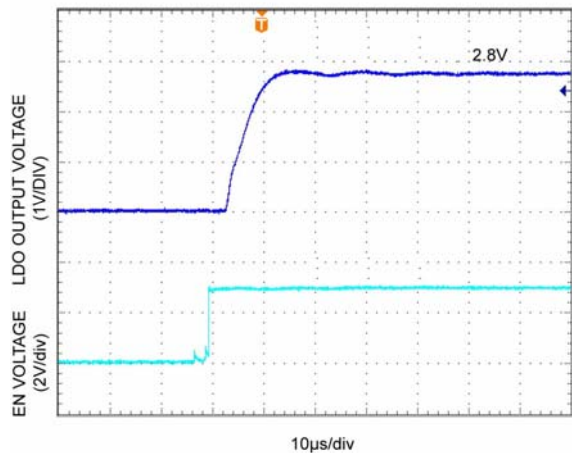
DC-DC Enable



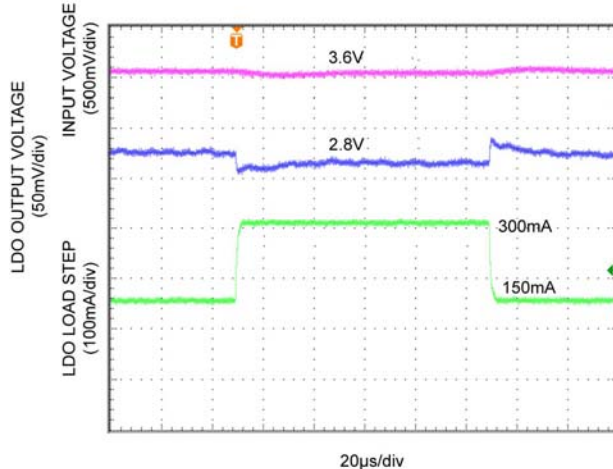
DC-DC Load Transient



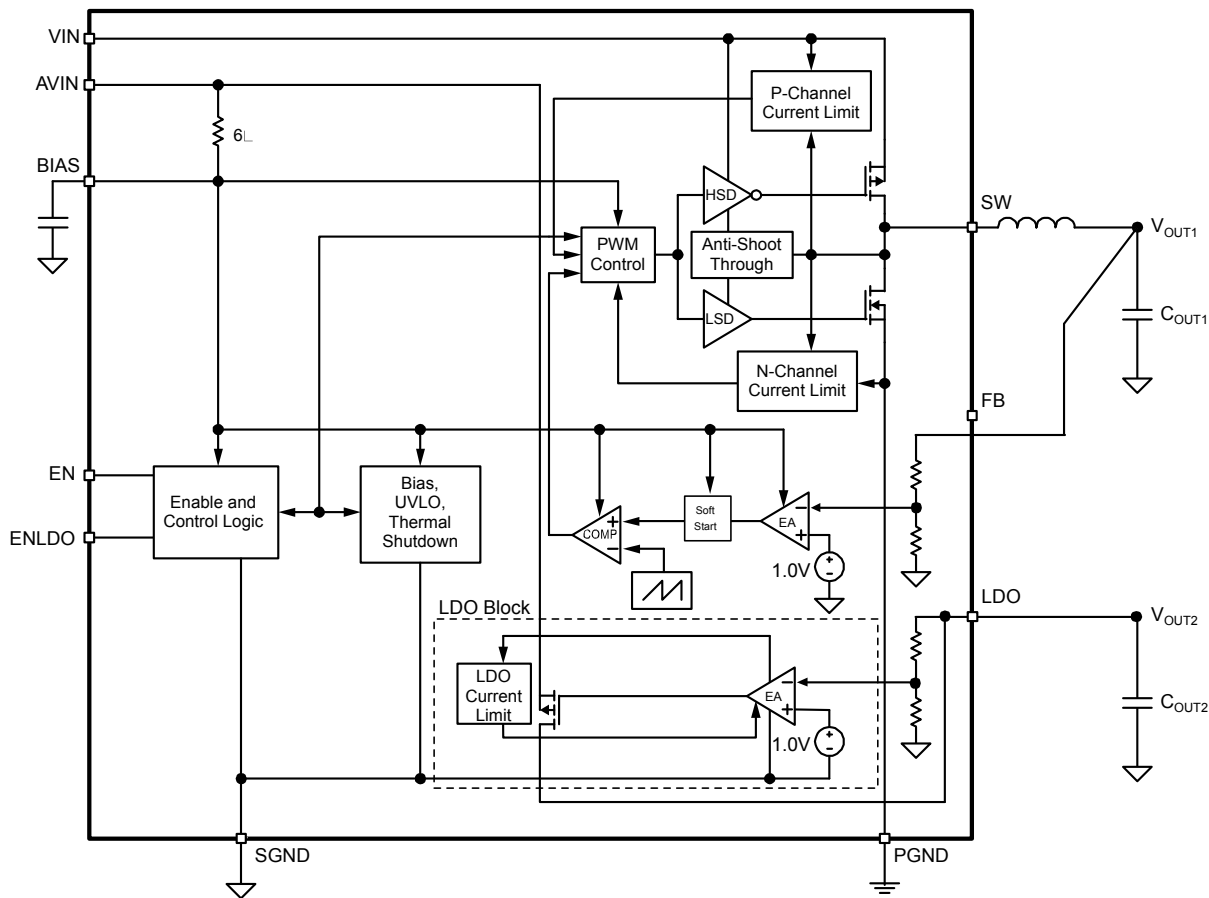
LDO Enable



LDO Load Transient



Functional Diagram



MIC2225 Block Diagram

Functional Description

VIN

VIN provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, it is recommended that a 1 μ F capacitor be placed close to VIN and the power ground (PGND) pin for bypassing. Please refer to layout recommendations.

AVIN

Analog VIN (AVIN) provides power to the LDO section and the bias through an internal 6 Ω resistor. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN.

LDO

The LDO pin is the output of the linear regulator and needs to be connected to a 2.2 μ F output capacitor.

EN

The enable pin provides a logic level control of the output. In the off state, the supply current of the device is greatly reduced (typically <1 μ A). Also, in the off state, the output drive is placed in a "tri-stated" condition, wherein both the high side P-channel MOSFET and the low-side N-channel are in an "off" or non-conducting state. Do not drive the enable pin above the supply voltage.

ENLDO

The enable pin provides a logic level control of the LDO output. In the off state, supply current of the device is greatly reduced (typically <1 μ A). Do not drive the enable pin above the supply voltage.

BIAS

The BIAS pin supplies the power to the internal power to the control and reference circuitry. The bias is powered from AVIN through an internal 6 Ω resistor. A small 0.1 μ F capacitor is recommended for bypassing.

FB

The feedback pin (FB) provides the control path to control the output. For fixed output, the controller output is directly connected to the feedback (FB) pin.

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop. Refer to the layout considerations for more details.

SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop. Refer to the layout considerations for more details.

Application Information

The MIC2225 is a 600mA PWM and 300mA LDO dual power supply. Both PWM output and LDO outputs are independent and are controlled by EN and ENLDO pins respectively. These enable pins are logic level compatible.

Input Capacitor

A minimum 1 μ F ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

A minimum 1 μ F is recommended for placement close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to layout recommendations for proper layout of the input capacitor.

Output Capacitor

Even though the MIC2225 is optimized for a 2.2 μ F output capacitor, output capacitance can be varied from 1 μ F to 10 μ F. The MIC2225 utilizes Type III internal compensation and utilizes an internal high frequency zero to compensate for the double pole roll off of the LC filter. For this reason, larger output capacitors can create instabilities. X5R or X7R dielectrics are recommended for the output capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore,

not recommended.

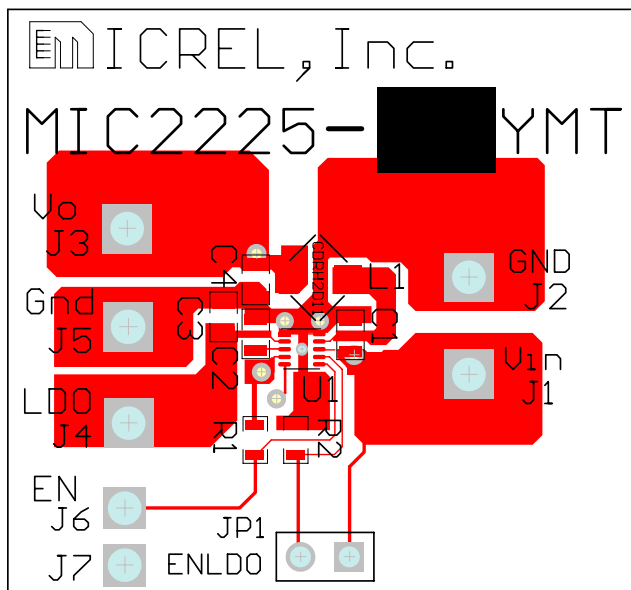
In addition to a 2.2 μ F, a small 10nF is recommended close to the load for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL.

Inductor Selection

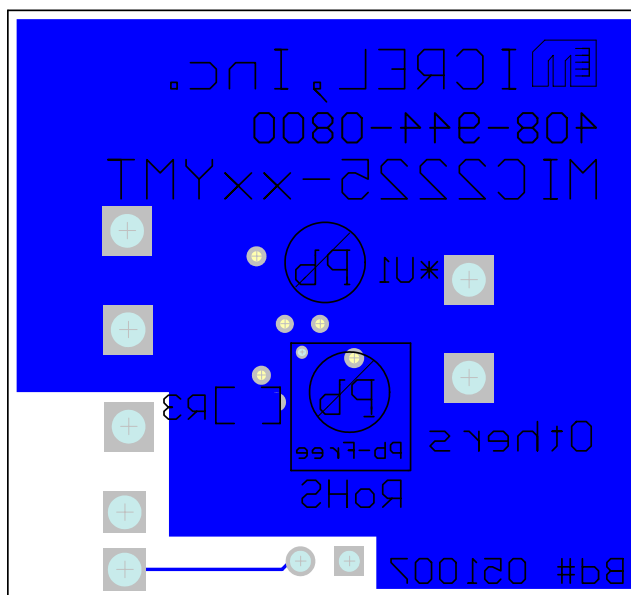
The MIC2225 is designed for use with a 2.2 μ H inductor. Proper selection should ensure that the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings for the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{2 \times f \times L}$$

PCB Layout Recommendations



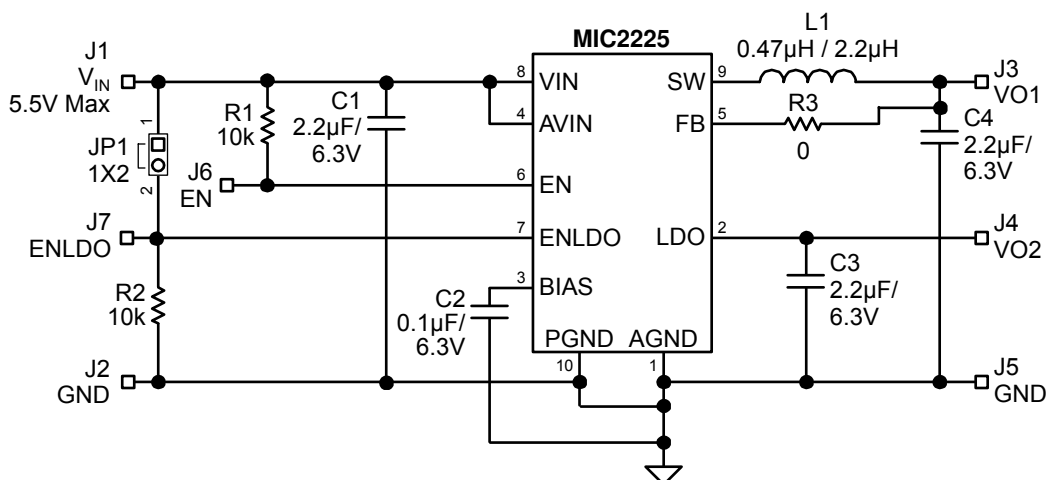
Top Layer



Bottom Layer

Note:

The above figures demonstrate the recommended layout for the MIC2225 fixed output option.



Schematic Diagram

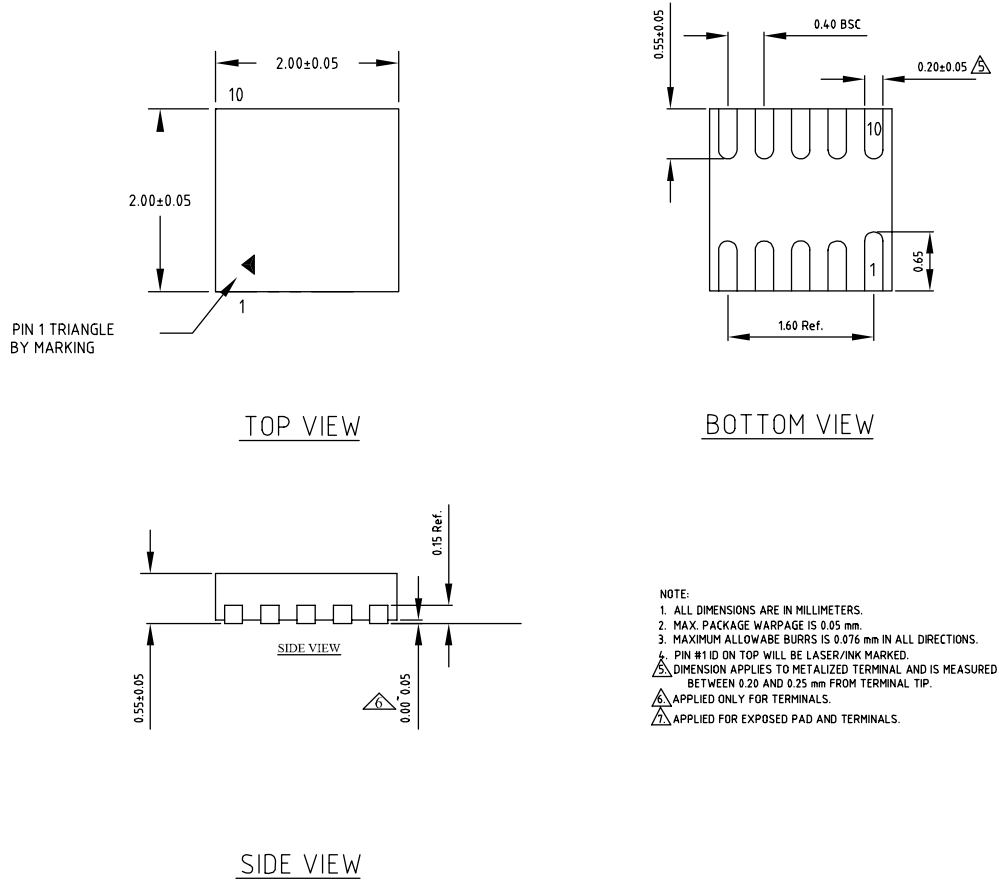
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X5R0J225K	TDK ⁽¹⁾	2.2µF/6.3V, X5R	1
C2	VJ0402Y104KXQCW1BC	Vishay Vitramon ⁽²⁾	0.1µF/6.3V, X7R	1
C3	C1608X5R0J225K	TDK ⁽¹⁾	2.2µF/6.3V, X5R	1
C4	C1608X5R0J225K	TDK ⁽¹⁾	2.2µF/6.3V, X5R	1
R1	CRCW06031002FKEYE3	Vishay Dale ⁽²⁾	10k, 0603, 1/16W, 1%	1
R2	CRCW06031002FKEYE3	Vishay Dale ⁽²⁾	10k, 0603, 1/16W, 1%	1
R3	CRCW08050000FKEYE3	Vishay Dale ⁽²⁾	0, 0805, 1/8W, 1%	1
L1	CDRH2D11/HPNP-2R2NC	Sumida ⁽³⁾	2.2µH, 1.1A (Isat)	1
U1	MIC2225-XYMT	Micrel, Inc. ⁽⁴⁾	2Mhz PWM Synchronous Buck Regulator with 300mA LDO	1

Notes:

1. TDK: www.tdk.com
2. Vishay: www.vishay.com
3. Sumida: www.sumida.com
4. Micrel, Inc.: www.micrel.com

Package Information



10-Pin Thin MLF[®] (MT)

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