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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MIC2341/2341R

Dual-Slot PCI Express Hot-Plug Controller

General Description

The MIC2341 is a dual-slot power controller supporting the power distribution requirements for Peripheral Component Interconnect Express (PCI Express) Hot-Plug compliant systems. The MIC2341 provides complete power control support for two PCI Express slots, including the 3.3VAUX defined by the PCI Express standards. Support for the 12V, 3.3V, and 3.3VAUX supplies includes programmable gate voltage slew-rate control, voltage supervision, programmable current limit, and circuit breaker functions. These features provide comprehensive system protection and fault isolation.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Supports two independent PCI Express slots
- 12V, 3.3V, and 3.3VAUX supplies supported per PCI Express Specification v1.0a, v.2.0
  - Integrated Power MOSFETS for 3.3VAUX rails
  - Standby Operation for Wake-on-LAN applications with low backfeed on Main +12V and +3.3V rails
- Electronic circuit breakers for each supply per slot
  - Programmable gate voltage slew-rate control
  - Active current regulation controls inrush current
- High accuracy Primary and Secondary Circuit Breaker Current-limit Thresholds
- Dual-level, dual-speed fault detection for fast response without nuisance tripping
- User-programmable Primary Overcurrent Detector
- /PWRGD and Delayed /PWRGD (164 ms) signal outputs per slot
- Separate /FAULT output signals for MAIN and AUX rails for each slot
- Global Systems Power-is-Good Output
- Both slots thermally isolated
- Internally Debounced Plug-in Card Retention Switch Inputs per slot.

Applications

- PCI Express v1.0a, v2.0 hot-plug power control

PCI Express is a registered trademark of the PCI SIG

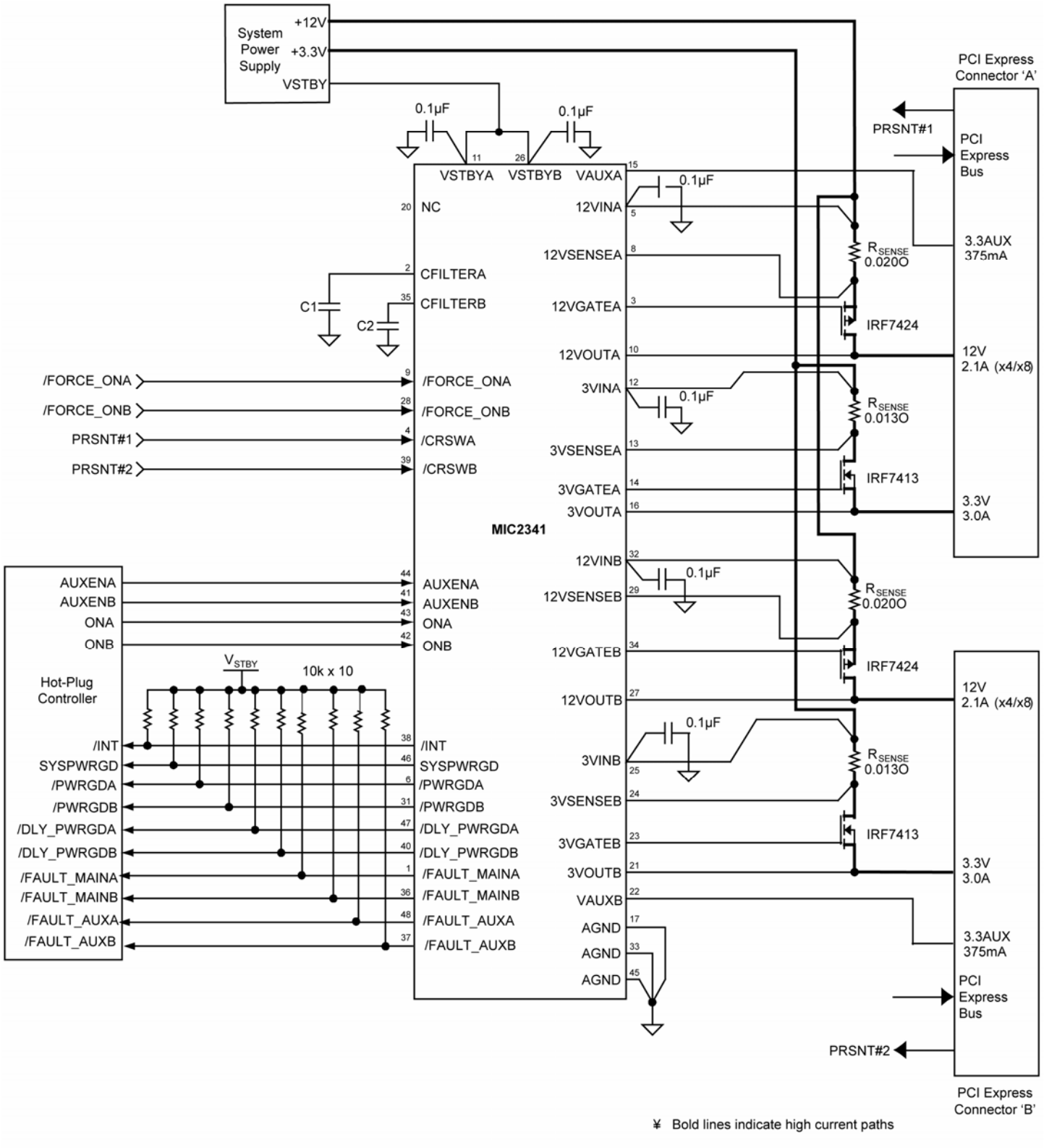
Ordering Information

Part Number		12V and 3V Fast-Trip Thresholds	3.3VAUX Nominal Current Limit	Package
Latch Off	Auto-Retry			
MIC2341–2YTQ	MIC2341R–2YTQ	100mV	0.375A	48 Pin TQFP
MIC2341–3YTQ[1]	MIC2341R–3YTQ[1]	150mV	0.375A	48 Pin TQFP
MIC2341–5YTQ[1]	MIC2341R–5YTQ[1]	Disabled	0.375A	48 Pin TQFP

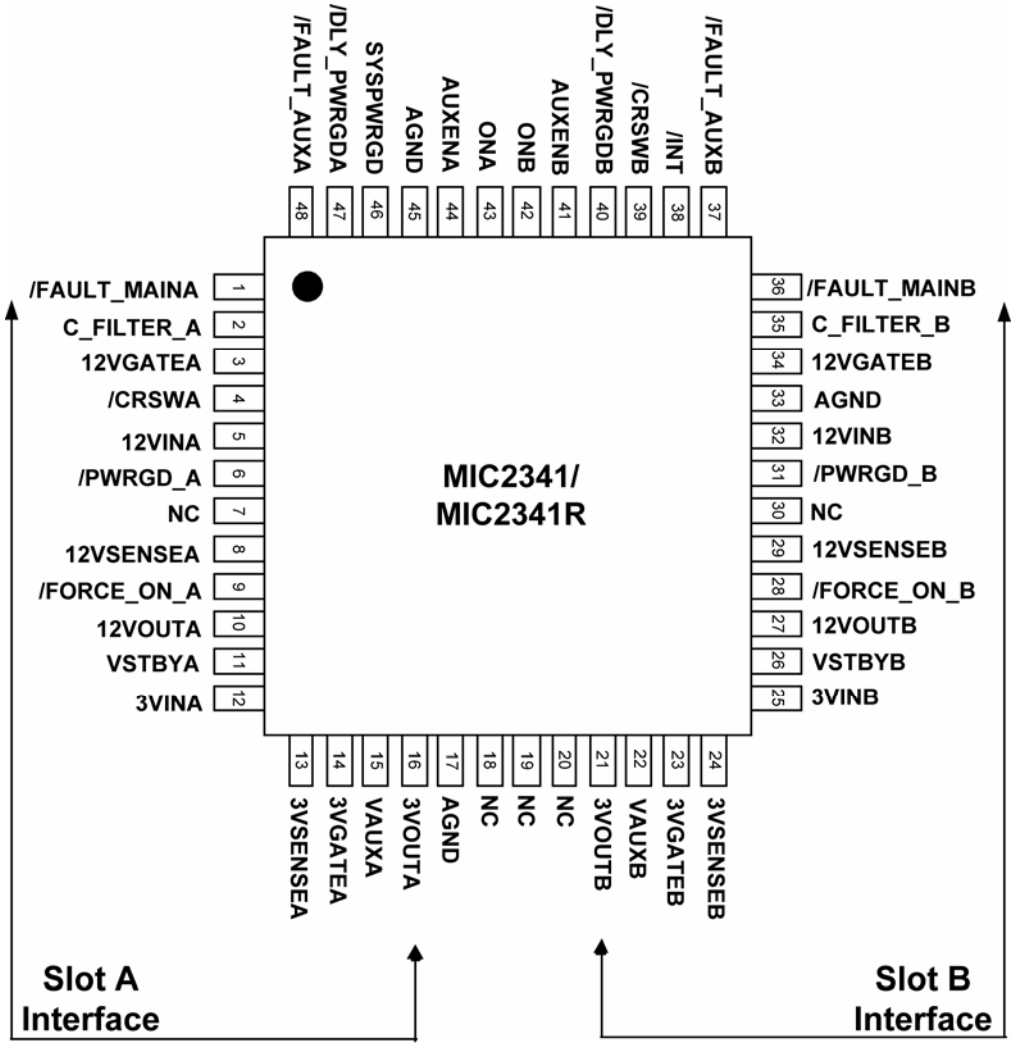
Note:

1. Contact factory for availability

Typical Application



Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
5 32	12VINA 12VINB	12V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin connection (one for each slot). Pin 5 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 12V Slot A. Pin 32 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 12V Slot B. These two pins must ultimately connect to each other as close as possible at the MIC2341 controller in order to eliminate any IR drop between these pins. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is lower than its lockout threshold voltage.
12 25	3VINA 3VINB	3.3V Supply Power and Sense Inputs [A/B]: Two pins are provided for connection (one for each slot). Pin 12 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 3V Slot A. Pin 25 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 3V Slot B. These two pins must ultimately connect to each other as close as possible at the MIC2341 controller in order to eliminate any IR drop between these pins. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is lower than its lockout threshold voltage.
16 21	3VOUTA 3VOUTB	3.3V Power-Good Sense Inputs: Connect to 3.3V[A/B] outputs. Used to monitor the 3.3V output voltages for 3.3V Output Power-is-Good status.
10 27	12VOUTA 12VOUTB	12V Power-Good Sense Inputs: Connect to 12V[A/B] outputs. Used to monitor the 12V output voltages for 12V Output Power-is-Good status.
8 29	12VSENSEA 12VSENSEB	12V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 12VIN[A/B]. When the 12V primary overcurrent detector current-limit threshold of 50mV is reached, the 12VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT} or t_{DFLT} (whichever is shorter), the circuit breaker is tripped and the corresponding 12VGATE pin for the affected slot is immediately pulled up to its corresponding 12VIN to turn OFF the external MOSFET.
13 24	3VSENSEA 3VSENSEB	3V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 3VIN[A/B]. When the 3V primary overcurrent detector current-limit threshold of 50mV is reached, the 3VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT} or t_{DFLT} (whichever is shorter), the circuit breaker is tripped and the corresponding 3VGATE pin for the affected slot is immediately pulled down to AGND to turn OFF the external MOSFET.
3 24	12VGATEA 12VGATEB	12V Gate Drive Outputs [A/B]: Each pin connects to the gate of an external P-channel power MOSFET. During power-up, the external C_{GATE} (if used) and the C_{GS} of the external MOSFETs are connected to a 25µA current sink. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the 12V load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the FET for a period of t_{FLT} or t_{DFLT} (whichever is shorter). Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the corresponding 12VGATE pin for the affected slot is pulled up to its corresponding 12VIN pin to turn OFF the external MOSFET.

Pin Description (cont.)

Pin Number	Pin Name	Pin Function
14 23	3VGATEA 3VGATEB	3V Gate Drive Outputs [A/B]: Each pin connects to the gate of an external N−channel power MOSFET. During power-up, the C_{GATE} (if used) and the C_{GS} of the external MOSFETs are connected to a 25µA current source. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the 3V load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the FET for a period of t_{FLT} or t_{DFLT} (whichever is shorter). Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the corresponding 3VGATE pin for the affected slot is pulled down to AGND to turn OFF the external MOSFET.
11 26	VSTBYA VSTBYB	3.3V Standby Supply Voltage: Required to support the PCI Express VAUX output. Additionally, all internal logic circuitry operates on VSTBY[A/B]. An internal UVLO circuit prevents turn-on of the external 3.3VAUX supply until the voltage at the VSTBY[A/B] pins is higher than the $V_{UVLO(STBY)}$ threshold voltage. Both pins must be externally connected together at the MIC2341 controller.
15 22	VAUXA VAUXB	3.3VAUX[A/B] Outputs to PCI Express Card Slots: These outputs connect the 3.3AUX pin of the PCI Express connectors to VSTBY[A/B] via internal 0.4-Ω MOSFETs. These outputs are current limited and protected against short-circuit faults.
44 43	ONA ONB	Main +12VOUT[A/B] and +3.3VOUT[A/B] Enable Inputs: These level-sensitive digital inputs are each internally connected with pull-up resistors to VSTBY[A] and are used to enable or disable the MAIN[A/B] (+3.3V and +12V) outputs. Applying a high-to-low transition on ON[A/B] for at least 200ns (t_{LPW}) after a fault resets the +12V and/or +3.3V fault latches for the affected slot and de-asserts the /FAULT_MAIN[A/B] output signals. The +12V and/or the +3.3V electronic circuit breakers are reset once the /FAULT_MAIN[A/B] output signals are de-asserted.
45 42	AUXENA AUXENB	VAUX[A/B] Enable Inputs: These level-sensitive digital inputs are each internally connected with pull-up resistors to VSTBY[A] and are used to enable or disable the VAUX[A/B] outputs. Applying a high-to-low transition on AUXEN[A/B] for at least 200ns (t_{LPW}) after a fault resets the VAUX fault latches for the affected slot and de-asserts the /FAULT_AUX[A/B] output signals. The VAUX[A/B] electronic circuit breakers are reset once the /FAULT_AUX[A/B] output signals are de-asserted.
2 35	CFILTERA CFILTERB	Overcurrent Filter Capacitor [A/B]: Capacitors connected between these pins and AGND set the duration of t_{FLT}, the response time of the primary overcurrent (OC) detector circuits. t_{FLT} is the amount of time for which a slot remains in current limit before its circuit breaker is tripped. To configure the controller to use its internal digital filter delay timer, CFILTER[A/B] pins shall be connected to AGND
6 31	/PWRGDA /PWRGDB	/PWRGD[A/B] are open-drain, asserted active-LOW digital outputs that are normally connected by an external 10kΩ pull-up resistor (each) to VSTBY. Each output signal is asserted when inputs signals ON[A/B] and AUXEN[A/B] have been enabled, each output voltage has crossed its respective Power-is-Good output threshold ($V_{UVTH(12V)}$, $V_{UVTH(3V)}$, and $V_{UVTH(VAUX)}$ threshold voltages), and no fault conditions exist . Please consult the /PWRGD[A/B] and the /DLY_PWRGD[A/B] state diagrams in the Applications Information section for more detail.

Pin Description (cont.)

Pin Number	Pin Name	Pin Function
1 36	/FAULT_MAINA /FAULT_MAINB	/FAULT_MAIN[A/B] Outputs are open-drain, asserted active-LOW digital outputs that are normally connected by an external 10kΩ resistor to VSTBY. Asserted whenever the primary or secondary circuit breaker trips because of an overcurrent fault condition or an input undervoltage. Applying a high-to-low transition at the ON[A/B] pin resets the /FAULT_MAIN[A/B] outputs if /FAULT_MAIN[A/B] was asserted in response to a fault condition on one of the slot's MAIN outputs (+12V or +3.3V). If an overcurrent event asserted /FAULT_MAIN[A/B], the respective output's circuit breaker is reset when /FAULT_MAIN[A/B] output signal is de-asserted. A 200ns minimum pulse width (t_{LPW}) for ON[A/B] will reset the MAIN outputs in the event of an overcurrent fault once the fault is removed. If a fault condition occurred on both the MAIN and VAUX outputs of the same slot, then a high-to-low transition on both ON[A/B] and AUXEN[A/B] must be applied to de-assert the /FAULT_MAIN[A/B] and /FAULT_AUX[A/B] outputs. To simplify system fault reporting, the /FAULT_MAIN[A/B] output pins may be connected together with the /FAULT_AUX[A/B] output pins.
4 39	/CRSWA /CRSWB	Card Retention Switch Inputs [A/B]. These are level sensitive, asserted active- LOW digital inputs with internal pull-up resistors to VSTBY[A]. These inputs can be connected to the PRNST#1 or PRNST#2 pins on a PCIe connector to indicate to the MIC2341 that a PCIe plug-in card is present and firmly mated. Internally, the MIC2341's +12VGATE[A/B], +3VGATE[A/B], and 3VAUX[A/B] gate drive circuits are gated with the MIC2341's ON[A/B] and the AUXEN[A/B] inputs to deliver power to the connector only when a PCIe plug-in card is present. During operation, if the /CRSW[A/B] inputs are disconnected or if there is a pc board trace failure, all outputs on the respective slot are turned OFF without delay. Each of these inputs exhibit an internal switch debounce delay of approximately 10ms.
48 37	/FAULT_AUXA /FAULT_AUXB	/FAULT_AUX[A/B] Outputs are open-drain, asserted active-LOW digital outputs that are normally connected by an external 10kΩ resistor to VSTBY. Asserted whenever the VAUX[A/B] circuit breaker trips because of an overcurrent fault condition or a slot/die overtemperature condition. Applying a high-to-low transition at the AUXEN[A/B] pin for at least 0.5µs resets the /FAULT_AUX[A/B] outputs if the /FAULT_AUX[A/B] output signal was asserted in response to a fault condition on the respective slot's VAUX output. If an overcurrent event asserted /FAULT_AUX[A/B], the respective output's VAUX circuit breaker is reset when /FAULT_AUX[A/B] output signal is de-asserted. A 200ns minimum pulse width (t_{LPW}) for AUX_EN[A/B] will reset the MAIN outputs in the event of an overcurrent fault once the fault is removed. If a fault condition occurred on both the MAIN and VAUX outputs of the same slot, then a high-to-low transition on both ON[A/B] and AUXEN[A/B] must be applied to de-assert the /FAULT_MAIN[A/B] and /FAULT_AUX[A/B] outputs. To simplify system fault reporting, the /FAULT_AUX[A/B] output pins may be connected together with the /FAULT_MAIN[A/B] output pins.
9 28	/FORCE_ONA /FORCE_ONB	Force On Enable Inputs [A/B]: These active-LOW, level-sensitive inputs with internal pull-up current (µA) to VSTBY[A] will turn on all three of the respective slot's outputs (+12V, +3.3V, and VAUX), while specifically defeating all protections on those supplies when asserted. This explicitly includes all overcurrent and short circuit protections and on-chip thermal protection for the VAUX[A/B] supplies. Additionally included are the UVLO protections for the +3.3V and +12V main supplies. The /FORCE_ON[A/B] pins do not disable UVLO protection for the VAUX[A/B] supplies. **These input pins are intended for diagnostic purposes only.** Asserting /FORCE_ON[A/B] will cause the respective slot's /PWRGD[A/B] and /DLY_PWRGD[A/B] output signals to be asserted LOW and cause the /FAULT_MAIN[A/B], the /FAULT_AUX[A/B], the /INT, and the SYSPWRGD output signals to their open-drain state.

Pin Description (cont.)

Pin Number	Pin Name	Pin Function
47 40	/DLY_PWRGDA /DLY_PWRGDB	/DLY_PWRGD[A/B] are open-drain, asserted active-LOW digital outputs that are normally connected by an external 10kΩ pull-up resistor (each) to VSTBY or to a local logic supply. Each output signal is asserted approximately 164 ms after their respective /PWRGD[A/B] output signals are asserted. The /DLY_PWRGD[A/B] output signals are de-asserted when the /PWRGD[A/B] outputs are de-asserted or upon a high-to-low transition on the ON[A/B] or AUXEN[A/B] inputs. There is approximately a 1-ms delay between the de-assertion of /DLY_PWRGD[A/B] and its corresponding /PWRGD[A/B] digital outputs. Please consult the /PWRGD[A/B] and /DLY_PWRGD[A/B] state diagrams within the Applications Information section for more detail.
46	SYSPWRGD	System Power is Good. SYSPWRGD is an open-drain, active-HIGH digital output that is normally connected by an external 10kΩ pull-up resistor to VSTBY or to a local logic supply. The SYSPWRGD output signal is asserted LOW when: (1) /CRSW[A] is asserted, ON[A] is asserted, /FORCE_ON_A is HIGH, and either MAIN 12V[A] or MAIN 3V[B] output is below its output Power-Good threshold; (2) /CRSW[B] is asserted, ON[B] is asserted, /FOCRE_ON_B is HIGH, and either MAIN 12V[B] or MAIN 3V[B] output is below its output Power-Good threshold; (3) /CRSW[A] is asserted, AUXEN[A] is asserted, /FORCE_ON_A is HIGH, and the VAUXA output is below its output Power-Good threshold; or (4) /CRSW[B] is asserted, AUXEN[B] is asserted, /FORCE_ON_B is HIGH, and VAUXB output is below its Power-Good threshold. For all other conditions, the SYSPWRGD output is open-drain. For more information with respect to the SYSPWRGD output signal, please consult the “Functional Description” section.
38	/INT	Interrupt Output: This open-drain, asserted active-LOW digital output is normally connected by an external 10kΩ resistor to VSTBY or a local logic supply. This signal is asserted whenever a power fault is detected. Checking the status of /FAULT_MAIN[A/B] or /FAULT_AUX[A/B] output will determine which slot and which rail caused the interrupt. To de-assert this signal output, please follow instructions provided on /FAULT_MAIN[A/B] and /FAULT_AUX[A/B] output pin descriptions.
17 33 45	AGND	3 Pins, IC Ground Connections: Tie directly to the system’s analog GND plane directly at the device.
7 18 19 20 30	NC	Reserved: Make no external connections to these pins.

Absolute Maximum Ratings[1]

12VIN[A/B], 12VSENSE[A/B], 12VGATE[A/B], 12VOUT[A/B] 14V
3VIN[A/B], 3VSENSE[A/B], 3VGATE[A/B], 3VOUT[A/B], VSTBY[A/B], VAUX[A/B] 7V
Digital Inputs
ON[A/B], AUXEN[A/B], /CRSW[A/B], /FORCE_ON[A/B] ..... –0.5V (min) to 3.6V (max)
CFILTER[A/B], RFILTER[A&B] 7V
Output Current
/PWRGD[A/B], /DLY_PWRGD[A/B] /FAULT_MAIN[A/B], SYSPWRGD, /INT, /FAULT_AUX[A/B] 10mA
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering)
Lead-Free Package (-xYTQ)
IR Reflow, Peak ..... 260°C +0°C/–5°C
Storage Temperature ..... –65°C to +150°C
ESD Rating[3]
Human Body Model 2kV
Machine Model 200V

Operating Ratings[2]

Supply Voltages
12VIN[A/B] ..... 11.0V to 13.0V
3VIN[A/B] ..... 3.0V to 3.6V
VSTBY[A/B] ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... 0°C to + 70°C
Junction Temperature (T_J) ..... 125°C
Package Thermal Resistance
TQFP (θ_{JA}) ..... 76.8°C/W

DC Electrical Characteristics[4]

$12V_{IN[A/B]}$ = 12V, $3V_{IN[A/B]}$ = 3.3V, $V_{STBY[A/B]}$ = 3.3V, T_A = 25°C, unless otherwise noted. **Bold** values specifications applies over the full operating temperature range from 0 °C ≤ T_A ≤ +70 °C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Control and Logic Sections						
I_{CC12} $I_{CC3.3}$ I_{CCSTBY}	Supply Current	/CRSW[A/B] = LOW /FORCE_ON[A/B] = HIGH AUX_EN[A/B], ON[A/B] = [L,H], [L,L]		1.8 0.6 2.8	**3** **2.5** **5**	mA mA mA
$V_{UVLO(12V)}$ $V_{UVLO(3V)}$ $V_{UVLO(STBY)}$	Undervoltage Lockout Thresholds 12VIN[A/B] 3VIN[A/B] VSTBY[A/B]	 $12V_{IN[A/B]}$ increasing $3V_{IN[A/B]}$ increasing $V_{STBY[A/B]}$ increasing	 **8** **2.2** **2.8**	 9 2.5 2.9	 **10** **2.75** **3.0**	 V V V
$V_{HYSSTBY}$	Undervoltage Lockout Hysteresis VSTBY[A/B]			50		mV
V_{HYSUV}	Undervoltage Lockout Hysteresis 12VIN[A/B], 3VIN[A/B]			180		mV
$V_{UVTH(12V)}$ $V_{UVTH(3V)}$	Power-Good Undervoltage Thresholds 12VOUT[A/B] 3VOUT[A/B]	12VOUT[A/B] decreasing 3VOUT[A/B] decreasing	**10.2** **2.7**	10.5 2.8	**10.8** **2.9**	V V
$V_{UVTH(VAUX)}$	Power-Good Undervoltage Threshold VAUX[A/B]	VAUX[A/B] decreasing I_{AUX} = 600mA	**2.7**	2.8	**2.9**	V
V_{HYSPG}	Power-Good Detect Hysteresis			30		mV
$V_{GATE(12V)}$	12VGATE[A/B] Voltage		**0**		**1.5**	V
$I_{GATE(12VSINK)}$	12VGATE[A/B] Pull-down Current	Start Cycle	**15**	25	**35**	µA
$I_{GATE(12VPULLUP)}$	12VGATE[A/B] Pull-up Current (Fault Off)	Any fault condition (VDD –VGATE) = 2.5V	**20**			mA

DC Electrical Characteristics[4]

$12V_{IN[A/B]}$ = 12V, $3V_{IN[A/B]}$ = 3.3V, $V_{STBY[A/B]}$ = 3.3V, T_A = 25°C, unless otherwise noted. **Bold** values specifications applies over the full operating temperature range from 0°C ≤ T_A ≤ +70°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{GATE(3V)}$	3VGATE[A/B] Voltage		**12VIN –1.5**		**12VIN**	V
$I_{GATE(3VCHARGE)}$	3VGATE[A/B] Charge Current	Start Cycle	**15**	25	**35**	µA
$I_{GATE(3VSINK)}$	3VGATE[A/B] Pull-down Current (Fault Off)	Any fault condition V_{3VGATE} = 2.5V	**65**			mA
V_{FILTER}	CFILTER[A/B] Threshold Voltage		**1.20**	1.25	**1.30**	V
I_{FILTER}	CFILTER[A/B] Charging Current	$V_{12VIN} – V_{12VSENSE} > V_{THILIMIT}$ and/or $V_{3VIN} – V_{3VSENSE} > V_{THILIMIT}$	**1.80**	2.5	**5.0**	µA
$V_{THLIMIT}$	Current Limit Threshold Voltages 12VIN[A/B] Supplies 3VIN[A/B] Supplies	 $V_{12VIN} – V_{12VSENSE}$ $V_{3VIN} – V_{3VSENSE}$	 **45** **45**	 50 50	 **57** **57**	 mV mV
V_{THFAST}	12VOUT[A/B] & 3VOUT[A/B] Fast-Trip Threshold Voltages	$V_{12VIN} – V_{12VSENSE}$ $V_{3VIN} – V_{3VSENSE}$ MIC2341-2YTQ Only	**90**	100	**110**	mV
V_{THFAST}	12VOUT[A/B] & 3VOUT[A/B] Fast-Trip Threshold Voltages	$V_{12VIN} – V_{12VSENSE}$ MIC2341-2YTQ $V_{3VIN} – V_{3VSENSE}$ MIC2341-3YTQ MIC2341-5YTQ	**90** **135**	100 150 Dis-abled	**110** **165**	mV mV
$I_{12VSENSE[A/B]}$	12VSENSE[A/B] Input Current			0.35	**1**	µA
$I_{3VSENSE[A/B]}$	3VSENSE[A/B] Input Current			0.35	**1**	µA
$I_{LKG,OFF(12VIN[A/B]}$	12VIN[A/B] Input Leakage Current	VSTBY = VSTBY[A/B] = +3.3V; 12VIN[A/B] = OFF; 3VIN[A/B] = OFF			**1**	µA
$I_{LKG,OFF(3VIN[A/B]}$	3VIN[A/B] Input Leakage Current	VSTBY = VSTBY[A/B] = +3.3V; 12VIN[A/B] = OFF; 3VIN[A/B] = OFF			**1**	µA
V_{IL}	LOW-Level Digital Input Voltage ON[A/B], AUXEN[A/B], /CRSW[A/B], /FORCE_ON[A/B]				**0.8**	V
V_{IH}	HIGH-Level Digital Input Voltage ON[A/B], AUXEN[A/B], /CRSW[A/B], /FORCE_ON[A/B]		**2.1**		**3.6**	V
V_{OL}	LOW-Level Digital Output Voltage /FAULT_AUX[A/B], /INT, /FAULT_MAIN[A/B], /PWRGD[A/B] ,SYSPWRGD, /DLY_PWRGD	I_{OL} = 3 mA			**0.4**	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LKG(OFF)}$	Digital Output Off-State Leakage Current /FAULT_AUX[A/B], /INT, /FAULT_MAIN[A/B], /PWRGD[A/B], SYSPWRGD /DLY_PWRGD[A/B]				**5**	µA
R_{PULLUP}	Internal Pull-up Resistors to VSTBY[A] [/CRSW[A/B],ON[A/B], AUXEN[A/B]]	VSTBY[A/B] = +3.3V		45		kΩ
I_{PULLUP}	Internal Pull-up Current to VSTBY[A] [/FORCE_ON[A/B]]	VSTBY[A/B] = +3.3V		60		µA
$R_{DS(AUX)}$	Internal VAUX[A/B] Power MOSFET Channel Resistance	I_{DS} = 375 mA; T_J = 100 °C			**0.4**	Ω
$V_{OFF(12VOUT[A/B])}$	12VOUT[A/B] Off-state Output Offset Voltage	ON[A/B] = LOW, 12VOUT[A/B] = OFF, T_J = 100 °C			**50**	mV
$V_{OFF(3VOUT[A/B])}$	3VOUT[A/B] Off-state Output Offset Voltage	ON[A/B] = LOW, 3VOUT[A/B] = OFF, T_J = 100 °C			**50**	mV
$V_{OFF(VAUX[A/B])}$	VAUX[A/B] Off-state Output Offset Voltage	AUXEN[A/B] = LOW, VAUX[A/B] = OFF, T_J = 100 °C			**50**	mV
T_{OV}	Overtemperature Shutdown and Reset Thresholds with Overcurrent on Slot[5]	T_J increasing, each slot T_J decreasing, each slot		140 130		°C °C
	Overtemperature Shutdown and Reset Thresholds, All Other Conditions (All Outputs will Latch OFF) [5]	T_J increasing, both slots T_J decreasing, both slots		160 150		°C °C
$I_{AUX(THRESH)}$	Auxiliary Output Current Limit Threshold (Figure 4)	Current which must be drawn from VAUX to register as a fault		0.84		A
$I_{SC(TRAN)}$	Maximum Transient Short Circuit Current	VAUX[A/B] Enabled, then Grounded	$I_{MAX} = \frac{V_{STBY[A/B]}}{R_{DS(AUX)}}$			A
$I_{LIM(AUX)}$	Regulated Current after Transient	From end of $I_{SC(TRAN)}$ to CFILTER time-out	**0.375**	0.7	**0.975**	A
$R_{DIS(12V)}$ $R_{DIS(3V)}$ $R_{DIS(VAUX)}$	Output Discharge Resistance 12VOUT[A/B] 3VOUT[A/B] 3VAUX[A/B]	 $12V_{OUT[A/B]}$ = 6.0V $3V_{OUT[A/B]}$ = 1.65V $3V_{AUX[A/B]}$ = 1.65V		 160 0 150 430		 Ω Ω Ω

AC Electrical Characteristics[4]

$12V_{IN[A/B]}$ = 12V, $3V_{IN[A/B]}$ = 3.3V, $V_{STBY[A/B]}$ = 3.3V, T_A = 25°C, unless otherwise noted. **Bold** values specifications applies over the full operating temperature range from 0°C ≤ T_A ≤ +70°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{OFF(12V)}$	12V Current Limit Response Time [5] (Figure 2)	MIC2341-2YTQ CGATE[A/B] = 25pF $V_{IN} - V_{SENSE}$ = 140mV		1	**2.0**	µs
$t_{OFF(3V)}$	3.3V Current Limit Response Time [5] (Figure 3)	MIC2341-2YTQ CGATE[A/B] = 25pF $V_{IN} - V_{SENSE}$ = 140mV		1	**2.0**	µs
$t_{SC(TRAN)}$	VAUX[A/B] Current Limit Response Time (Figure 5)	VAUX[A/B] = 0V, VSTBY[A/B] = +3.3V		2.5	**5**	µs
$t_{PROP(12VFAULT)}$	Delay from 12VOUT[A/B] Overcurrent Limit to /FAULT_MAIN[A/B] = LOW [5]	MIC2341-2YTQ CFILTER[A/B] = OPEN $V_{IN} - V_{SENSE}$ = 140mV			**1**	µs
$t_{PROP(3VFAULT)}$	Delay from 3VOUTA/B] Overcurrent Limit to /FAULT_MAIN[A/B] = LOW [5]	MIC2341-2YTQ CFILTER[A/B] = OPEN $V_{IN} - V_{SENSE}$ = 140mV			**2**	µs
$t_{PROP(VAUXFAULT)}$	Delay on VAUX[A/B] Overcurrent from CFILTER "time out" ($V_{CFILTER}$ = V_{FILTER}) to /FAULT_AUX[A/B] = LOW [5]	MIC2341-2YTQ limit to /FAULT_AUX[A/B] output CFILTER[A/B] = 50pF V_{AUX} Output Grounded		10		µs
t_{LPW}	ON[A/B], AUXEN[A/B] Low Pulse Width to Reset Output Upon Fault Removal[5]	ON[A/B], AUXEN[A/B] = HIGH-to-LOW-HIGH	**200**			ns
t_{INTCLK}	Digital Filter (Internal Clock) Period		**5**		**15**	µs
t_{POR}	MIC2341 Power-On Reset Time after VSTBY[A/B] becomes valid [5]		**80**		**255**	µs
$t_{/CRSW[A/B]}$	/CRSW[A/B] Debounce Delay Time		**5.10**		**15.85**	ms
$t_{/PWRGD}$	/PWRGD[A/B] De-assertion Delay Time	ON[A/B] or AUXEN[A/B] High-to-Low Transition	**640**		**2040**	µs
$t_{/DLY\_PWRGD}$	/DLY_PWRGD[A/B] Assertion Delay after /PWRGD[A/B] Assertion	ON[A/B], AUXEN[A/B] = HIGH, 12VOUT[A/B], 3VOUT[A/B], VAUX[A/B] = VALID;	**80**		**241**	ms
t_{DFLT}	Internal Primary OC Detector Response Time (MIC2341 and MIC2341R)	CFILTER[A/B] = GND	**20.5**	41	**63.5**	ms
$t_{AUTO\ RETRY}$	Auto Retry Period (MIC2341R only)		**410**		**1236**	ms

Notes:

1. Exceeding measurements given within the "Absolute Maximum Ratings" section may damage the device.
2. The device is not guaranteed to function outside of the measurements given in the "Operating Ratings" section.
3. These devices are ESD sensitive. Employ proper handling precautions. The HBM is 1.5kΩ in series with 100pF.
4. Specifications apply to packaged product only.
5. Parameters guaranteed by design, not subject to test.

Timing Diagrams

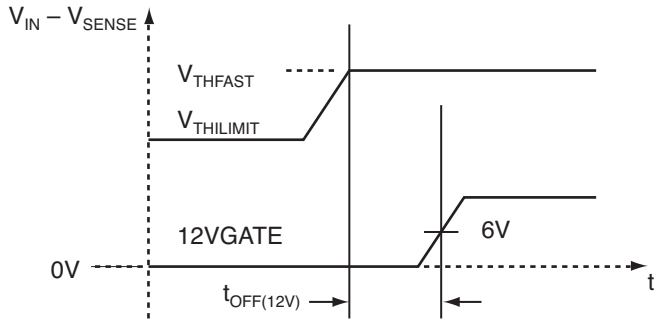


Figure 1. 12V Current Limit Response Timing

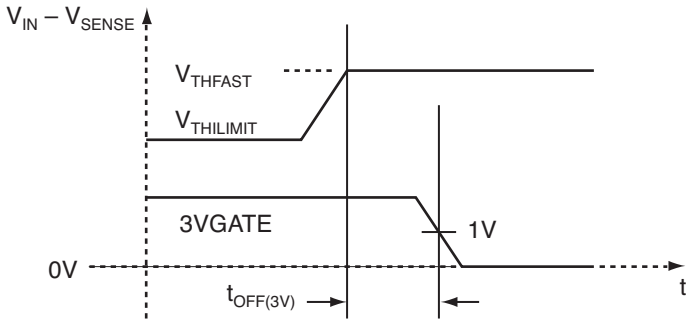


Figure 2. 3V Current Limit Response Timing

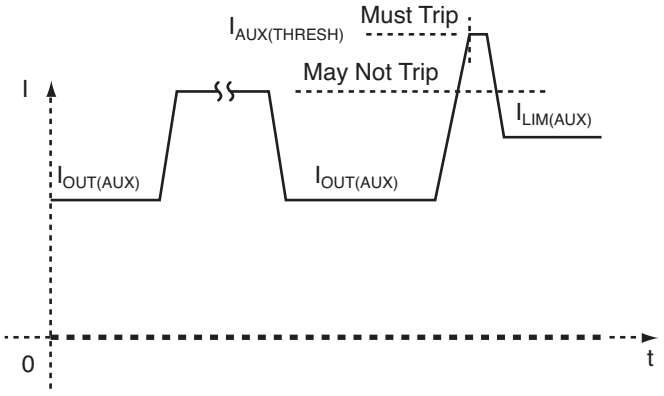


Figure 3. VAUX Current Limit Threshold

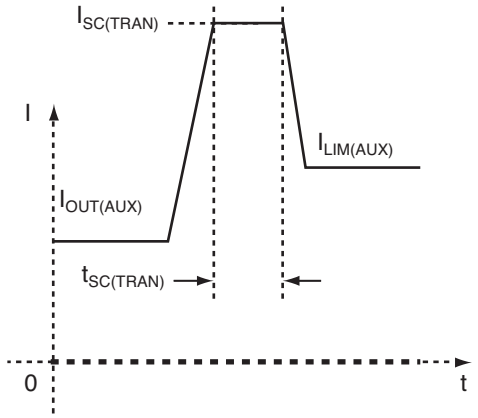
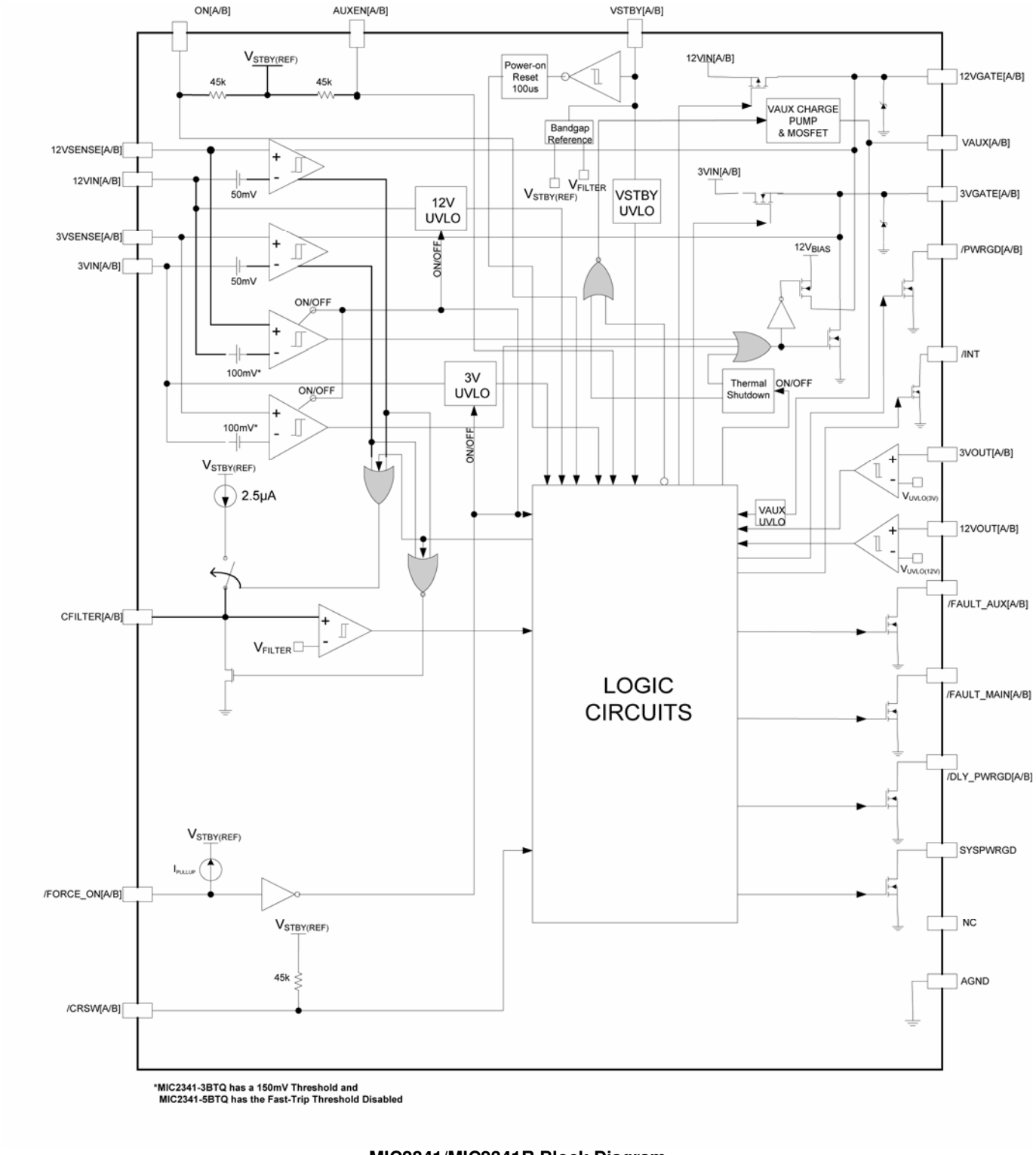


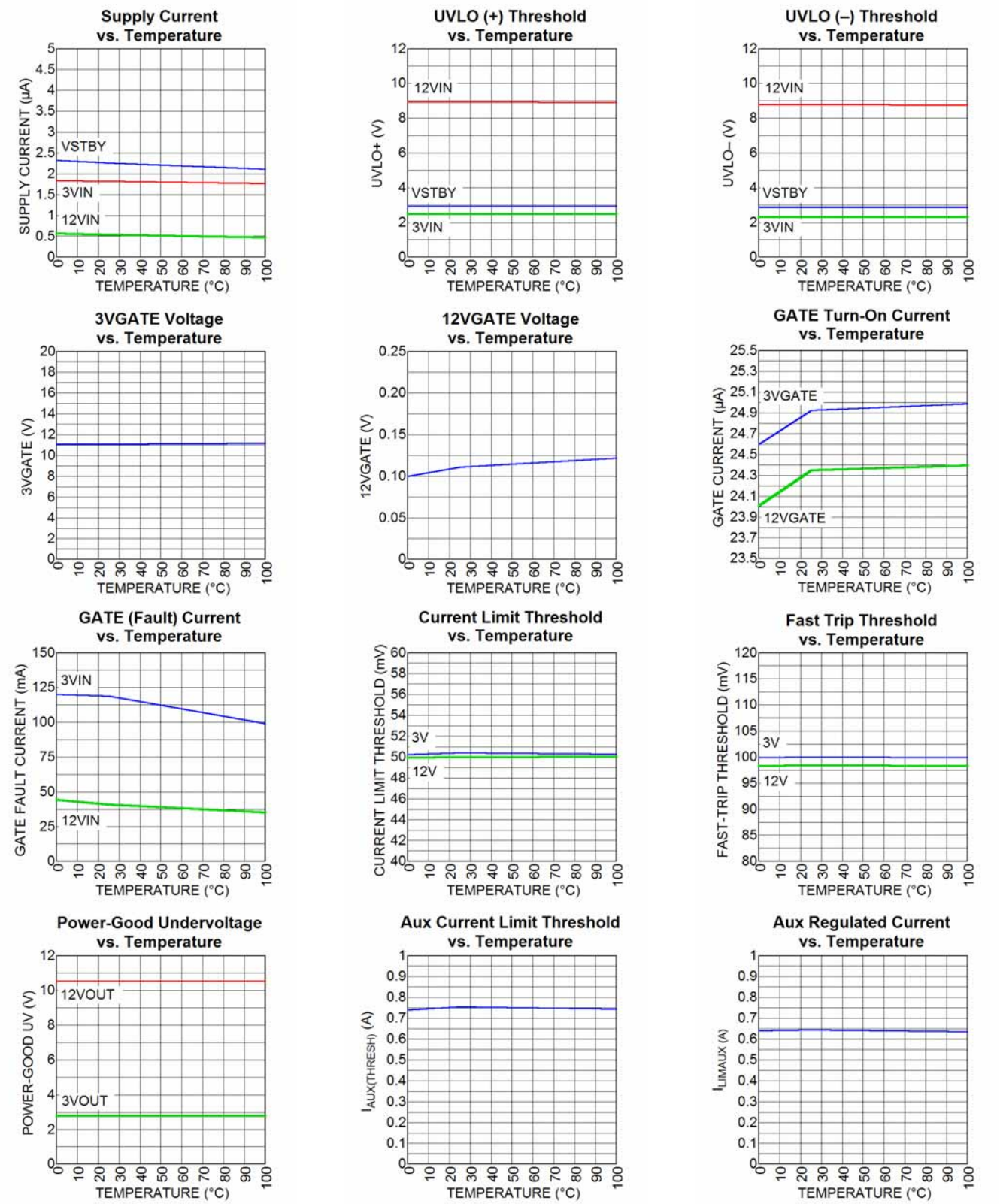
Figure 4. VAUX Current Limit Response Timing

Functional Diagram

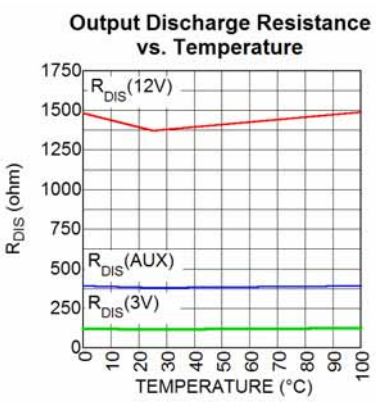


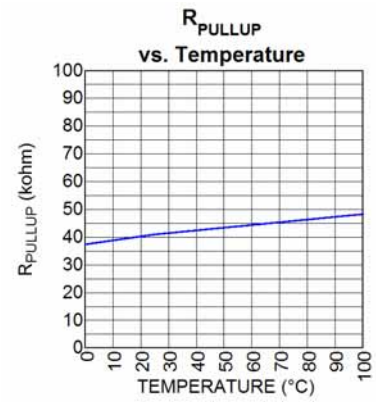
MIC2341/MIC2341R Block Diagram

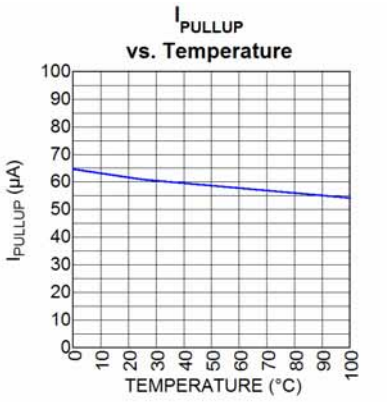
Typical Characteristics

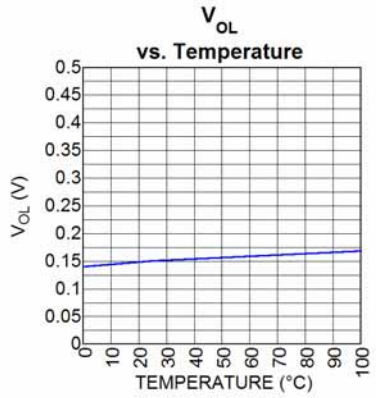


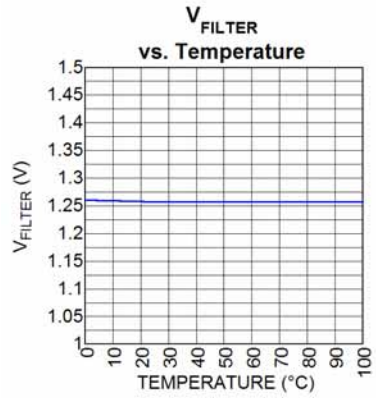
Typical Characteristics (cont.)

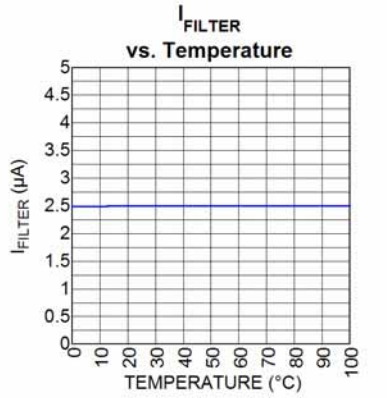


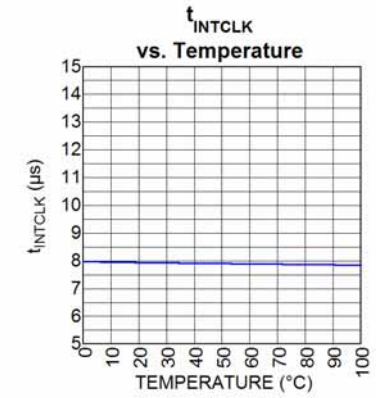


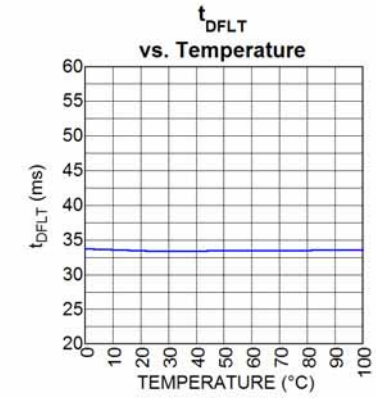


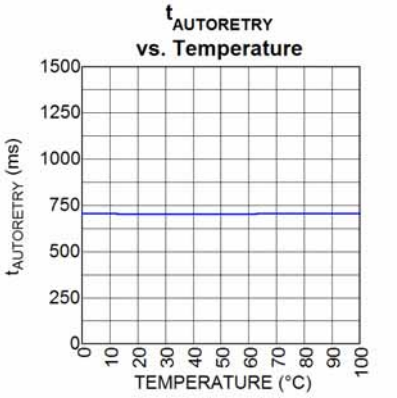












Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot-plugged"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. This transient inrush current can cause the system's supply voltages to temporarily go out of regulation, causing data loss or system lock−up. In more extreme cases, the transients occurring during a hot-plug event may cause permanent damage to connectors or on-board components.

The MIC2341 addresses these issues by limiting the inrush currents to the load (PCI Express Board), and thereby controlling the rate at which the load's circuits turn-on. In addition to this inrush current control, the MIC2341 offers input and output voltage supervisory functions and current limiting to provide robust protection for both the system and circuit board.

System Interface

The MIC2341 employs a hardware system interface that includes: ON[A/B], AUXEN[A/B], /CRSW[A/B], /FAULT_MAIN[A/B], /FAULT_AUX[A/B], /PWRGD[A/B], /INT, and SYSPWRGD.

Power-On Reset

VSTBY[A/B] are the main power supply for the MIC2341's internal logic circuits and state machines . VSTBY[A/B] is required for proper operation of the MIC2341's internal logic circuitry and must be applied at all times. A Power-On Reset (POR) cycle is initiated after VSTBY[A/B] is higher than its $V_{UVLO(STBY)}$ threshold voltage and remains valid at that voltage for at least 80µs. All internal logic flags are cleared after POR. If the VSTBY[A/B] pin voltages are cycled ON-OFF-ON, a new power-on-reset cycle is initiated. V_{STBY} must be the first supply input applied followed by the MAIN supply inputs of $12V_{IN}$ and $3V_{IN}$. During t_{POR}, all outputs remain off. In most applications, the total POR interval will consist of the time required to charge the V_{STBY} input (bypass) capacitance to the UVLO threshold plus the internal t_{POR} delay time. The following equation is used to approximate the total POR interval:

$$t_{POR\_TOTAL(\mu s)} = \left\{ \left[\frac{\left(C_{STBY(\mu F)} \times V_{ULVO(STBY)}\right)}{I_{CHARGE(STBY)(A)}} \right] \times 10^{-6} \right\} + t_{POR(\mu s)}$$

where C_{STBY} is the V_{STBY} input bulk bypass capacitance and $I_{CHARGE(STBY)}$ is the current supplied by the V_{STBY} source to charge the capacitance.

+12VOUT[A/B] and +3VOUT[A/B] Start-Up Cycles

All four of the MIC2341's +12V and +3V gate drive circuits have been designed to drive the gates of external power MOSFETs. The +12V gate drive circuits have been designed to drive P-channel MOSFETs and the +3V gate drive circuits are intended to drive N-channel MOSFETs. A list of recommended N- and P-channel power MOSFETs suited for use with the MIC2341 and PCI Express applications can be found in Table 2.

These gate drive circuits have also been designed to limit inrush current in one of two modes: (1) by controlling the 12VGATE[A/B] or the 3VGATE[A/B] voltage slew rates ($dV_{12GATE[A/B]}/dt$ or $dV_{3GATE[A/B]}/dt$) or (2) by actively limiting the inrush current, thereby charging the corresponding load capacitance in current limit. The mode that the MIC2341 automatically enters is dependent upon the magnitude of the inrush current and the magnitude of the load capacitance at 12VOUT[A/B] and 3VOUT[A/B].

Mode 1: [12V/3V]GATE[A/B] Slew Rate Control

When a slot's MAIN supply voltages (12VOUT[A/B] and 3VOUT[A/B]) are OFF, each of the 12VGATE[A/B] pins is held at 12VIN[A/B] by an internal pull-up transistor. Similarly, each 3VGATE[A/B] pin is internally held at AGND. When the MAIN supply voltages are enabled by a low-to-high transition on the ON[A/B] input pins (recall that the /CRSW[A/B] inputs must also be asserted), the 12VGATE[A/B] and the 3VGATE[A/B] pins are each connected to an internal constant current supply, typically 25 µA each. At each 12VGATE[A/B] pin, this constant current supply is a current sink; at each 3VGATE[A/B] pin, the supply is a current source. For applications where the inrush current is controlled by the 12VGATE[A/B] voltage rate of change, an expression for the circuit's behavior is given by the following equation:

$$\frac{dV_{12VGATE[A/B]}}{dt} = \frac{I_{GATE(12VGATE)}}{C_{ISSP}} = \frac{25\mu A}{C_{ISSP}}$$

where C_{ISSP} = P-channel power MOSFET gate input capacitance.

For example, a Si4435BDY (a 30-V P-channel power MOSFET) exhibits an approximate C_{ISSP} of 1700pF at V_{DS} = 12V. The 12VGATE[A/B] pin voltage rate-of-change (slew rate) would be:

$$\frac{dV_{12VGATE[A/B]}}{dt} = \frac{I_{GATE(12VSNK)}}{C_{ISSP}} = \frac{25\mu A}{1700pF} = 14.7\frac{V}{ms}$$

The 12VOUT[A/B] inrush current to the load while the 12VGATE[A/B] voltage is ramping is dependent on $C_{LOAD(12VOUT[A/B])}$ and C_{ISSP}. An expression for the 12VOUT[A/B] inrush current is given by:

$$I_{INRUSH(12VOUT[A/B])} = \frac{dV_{12VGATE[A/B]}}{dt} \times C_{LOAD(12VOUT[A/B])}$$

$$= I_{GATE(12VSNK)} \times \frac{C_{LOAD(12VOUT[A/B])}}{C_{ISSP}}$$

For the same p-channel power MOSFET in the previous example, if C_{ISSP} = 1700pF and $C_{LOAD(12VOUT[A/B])}$ = 100µF, the 12VOUT[A/B] inrush current charging this load capacitance is:

$$I_{INRUSH(12VOUT[A/B])} = 25\mu A \times \frac{100\mu F}{1700pF} = 1.47A$$

Calculating the 12VOUT[A/B] voltage rate-of-change for a given capacitive load can be determined by the following expression:

$$\frac{dV_{12VOUT[A/B]}}{dt} = \frac{I_{INRUSH(12VOUT[A/B])}}{C_{LOAD(12VOUT[A/B])}}$$

and, using the same quantities in the current example, is given by:

$$\frac{dV_{12VOUT[A/B]}}{dt} = \frac{1.47\ A}{100\ \mu F} = 14.7\ \frac{V}{ms}$$

To determine (to first-order) the time point at which the 12VOUT[A/B] voltage crosses its corresponding output "Power Good" threshold, the following equation can be used:

$$t_{PWRGD(12VOUT[A/B])} = \frac{\left(V_{UVTH(12V)} + V_{HYSPG}\right)}{\frac{dV_{12VOUT[A/B]}}{dt}} = \frac{10.53V}{14.7\frac{V}{ms}} \approx 0.72ms$$

To determine 3VGATE[A/B] pin voltage slew rates, inrush currents, 3VOUT[A/B] output voltage slew rates, and time to assert its corresponding internal "Power Good" flag into capacitive loads connected to 3VOUT[A/B], simple computations can be made using the same equations by substituting $I_{GATE(3VCHARGE)}$ for $I_{GATE(12VSINK)}$, C_{ISSN} (the input gate capacitance of an N-channel power MOSFET) for C_{ISSP}, $C_{LOAD(3VOUT[A/B])}$ for $C_{LOAD(12VOUT[A/B])}$, $I_{INRUSH(3VOUT[A/B])}$ for $I_{INRUSH(12VOUT[A/B])}$, and $V_{UVTH(3V)}$ for $V_{UVTH(12V)}$.

For example, if a Si4420BDY n-channel power MOSFET is used with the MIC2341 to control inrush currents at 3VOUT[A/B], its C_{ISSN} is approximately 4100pF at V_{DS} = 3V. The 3VGATE[A/B] pin voltage rate of change is given by:

$$\frac{dV_{3VGATE[A/B]}}{dt} = \frac{I_{GATE(3VCHARGE)}}{C_{ISSN}} = \frac{25\mu5}{4100pF} = 6.1\frac{V}{ms}$$

Assuming a 300-µF capacitive load, the 3VOUT[A/B] inrush current charging this load capacitance is given by:

$$I_{INRUSH(3VOUT[A/B])} = 25\mu5 \times \frac{300\mu0}{4100pF} = 1.82\ A$$

The 3VOUT[A/B] output voltage slew rate is given by:

$$\frac{dV_{3VOUT[A/B]}}{dt} = \frac{1.82\ A}{300\ \mu F} \approx 6.1\frac{V}{ms}$$

and the time to assert the internal 3VOUT[A/B] "Power Good" flag is given by:

$$t_{PWRGD(3VOUT[A/B])} = \frac{\left(V_{UVTH(3V)} + V_{HYSPG}\right)}{\frac{dV_{3VOUT[A/B]}}{dt}} = \frac{2.77V}{6.1\frac{V}{ms}} \approx 0.45\ ms$$

Mode 2: Charging 12VOUT and 3VOUT Capacitive Loads in Current Limit

In x4 and x8 PCI Express applications, capacitive loads at 12VOUT[A/B] and 3VOUT[A/B] can be as large as 1000µF. As a result, the inrush load charging currents at start-up can be large enough to cause a voltage drop across the external sense resistor larger than 50mV. In these applications, internal servo circuits at 12VGATE[A/B] and 3VGATE[A/B] modulate the drive to the gates of their corresponding power MOSFETs to regulate the load current to:

$$I_{LIMIT(12VOUT[A/B])} = \frac{V_{THLIMIT}}{R_{12VSENSE[A/B]}} = \frac{50\ mV}{R_{12VSENSE[A/B]}}$$

In the typical application circuit, the external sense resistor connected between 12VIN[A/B] and 12VSENSE[A/B] pins was selected to be 20mΩ. The regulated current charging the load capacitance at 12VOUT[A/B] is given by:

$$I_{LIMIT(12VOUT[A/B])} = \frac{50\ mV}{20\ m\Omega} = 2.5\ A$$

Once current-regulation control is activated, the circuit breaker's t_{FLT} timer is also activated to protect the external power MOSFET against potentially excessive power dissipation. For additional information on this timer and the MIC2341's circuit breaker operation, please consult the section labeled "Circuit Breaker Function." The output voltage rate of change at 12VOUT[A/B] during current limit charging into a 1000µF capacitive load is given by:

$$\frac{dV_{12VOUT[A/B]}}{dt} = \frac{I_{LIMIT(12VOUT[A/B])}}{C_{LOAD(12VOUT[A/B])}} = \frac{2.5\ A}{1000\ \mu F} = 2.5\frac{V}{ms}$$

In this fashion, the inrush current is controlled and the load capacitance is charged up slowly during the start-up cycle. The gate drive circuits will maintain control of the inrush current until the 12VOUT[A/B] or 3VOUT[A/B] voltages have reached their corresponding "Power Good" thresholds ($V_{UVTH(12V)[A/B]}$ or $V_{UVTH(3V)[A/B]}$, respectively) at which time the inrush current approaches its nominal steady-state level, the voltage across the external sense resistor drops below the circuit breaker's $V_{THLIMIT}$ threshold, and the corresponding internal "Power-is-Good" flag is asserted. For the 12VOUT[A/B] example, its internal "Power-is-Good" flag is asserted at:

$$t_{PWRGD(12VOUT[A/B])} = \frac{\left(V_{UVTH(12V)} + V_{HYSPG}\right)}{\frac{dV_{12VOUT[A/B]}}{dt}} = \frac{10.53V}{2.5\frac{V}{ms}} \approx 4.2\ ms$$

Calculating the current limit for charging the 3VOUT[A/B] load capacitance, the output voltage slew rate at 3VOUT[A/B], and when the internal 3VOUT[A/B] "Power

Good" flag is asserted is a simple matter of substituting $R_{3VSENSE[A/B]}$ for $R_{12VSENSE[A/B]}$, $C_{LOAD(3VOUT[A/B])}$ for $C_{LOAD(12VOUT[A/B])}$, and $V_{UVTH(3V)}$ for $V_{UVTH(12V)}$.

Even though individual internal "Power Good" flags may be asserted, the conditions under which the MIC2341's external /PWRGD[A/B] and /DLY_PWRGD[A/B] digital outputs are asserted is described in the section labeled "/PWRGD[A/B] and /DLY_PWRGD[A/B] Digital Outputs."

Power-Down Cycle

When a slot is turned off, resistors internal to the MIC2341/MIC2341R are connected to each of the outputs to provide a discharge path for capacitors connected to the part's outputs. The nominal output discharge resistance values for each rail are found in the "Electrical Characteristics" table.

Use of an External Gate Capacitor to Control Inrush Current Profile

In PCI Express applications where the 12VOUT[A/B] and the 3VOUT[A/B] maximum load capacitance is 1000 µF (2000uF on the 12V rail for x16 modules), the PCI Express power control specification clearly states that any inrush current rate-of-change shall not exceed 0.1A/µs. This situation is most likely to happen when the controller is charging these large load capacitances in current limit. Under these circumstances, it may be preferable to modify the gate drive by using GATE voltage control instead of active current regulation to charge the load. As shown in Figure 5, an external capacitor connected from each 3VGATE[A/B] to AGND can be used. For the 12VGATE[A/B], an optional Miller capacitor (Gate-Drain) can be used in conjunction with a Gate-Source capacitor to form a Miller integrator to control the output slew rate. The optimal capacitor value is best determined empirically as the magnitude of the inrush current slew rate is a function of the power MOSFET's input capacitance (C_{ISS}), the load capacitance ($C_{LOAD(3VOUT[A/B])}$ and $C_{LOAD(12VOUT[A/B])}$), and the current-limit sense resistor ($R_{3VSENSE[A/B]}$ and $R_{12VSENSE[A/B]}$). Using an external capacitor to control the gate voltage slew rate for large load capacitance may affect the MIC2341/MIC2341R's specified system turn-on and turn-off time performance.

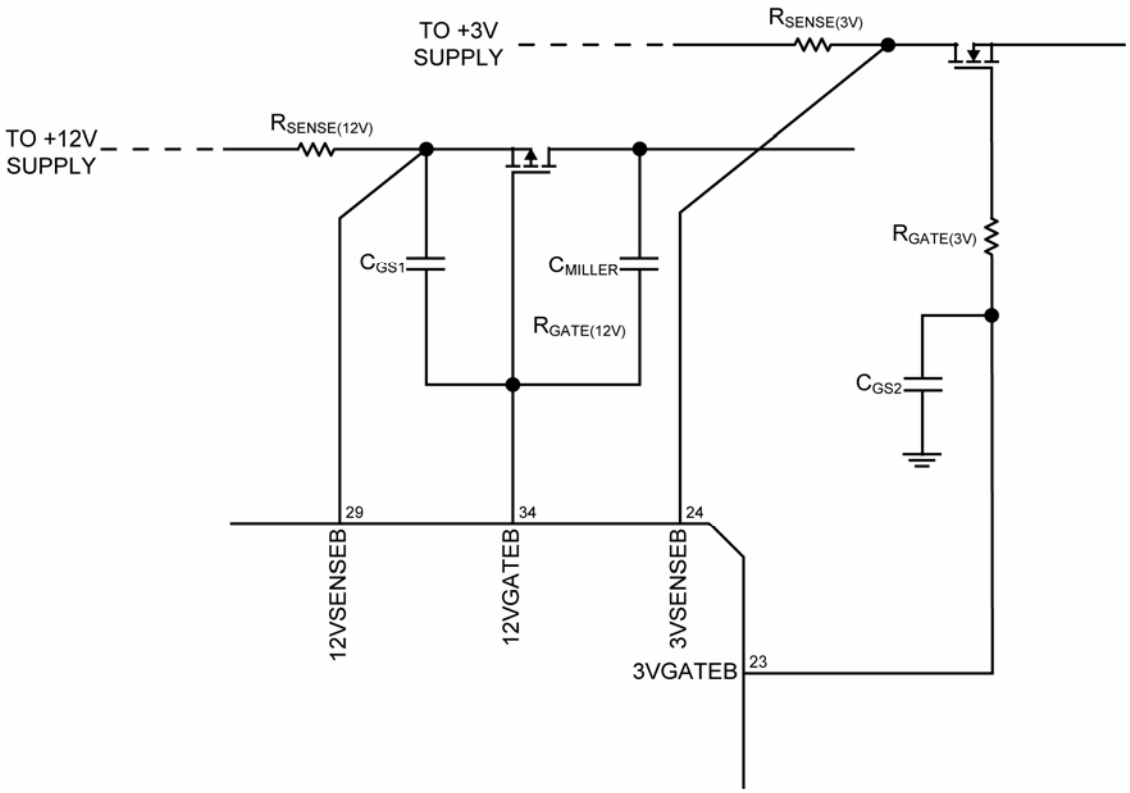


Figure 5. (Optional) External Gate Slew Control Components

Standby Mode

Standby mode is entered when one or more of the MAIN supply inputs (12VIN and/or 3VIN) are below its respective UVLO threshold or OFF. The MIC2341 also supplies 3.3V auxiliary outputs (VAUX[A/B]), satisfying PCI Express specifications. These outputs are fed via the VSTBY[A/B] input pins and controlled by the AUXEN[A/B] input pins. These outputs are independent of the MAIN outputs (12VIN[A/B] and 3VIN[A/B]). Should the MAIN supply inputs move below their respective UVLO thresholds, VAUX[A/B] will still function as long as VSTBY[A/B] is present. Prior to standby mode, ONA and ONB inputs should be de-asserted or the MIC2341 will assert the /FAULT_MAIN[A/B] and /INT output signals, if an undervoltage condition on the MAIN supply inputs is detected.

Circuit Breaker Function

The MIC2341 provides an electronic circuit breaker function that protects against excessive loads, such as short circuits, at each supply. When the current from one or more of a slot's MAIN outputs exceeds the current limit threshold (I_{LIM} = 50mV/R_{SENSE}) for a duration greater than t_{FLT}, the circuit breaker is tripped and both MAIN supplies (all outputs except VAUX[A/B]) are shut off. Should the load current cause a MAIN output's V_{SENSE} to exceed V_{THFAST}, the outputs are immediately shut off with no delay. Undervoltage conditions on the MAIN supply inputs also trip the circuit breaker, but only when the MAIN outputs are enabled (to signal a supply input brown-out condition).

The VAUX[A/B] outputs have a different circuit-breaker function. The VAUX[A/B] circuit breakers do not incorporate a fast-trip detector, instead they regulate the output current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to an overcurrent on VAUX[A/B] when the fault timer expires. This use of the t_{FLT} timer prevents the circuit breaker from tripping prematurely due to brief current transients.

Following a fault condition, the outputs can be turned on again by toggling the ON[A/B] input high-low-high (if the fault occurred on one of the MAIN outputs), or similarly toggling the AUXEN[A/B] input (if the fault occurred on the AUX outputs), or by cycling both ON[A/B] and AUXEN[A/B] (if faults occurred on both the MAIN and AUX outputs). When the circuit breaker trips, the corresponding /FAULT_MAIN[A/B] or /FAULT_AUX[A/B] will be asserted. At the same time, /INT will be asserted. Note that /INT is only de-asserted by applying a high-to-low transition on the corresponding slot's ON[A/B] or AUXEN[A/B] input.

The response time (t_{FLT}) of the MIC2341's primary overcurrent detector is set by external capacitors at the CFILTER[A/B] pins to GND. For Slot A, CFILTER[A] is located at Pin 2; for Slot B, CFILTER[B] is located at Pin 35. For a given response time, the value for $C_{FILTER[A/B]}$ is given by:

$$C_{FILTER[A/B]}(\mu F) = \frac{t_{FLT[A/B]}(ms) \times I_{FILTER}(\mu A)}{V_{FILTER}(V) \times 10^3}$$

where $t_{FLT[A/B]}$ is the desired response time and quantities I_{FILTER} and V_{FILTER} are specified in the MIC2341's "Electrical Characteristics" table.

Digital Filter and Auto-Retry Functions

New timers have been incorporated for additional protection for overcurrent situations. In many applications, external power MOSFETs used at 12VOUT[A/B] and at 3VOUT[A/B] have been damaged during initial start-up and overcurrent conditions because the response time of the primary OC detectors was set too long (that is, an incorrect value for CFILTER[A/B] was used). In these products, a digital filter delay counter is introduced, and is internally set to a typical delay time of 40 ms. As shown in the typical applications circuit of the MIC2341, an external capacitor from CFILTER[A/B] to ground is used to set the response time of the primary overcurrent detectors to t_{FLT}. At the time a large inrush current causes the primary OC detector to sense an overcurrent condition, a CFILTER[A/B] charge-up sequence is initiated. At the same time, the MIC2341's digital filter delay counter is also initiated and commences a count-up to 40 ms. The MIC2341's internal logic circuits have been designed to trip the circuit breaker after t_{FLT} or t_{DFLT}, whichever delay is smaller. If the overcurrent condition causes the electronic circuit breaker to latch off and thereby asserting a FAULT condition, the MIC2341 remains latched-off awaiting system intervention (by toggling ON[A/B] and/or AUXEN[A/B] and/or cycling the input power supplies). Internal to the MIC2341R only, a second, or auto-retry, delay counter is initiated and commences a count-up to approximately 820 ms to allow the external power MOSFET to cool before attempting another power-up sequence. Figure 6 illustrates the filter responses during an overcurrent fault.

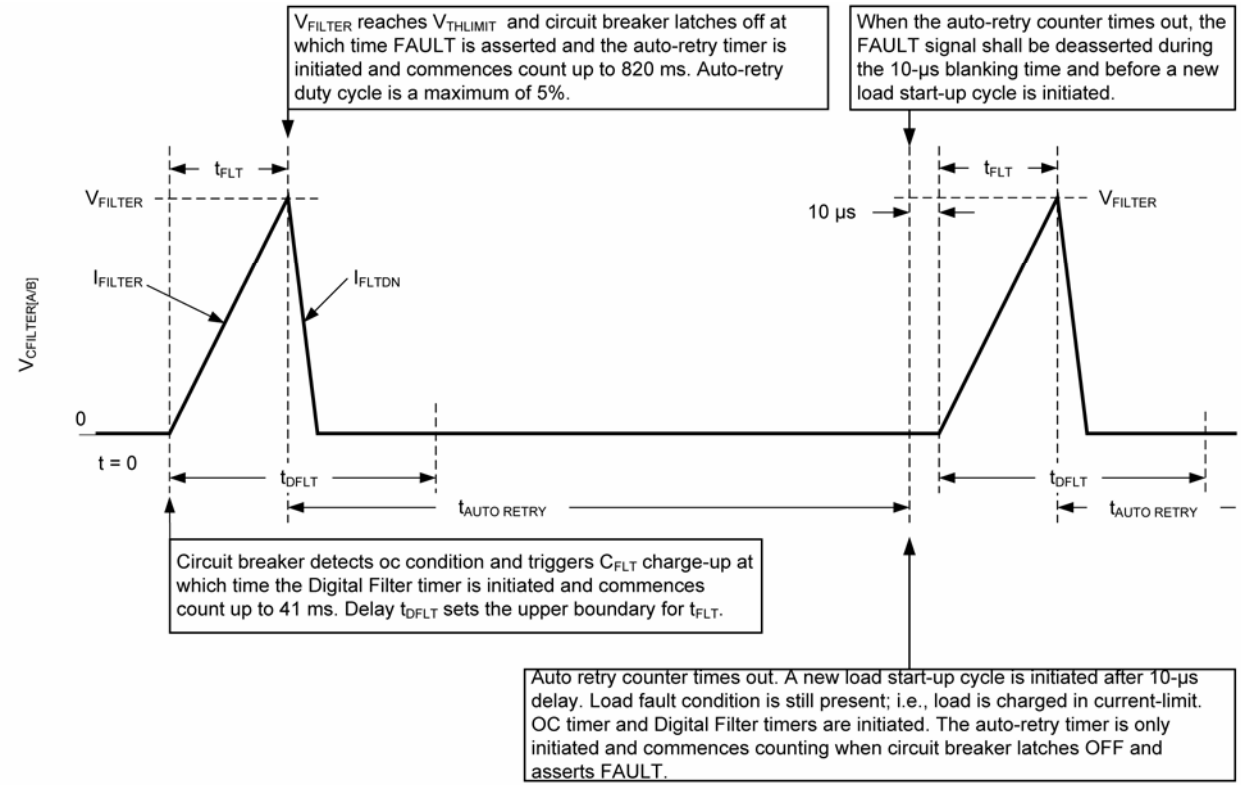


Figure 6. MIC2341R Auto-Retry Timing Diagram and Operation

In very cost-sensitive applications, the system design engineer can save the cost of the (2) external CFILTER[A/B] capacitors by using only the digital filter and/or the auto-retry delay counters. This mode is automatically invoked by connecting the MIC2341 or the MIC2341R's CFILTER[A/B] pins directly to AGND. In this configuration, the primary OC detectors' response time t_{FLT} is equal to t_{DFLT} (or 40ms as above) In Figure 7, the gate drive circuits have taken control and regulate the inrush current to charge the load capacitances in current limit. Once the internal digital filter delay counter terminates, the circuit breaker trips off. As in the previous case, the MIC2341 latches off and the MIC2341R initiates the auto-retry delay counter to count up to 820ms before attempting another power-up cycle.

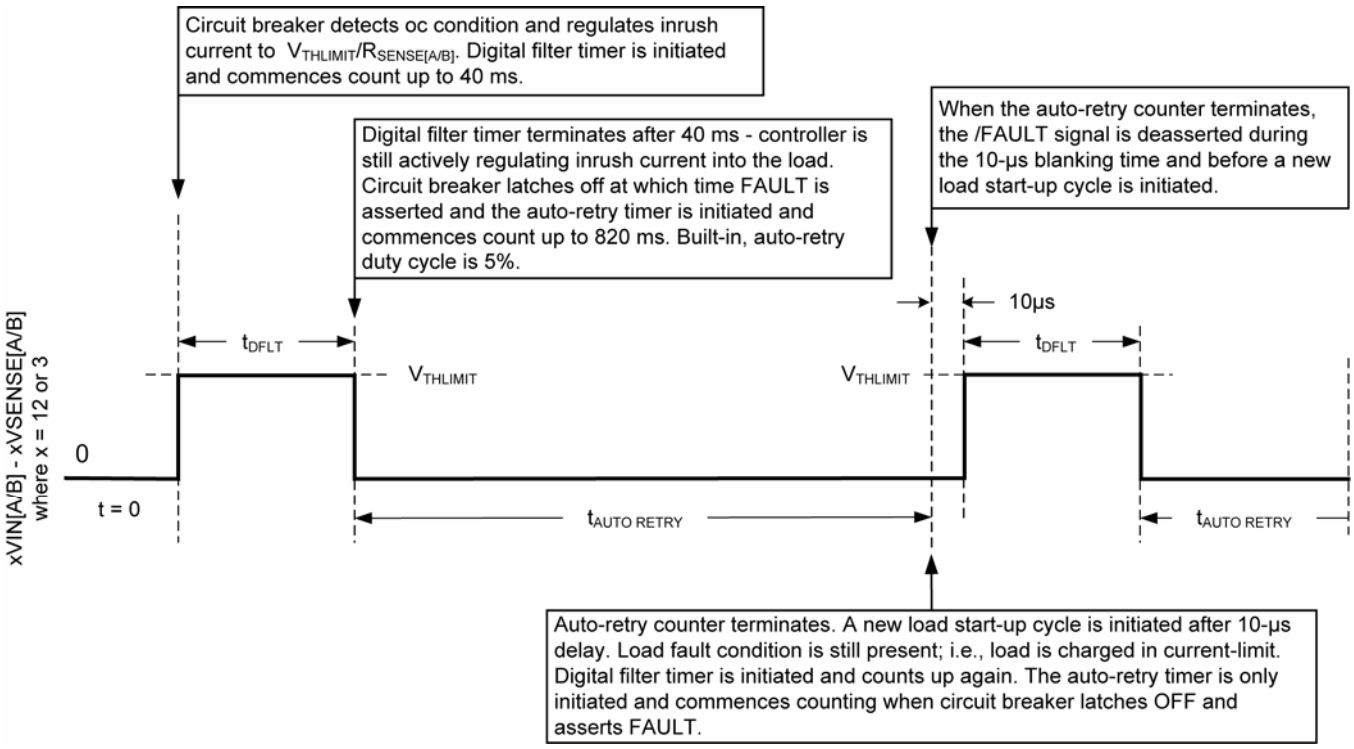


Figure 7. MIC2341R Auto-Retry Timing Diagram and Operation in Current-limit

Thermal Shutdown

The internal VAUX[A/B] MOSFETs are protected against damage not only by current limiting, but by overtemperature protection as well. Should an overcurrent condition on either VAUX[A] or VAUX[B] raise the junction temperature of the MIC2341 to 140°C, all of the outputs for that corresponding slot (including VAUX) will be shut off and that slot's /FAULT_AUX output will be asserted. The slot's /FAULT_MAIN output will not be asserted. The other slot's operating condition will remain unaffected. However, should the MIC2341's die temperature exceed 160°C because of an overcurrent fault condition on both VAUX[A] and

VAUX[B], both slots (all outputs, including VAUXA and VAUXB) will be shut off. In this case, both /FAULT_AUX[A/B] output signals will be asserted; the /FAULT_MAIN[A/B] output signals will not be asserted.

Plug-in Card Retention Switch Inputs

Two pins on the MIC2341 are available for use as card retention switch inputs, /CRSW[A/B]. These pins are internally pulled-up by 45kΩ resistors to VSTBY and prevent the enabling of all gate drive circuits on 12GATE[A/B], 3VGATE[A/B], and VAUX[A/B] unless these input pins are asserted LOW. In addition, each of these inputs exhibits an internal debounce delay time of approximately 10ms.

/FORCE_ON[A/B] Inputs

These level sensitive, asserted active-low digital inputs are internally pulled up to VSTBY through a weak current source and are intended for diagnostics during the debug phase of the system design involving the MIC2341. In asserting /FORCE_ON[A/B] LOW, all three of the respective slot's outputs (+12V, +3.3V, and VAUX) will turn on. However, all protections for those outputs are disabled. This explicitly includes all overcurrent and short circuit protections, and on-chip thermal protection for the VAUX supplies. Additionally, asserting a slot's /FORCE_ON[A/B] input will disable all of its input and output UVLO protections, with the sole exception of that asserting either or both of the /FORCE_ON[A/B] inputs will not disable the VSTBY[A/B] input UVLO.

Asserting /FORCE_ON[A/B] LOW will cause the respective slot's /PWRGD[A/B], and /DLY_PWRGD[A/B] output signals to be asserted LOW while the /FAULT_MAIN[A/B], the /FAULT_AUX[A/B}, the /INT, and the SYSPWRGD output signals to enter their open-drain state.

/PWRGD[A/B] and /DLY_PWRGD Digital Outputs

The MIC2341 has two /PWRGD outputs and two /DLY_PWRGD outputs, one for each slot. These are open-drain, active-low outputs that are activated after power-on-reset and are normally connected by an

external 10kΩ resistor to V_{STBY} or a local logic supply. Each /PWRGD[A/B] output is asserted when a slot has been enabled and has successfully begun delivering power to its respective +12V, +3.3V, and VAUX outputs. The /DLY_PWRGD[A/B] outputs are asserted 164ms after its corresponding /PWRGD[A/B] output. An equivalent logic diagram for /PWRGD[A/B] is shown in Figure 8 with their corresponding state diagrams.

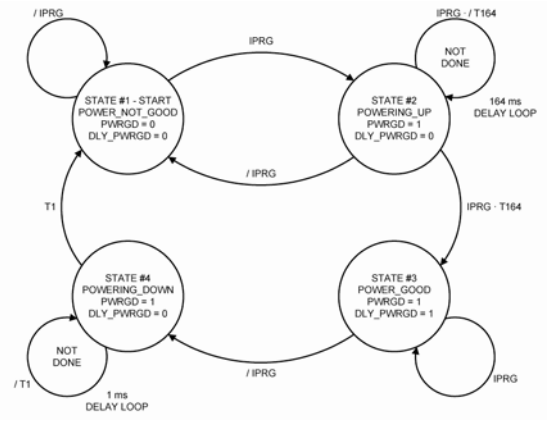


Figure 8. State Diagrams for /PWRGD[A/B] and /DLY_PWRGD[A/B]

SYSPWRGD Digital Output

SYSPWRGD is an open-drain, asserted active-HIGH digital output provided by the MIC2341 for additional slot status information to the service or system processor. This output is normally connected by an external 10kΩ resistor to V_{STBY} or a local logic supply. There is one SYSPWRGD output for each MIC2341 and this signal becomes activated after power-on-reset. This signal is asserted unless at least one PCIe slot is occupied, either ON[A/B] and/or AUXEN[A/B] of the slot in question is asserted, either /FORCE_ON[A/B] inputs are not asserted, and the output voltages at the load are lower than respective Power-is-Good output threshold voltages. Functionality of the SYSPWRGD output signal has been designed to accommodate single- and dual-slot applications as well as applications where the MAIN[A/B] outputs are used, but the VAUX[A/B] outputs are not. In multiple MIC2341 applications where one or more PCIe slots are unused and one or multiple ON[A/B] and AUXEN[A/B] input signals are not asserted, each SYSPWRGD digital output will appear asserted facilitating an “OR-tying” of all SYSPWRGD output signals, thereby ensuring correct logic functionality across the entire system. See Table 1 for the SYSPWRGD truth table.

ONA	AUXENA	/CRSWA	/FORCE_ONA	$12V_{OUT}$ MAIN A	$3V_{OUT}$ MAIN A	VAUX A	ONB	AUXENB	/CRSWB	/FORCE_ONB	$12V_{OUT}$ MAIN B	$3V_{OUT}$ MAIN B	VAUX B	SYSPWRGD
1	X	0	1	UV	X	X	X	X	X	X	X	X	X	0
1	X	0	1	X	UV	X	X	X	X	X	X	X	X	0
X	1	0	1	X	X	UV	X	X	X	X	X	X	X	0
X	X	X	X	X	X	X	1	X	0	1	UV	X	X	0
X	X	X	X	X	X	X	1	X	0	1	X	UV	X	0
X	X	X	X	X	X	X	X	1	0	1	X	X	UV	0

where “1” = Logic HIGH
“0” = Logic LOW
“X” = Don’t care

Table 1. SYSPWRGD Truth Table

Hardware Interface

Once the input power supply voltages are above their respective UVLO thresholds, the MIC2341/MIC2341R’s hardware interface can be enabled for power control by asserting the control input pins (/CRSW[A/B], AUXEN[A/B], and ON[A/B]) appropriately for each slot. The MIC2341/MIC2341R’s ON[A/B] and AUXEN[A/B] signals are asserted active-HIGH, level-sensitive digital inputs with internal pull-up 45kΩ resistors to VSTBY[A] to save pc board area and external component costs. As such, external hot-plug controllers connecting to these pins should configure their respective output drivers to OPEN-DRAIN and configure their firmware to de-assert these signals to turn OFF either the MAIN[A/B] outputs or the VAUX[A/B] outputs. As these input control signals are already asserted after POR, the corresponding /CRSW[A/B] control signal should be used to enable the slot’s gate drive circuits to initiate a power-up sequence. For example, in order for the MIC2341/MIC2341R to switch on the VAUX supply for either slot, the AUXEN[A/B] control can be enabled during or after the power-on-reset operation (typically, t_{POR} = 160µs. The timing response diagram of Figure 9 illustrates the hardware interface operation where an overcurrent fault is detected by the MIC2341/MIC2341R controller after initiating a power-up sequence. The MAIN (+12V & +3.3V) and VAUX[A/B] supply rails, /FAULT, /PWRGD and /INT output responses for both AUX and MAIN are shown in the figure.