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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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MIC3002

FOM Management IC with Internal Calibration

General Description

The MIC3002 is a fiber optic module controller which enables the implementation of sophisticated, hot-pluggable fiber optic transceivers with intelligent laser control and an internally calibrated Digital Diagnostic Monitoring Interface per SFF-8472. It essentially integrates all non-datapath functions of an SFP transceiver into a tiny (4mm x 4mm) QFN package. It also works well as a microcontroller peripheral in transponders or 10Gbps transceivers.

A highly configurable automatic power control (APC) circuit controls laser bias. Bias and modulation are temperature compensated using dual DACs, an on-chip temperature sensor, and NVRAM look-up tables. A programmable internal feedback resistor provides a wide dynamic range for the APC. Controlled laser turn-on facilitates hot plugging.

An analog-to-digital converter converts the measured temperature, voltage, bias current, transmit power, and received power from analog to digital. An EEPOT provides front-end adjustment of RX power. Each parameter is compared against user-programmed warning and alarm thresholds. Analog comparators and DACs provide high-speed monitoring of received power and critical laser operating parameters. Data can be reported as either internally calibrated or externally calibrated.

An interrupt output, power-on hour meter, and data-ready bits add user friendliness beyond SFF-8472. The interrupt output and data-ready bits reduce overhead in the host system. The power-on hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM.

In addition to the features listed above which are already implemented in the previous controller MIC3001, the MIC3002 features an extensive temperature range, options to mask alarms and warnings interrupt and TXFAULT, and ability to support up to four chips with the same address on the serial interface.

Communication with the MIC3002 is via an industry standard 2-wire serial interface. Nonvolatile memory is provided for serial ID, configuration, and separate OEM and user scratchpad spaces. Two-level password protection guards against data corruption.

Features

- Extensive temperature range
- Alarms and Warnings interrupt and TXFAULT masks
- Capability to support up to four chips on the serial interface
- LUT to compensate for chip-FOM case temperature difference
- APC or constant-current laser bias
- Turbo mode for APC loop start-up and shorter laser turn on time
- Supports multiple laser types and bias circuit topologies
- Integrated digital temperature sensor
- Temperature compensation of modulation, bias, and fault levels via NVRAM look-up tables
- NVRAM to support GBIC/SFP serial ID function
- User writable EEPROM scratchpad
- Diagnostic monitoring interface per SFF-8472
  - Monitors and reports critical parameters: temperature, bias current, TX and RX optical power, and supply voltage
  - S/W control and monitoring of TXFAULT, RXLOS, RATESELECT, and TXDISABLE
  - Internal or external calibration
  - EEPOT for adjusting RX power measurement
- Power-on hour meter
- Interrupt capability
- Extensive test and calibration features
- 2-wire SMBus-compatible serial interface
- SFP/SFP+ MSA and SFF-8472 compliant
- 3.0V to 3.6V power supply range
- 5V-tolerant I/O
- Available in (4mm x 4mm) 24-pin QFN package

Applications

- SFP/SFP+ optical transceivers
- SONET/SDH transceivers and transponders
- Fibre Channel transceivers
- 10Gbps transceivers
- Free space optical communications
- Proprietary optical links

Ordering Information

Part Number	Package Type	Junction Temp. Range	Package Marking	Lead Finish
MIC3002BML	24-pin QFN	–45°C to +105°C	3002	Sn-Pb
MIC3002BMLTR[1]	24-pin QFN	–45°C to +105°C	3002	Sn-Pb
MIC3002GML	24-pin QFN	–45°C to +105°C	3002 with Pb-Free bar-line indicator	Pb-Free NiPdAu
MIC3002GMLTR[1]	24-pin QFN	–45°C to +105°C	3002 with Pb-Free bar-line indicator	Pb-Free NiPdAu

1. Note:

2. Tape and Reel.

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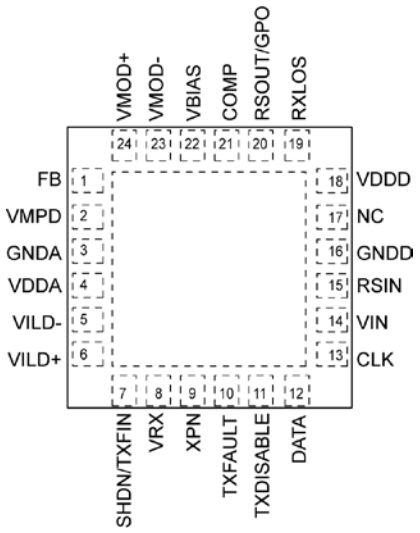
Pin Configuration



24-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	FB	Analog Input. Feedback voltage for the APC loop op-amp. Polarity and scale are programmable via the APC configuration bits. Connect to V_{BIAS} if APC is not used.
2	VMPD	Analog Input. Multiplexed A/D converter input for monitoring transmitted optical power via a monitor photodiode. In most applications, VMPD will be connected directly to FB. The input range is 0 - V_{REF} or 0 - V_{REF}/4 depending on the setting of the APC configuration bits
3	GNDA	Ground return for analog functions.
4	VDDA	Power supply input for analog functions.
5	VILD–	Analog Input. Reference terminal for the multiplexed pseudo-differential A/D converter inputs for monitoring laser bias current via a sense resistor (VILD+ is the sensing input). Tie to V_{DD} or GND to reference the voltage sensed on VILD+ to V_{DD} or GND, respectively. Limited common-mode voltage range, see “Applications Information” section for more details.
6	VILD+	Analog Input. Multiplexed A/D input for monitoring laser bias current via a sense resistor (signal input); accommodates inputs referenced to V_{DD} or GND (see pin 5 description). Limited common-mode voltage range, see “Applications Information” section for more details.
7	SHDN/TXFIN	Digital output/Input; programmable polarity. When used as shutdown output (SHDN), OEMCFG3-2 set to 0, SHDN is asserted at the detection of a fault condition if OEMCFG4-7 is set to 0. If the latter bit is set to 1, a fault condition will not assert SHDN. When programmed as TXFIN, it is an input for external fault signals to be ORed with the internal fault sources to drive TXFAULT.
8	VRX	Analog Input. Multiplexed A/D converter input for monitoring received optical power. The input range is 0 to V_{REF}. A 5-bit programmable EEPOT on this pin provides for coarse calibration and ranging of the RX power measurement.
9	XPN	Analog Input/Output. Optional connection to an external PN junction for sensing temperature at a remote location. The Zone bit in OEMCFG1 determines whether temperature is measured using the on-chip sensor or the remote PN junction.
10	TXFAULT	Digital Output; Open-Drain, programmable polarity. If OEMCFG5-4 is set to 0, a high level indicates a hardware fault impeding transmitter operation. The state of this pin is always reflected in the TXFLT bit.

Pin Description

Pin Number	Pin Name	Pin Function
11	TXDISABLE	Digital Input; Active High. The transmitter is disabled when this line is high or the STXDIS bit is set. The state of this input is always reflected in the TXDIS bit.
12	DATA	Digital I/O; Open-drain. Bi-directional serial data input/output.
13	CLK	Digital Input; Serial clock input.
14	VIN/INT	If bit 4 (IE) in USRCTL register is set to 0 (default), this pin is configured as analog input. If IE bit is set to 1, this pin is configured as open-drain output. Analog Input: Multiplexed A/D input for monitoring supply voltage. 0V to 5.5V input range. Open-drain output: outputs the internally generated interrupt signal /INT.
15	RSIN	Digital Input; Rate Select Input; ORed with rate select bit to determine the state of the RSOUT pin. The state of this pin is always reflected in the RSEL bit.
16	GNDD	Ground return for digital functions.
17	NC	No connection. This pin is used for test purposes and must be left unconnected.
18	VDDD	Power supply input for digital functions.
19	RXLOS	Digital Output; programmable polarity Open-Drain. Indicates the loss of the received signal as indicated by a level of received optical power below the programmed RXLOS comparator threshold; may be wire-ORed with external signals. Normal operation is indicated by a Low level when OEMCFG6-3 is set to 0 and a high level when OEMCFG6-3 is set to 1. RXLOS is de-asserted when VRX > LOSFLTn. The LOS bit reflects the state of RXLOS whether driven by the MIC3002 or an external circuit.
20	RS0/GPO	Digital Output. Open-Drain or push-pull. When used as rate select output, it represents the receiver rate select as per SFF. This output is controlled by the SRSEL bit ORed with RSIN input and is open drain only. When used as a general-purpose, non-volatile output, it is controlled by the GPO configuration bits in OEMCFG3.
21	COMP	Analog Output, compensation terminal. Connect a capacitor between this pin and GNDA or V_{DDA} with appropriate value to tune the APC loop time constant to a desirable value.
22	VBIAS	Analog Output. Buffered DAC output capable of sourcing or sinking up to 10mA under control of the APC function to drive an external transistor for laser diode D.C. bias. The output and feedback polarity are programmable to accommodate either a NPN or a PNP transistor to drive a common-anode or common-cathode laser diode.
23	VMOD–	Analog Input. Inverting terminal of VMOD buffer op-amp. Connect to V_{MOD}+ (gain = 1) or feedback resistors network to set a different gain
24	VMOD+	Analog Output. Buffered DAC output to set the modulation current on the laser driver IC. Operates with either a 0– V_{REF} or a (V_{DD}–V_{REF}) – V_{DD} output swing so as to generate either a ground-referenced or a V_{DD} referenced programmed voltage. A simple external circuit can be used to generate a programmable current for those drivers that require a current rather than a voltage input. See “Applications Information” section for more details.

Absolute Maximum Ratings[1]

Power Supply Voltage, V_{DD} ..... +3.8V
Voltage on CLK, DATA, TXFAULT, VIN, RXLOS, DISABLE, RSIN.....–0.3V to +6.0V
Voltage On Any Other Pin.....–0.3V to V_{DD}+0.3V
Power Dissipation, T_A = 85°C 1.5W
Junction Temperature (T_J) ..... 150°C
Storage Temperature (T_S) ..... –65°C to +150°C
ESD Ratings[3]
Human Body Model..... 2kV
Machine Model..... 300V
Soldering (20sec) 260ºC

Operating Ratings[2]

Power Supply Voltage, V_{DDA}/V_{DDD} ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ... –40°C to +105°C
Package Thermal Resistance
QFN (θ_{JA})..... 43°C/W

Electrical Characteristics

For typical values, T_A = 25°C, V_{DDA} = V_{DDD} = +3.3V, unless otherwise noted. **Bold** values are guaranteed for +3.0V ≤ (V_{DDA} = V_{DDD}) ≤ 3.6V, $T_{(min)} \le T_A \le T_{(max)}$[8]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
I_{DD}	Supply Current	CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE low; all DACs at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
		CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE high; FLTDAC at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
V_{POR}	Power-on Reset Voltage	All registers reset to default values; A/D conversions initiated.		2.9	2.98	V
V_{UVLO}	Under-Voltage Lockout Threshold	Note 5	2.5	2.73		V
V_{HYST}	Power-on Reset Hysteresis Voltage			170		mV
t_{POR}	Power-on Reset Time	V_{DD} > V_{POR}[4]		50		µs
V_{REF}	Reference Voltage		1.210	1.225	1.240	V
$\Delta V_{REF}/\Delta V_{DDA}$	Voltage Reference Line Regulation			1.7		mV/V
Temperature-to-Digital Converter Characteristics						
	Local Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C[6]		±1	±3	°C
	Remote Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C[6]		±1	±3	°C
t_{CONV}	Conversion Time	Note 4			60	ms
t_{SAMPLE}	Sample Period				100	ms
Remote Temperature Input, XPN						
I_F	Current to External Diode[4]	XPN at high level, clamped to 0.6V.		192	400	µA
		XPN at low level, clamped to 0.6V.	7	12		µA

Voltage-to-Digital Converter Characteristics (V_{RX}, V_{AUX}, V_{BIAS}, V_{MPD}, $V_{ILD±}$)

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Voltage Measurement Error	–40°C ≤ T_A ≤ +105°C(6)		±1	±2.0	%fs
t_{CONV}	Conversion Time	Note 4			10	ms
t_{SAMPLE}	Sample Period	Note 4			100	ms
Voltage Input, V_{IN} (Pin 14 used as an ADC Input)						
V_{IN}	Input Voltage Range	–0.3 ≤ V_{DD} ≤ 3.6V	GNDA		5.5	V
I_{LEAK}	Input Current	V_{IN} = V_{DD} or GND; V_{AUX} = V_{IN}		55		µA
C_{IN}	nput Capacitance			10		pF
Digital-to-Voltage Converter Characteristics (V_{MOD}, V_{BIAS})						
	Accuracy	–40°C ≤ T_A ≤ +105°C(6)		±1	2.0	%fs
t_{CONV}	Conversion Time	Note 4			20	ms
DNL	Differential Non-linearity Error	Note 4		±0.5	±1	LSB
Bias Current Sense Inputs, V_{ILD}+, V_{ILD}–						
V_{ILD}	Differential Input Signal Range, $\lvert V_{ILD}^+ - V_{ILD}^- \rvert$		0		V_{REF}/4	mV
I_{IN+}	V_{ILD}^+ input current				±1	µA
$I_{IN–}$	V_{ILD}^- input current	V_{ILD}^- referred to V_{DDA}		+150		µA
	$\lvert V_{ILD}^+ - V_{ILD}^- \rvert$ = 0.3V	V_{ILD}^- referred to GND		-150		µA
C_{IN}	Input Capacitance			10		pF
APC Op Amp, FB, V_{BIAS}, COMP						
GBW	Gain Bandwidth Product	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient(4)			1		µV/°C
V_{OUT}	Output Voltage Swing	I_{OUT} = 10mA, SRCE bit = 1	GNDA		1.25	V
		I_{OUT} = -10mA, SRCE bit = 0	V_{DDA} -1.25		V_{DDA}	V
I_{SC}	Output Short-Circuit Current			55		mA
t_{SC}	Short Circuit Withstand Time	T_J ≤ 150°C(4)				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; Gain = 1, to GND		55		dB
		C_{COMP} = 20pF; Gain = 1, to V_{DD}		40		
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF, Note 4			1	V/V
ΔV/Δt	Slew Rate	C_{COMP} = 20pF; Gain = 1		3		V/µs
ΔRFB	Internal Feedback Resistor Tolerance			±20		%
ΔRFB/Δt	Internal Feedback Resistor Temperature Coefficient			25		ppm/C
I_{START}	Laser Start-up Current Magnitude	START = 01_h		0.375		mA
		START = 02_h		0.750		mA
		START = 04_h		1.500		mA
		START = 08_h		3.000		mA
C_{IN}	Pin Capacitance			10		pF

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{MOD} Buffer Op-Amp, V_{MOD}+, V_{MOD}–						
GBW	Gain Bandwidth	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient			1		µV/°C
I_{BIAS}	V_{MOD}– Input Current			±0.1	±1	µA
V_{OUT}	Output Voltage Swing	I_{OUT} = ±1mA	GNDA+75		V_{DDA}-75	mV
I_{SC}	Output Short-Circuit Current			35		mA
t_{SC}	Short Circuit Withstand Time	$T_J \le 150°C$(4)				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; Gain = 1, to GND		65		dB
		C_{COMP} = 20pF; Gain = 1, to V_{DD}		44		dB
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF			1	V/V
$\Delta V/\Delta T$	Slew Rate	C_{COMP} = 20pF; Gain = 1		1		V/µs
C_{IN}	Pin Capacitance			10		pF
Control and Status I/O, TXDISABLE, TXFAULT, RSIN, RSOUT(GPO), SHDN(TXFIN), RXLOS, /INT						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.0			V
V_{OL}	Low Output Voltage	$I_{OL} \le$ 3mA			0.3	V
V_{OH}	High Output Voltage (applies to SHDN only)	$I_{OH} \le$ 3mA			V_{DDD}–0.3	V
I_{LEAK}	Input Current				±1	µA
C_{IN}	Input Capacitance			10		pF
Transmit Optical Power Input, V_{MPD}						
V_{IN}	Input Voltage Range	Note 4	GNDA		V_{DDA}	V
V_{RX}	Input Signal Range	BIASREF=0			V_{REF}	V
		BIASREF=1	V_{DDA}–V_{REF}		V_{DDA}	V
C_{IN}	Input Capacitance	Note 4		10		pF
I_{LEAK}	Input Current				±1	µA
Received Optical Power Input, VRX, RXPOT						
	Input Voltage Range	Note 4	GNDA		V_{DDA}	V
V_{RX}	Valid Input Signal Range (ADC Input Range)		0		V_{REF}	V
$R_{RXPOT(32)}$	End-to-End Resistance	RXPOT = $1F_h$		32		KΩ
ΔRXPOT	Resistor Tolerance			±20		%
ΔRXPOT/ΔT	Resistor Temperature Coefficient			25		ppm/C
$\Delta V_{RX}/V_{RXPOT}$	Divider Ratio Accuracy	00 ≤ RXPOT ≤ $1F_h$	-5		+5	%
I_{LEAK}	Input Current	RXPOT = 0 (disconnected)			±1	µA
C_{IN}	Input Capacitance	Note 4		10		pF
I_{LEAK}	Input Current				±1	µA

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Control and Status I/O Timing, TXFAULT, TXDISABLE, RSIN, RSOUT, and RXLOS						
t_{OFF}	TXDISABLE Assert Time	From input asserted to optical output at 10% of nominal, C_{COMP} = 10nF.			**10**	µs
t_{ON}	TXDISABLE De-assert Time	From input de-asserted to optical output at 90% of nominal, C_{COMP} = 10nF.			**1**	ms
t_{INIT}	Initialization Time	From power on or transmitter enabled to optical output at 90% of nominal and TX_FAULT de-asserted.(4)			**300**	ms
t_{INIT2}	Power-on Initialization Time	From power on to APC loop-enabled.			**200**	ms
t_{FAULT}	TXFAULT Assert Time	From fault condition to TXFAULT assertion.(4)			95	µs
t_{RESET}	Fault Reset Time	Length of time TXDISABLE must be asserted to reset fault condition.	**10**			µs
t_{LOSS_ON}	RXLOS Assert Time	From loss of signal to RXLOS asserted.			95	µs
t_{LOSS_OFF}	RXLOS De-assert Time	From signal acquisition to LOS de-asserted.			**100**	µs
t_{DATA}	Analog Parameter Data Ready	From power on to valid analog parameter data available.(4)			**400**	ms
t_{PROP_IN}	TXFAULT, TXDISABLE, RXLOS, RSIN Input Propagation Time	Time from input change to corresponding internal register bit set or cleared.(4)			**1**	µs
t_{PROP_OUT}	TXFAULT, RSOUT, /INT Output Propagation Time	From an internal register bit set or cleared to corresponding output change.(4)			**1**	µs
Fault Comparators						
ϕ_{FLTTMR}	Fault Suppression Timer Clock Period	Note 4	**0.475**	0.5	**0.525**	ms
	Accuracy		-3		+3	%/F.S.
t_{REJECT}	Glitch Rejection	Maximum length pulse that will not cause output to change state.(4)	4.5			µs
V_{SAT}	Saturation Detection Threshold	High level		95		%VDDA
		Low level		5		%VDDA
Power-On Hour Meter						
	Timebase Accuracy	0°C ≤ T_A ≤ +70°C(4)	**+5**		**-5**	%
		–40°C ≤ T_A ≤ +105°C	**+10**		**-10**	%
	Resolution	Note 4		10		hours
Non-Volatile (FLASH) Memory						
t_{WR}	Write Cycle Time(7)	From STOP of a one to four-byte write transaction.(4)			**13**	ms
	Data Retention		**100**			years
Endurance	Minimum Permitted Number Write Cycles		**10,000**			cycles

Serial Data I/O Pin, Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Output Voltage	I_{OL} = 3mA			**0.4**	V
		I_{OL} = 6mA			**0.6**	V
V_{IL}	Low Input Voltage				**0.8**	V
V_{IH}	High Input Voltage		**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 4		10		pF

Serial Clock Input, CLK

V_{IL}	Low Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V			**0.8**	V
V_{IH}	High Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V	**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 4		10		pF

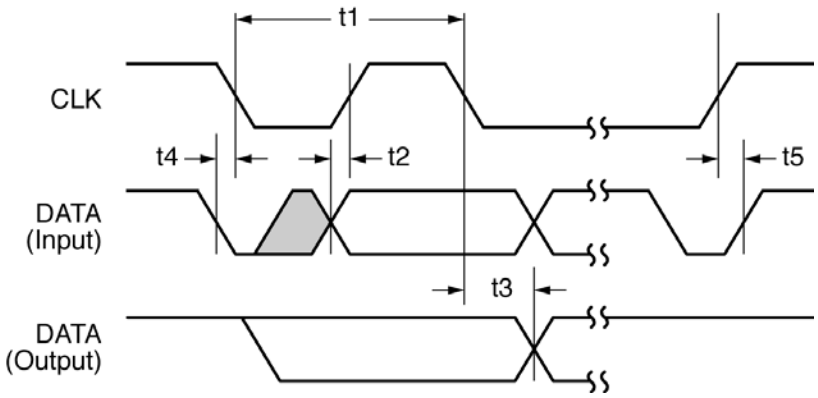
Serial Interface Timing(4)

t_1	CLK (clock) Period		**2.5**			µs
t_2	Data In Setup Time to CLK High		**100**			ns
t_3	Data Out Stable After CLK Low		**300**			ns
t_4	Data Low Setup Time to CLK Low	Start Condition	**100**			ns
t_5	Data High Hold Time After CLK High	Stop Condition	**100**			ns
t_{DATA}	Data Ready Time	From power on to completion of one set of ADC conversions; analog data available via serial interface.			**400**	ms

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Guaranteed by designing and/or testing of related parameters. Not 100% tested in production.
5. The MIC3000 will attempt to enter its shutdown state when V_{DD} falls below V_{UVLO}. This operation requires time to complete. If the supply voltage falls too rapidly, the operation may not be completed.
6. Does not include quantization error.
7. The MIC3002 will not respond to serial bus transactions during an EEPROM write-cycle. The host will receive a NACK during t_{WR}.
8. Final test on outgoing product is performed at T_A = +25°C.

Timing Diagram



Serial Interface Timing

Address Map

Address(s)	Field Size (Bytes)	Name	Description
0 –95	96	Serial ID defined by SEP MSA	G-P NVRAM; R/W under valid OEM password.
96 – 127	32	Vendor Specific	Vendor specific EEPROM
128 – 255	128	Reserved	Reserved for future use. G-P NVRAM; R/W under valid OEM password.

Table 1. MIC3002 Address Map, Serial Address = $A0_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00-27	0-39	40	Alarm and Warning Threshold	High/low limits for warning and alarms; writeable using OEM p/w; read-only otherwise.
28-37	40-55	16	Reserved	Reserved – do not write; reads undefined.
38-5B	56-91	36	Calibration Constants	Numerical constants for external calibration; writeable using OEM p/w; read-only otherwise.
5C-5E	92-94	3	Reserved	Reserved – do not write; reads undefined.
5F	95	1	Checksum	G-P NVRAM; writeable using OEM p/w; ready only otherwise.
60-69	96-105	10	Analog Data	Real time analog parameter data.
6A-6D	106-109	4	Reserved	Reserved – do not write; reads undefined.
6E	110	1	Control/Status Bits	Control and status bits.
6F	111	1	Reserved	Reserved – do not write; reads undefined.
70-71	112-113	2	Alarm Flags	Alarm status bits; read only.
72-73	114-115	2	Reserved	Reserved – do not write; reads undefined.
74-75	116-117	2	Warning Flags	Warning status bits; read only.
76-77	118-119	2	Reserved	Reserved – do not write; reads undefined.
78-7E	120-126	7	OEMPW	OEM password entry field. The OEM password location can be selected to be 78-7B (120-123) or 7B-7E (123-126) by setting the bit OEMCFG5 bit 2 to 0 (default) or 1.
7F	127	1	Vendor Specific	Vendor specific. Reserved – do not write; reads undefined.
80-DD	128-221	94	User Scratchpad	User writeable EEPROM. G-P NVRAM; R/W using any valid password.
DE	222	1	ALT_USRCTL	Alternate location for USRCTL register. Set bit OEMCFG6-2 to 1 to select this location. Can be used as a scratch pad if not selected.
DF-F5	223-245	23	User Scratchpad	User writeable EEPROM. G-P NVRAM; R/W using any valid password.
F6	246	1	USRPWSET	User password setting; read/write using any p/w; returns zero otherwise.
F7	247	1	USRPW	User password register
F8-F9	248-249	2	Alarms Masks	Bit =1: corresponding alarm not masked Bit = 0: corresponding alarm masked
FA-FB	250-251	2	Warnings Masks	Bit =1: corresponding warning not masked Bit = 0: corresponding warning masked
FC-FE	252-254	3	Reserved	Reserved – do not write; reads undefined.
FF	255	1	USRCTL	End-user control and status bits If ALT-USRCTL is not selected. Can be used as a scratch pad if not selected.

Table 2. MIC3002 Address Map, Serial Address = $A2_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00-3F	0-63	64	BIASLUT1	Bias temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: 90-9B.
40-7F	64-127	64	MODLUT1	Modulation temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: A0-AB.
80-BF	128-191	64	IFTLUT1	Bias current fault threshold temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: B0-BB.
C0-FF	192-255	64	HATLUT1	Bias current high alarm threshold temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: C0-CB.

Table 3. Temperature Compensation Tables, Serial Address = $A4_h$

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
00	0	1	OEMCFG0	OEM configuration register 0
01	1	1	OEMCFG1	OEM configuration register 1
02	2	1	OEMCFG2	OEM configuration register 2
03	3	1	APCSET0	APC setpoint register 0
04	4	1	APCSET1	APC setpoint register 1
05	5	1	APCSET2	APC setpoint register 2
06	6	1	MODSET0	Modulation setpoint register 0
07	7	1	IBFLT	Bias current fault-comparator threshold. This register is temperature compensated
08	8	1	TXPFLT	TX power fault threshold
09	9	1	LOSFLT	RX LOS fault-comparator threshold
0A	10	1	FLTTMR	Fault comparator timer setting
0B	11	1	FLTMSK	Fault source mask bits
0C-0F	12-15	4	OEMPWSET	Password for access to OEM areas
10	16	1	OEMCAL0	OEM calibration register 0
11	17	1	OEMCAL1	OEM calibration register 1
12	18	1	LUTINDX	Look-up table index read-back
13	19	1	OEMCFG3	OEM configuration register 3
14	20	1	APCDAC	Reads back current APC DAC value (setpoint+offset)
15	21	1	MODDAC	Reads back current modulation DAC value (setpoint+offset)
16	22	1	OEMREAD	Reads back OEM calibration data
17	23	1	LOSFLTn	LOS De-assert threshold
18	24	1	RXPOT	RXPOT tap selection
19	25	1	OEMCFG4	OEM configuration register 4
1A	26	1	OEMCFG5	OEM configuration register 5
1B	27	1	OEMCFG6	OEM configuration register 6
1C-1D	28-29	2	SCRATCH	Reserved – do not write; reads undefined.
1E	30	1	MODSET 1	Modulation setpoint register 1
1F	31	1	MODSET 2	Modulation setpoint register 2

20-27	32-39	8	POHDATA	Power-on hour meter scratchpad
28-47	40-71	32	RXLUT	RX power calibration look-up table. Eight sets of slope and offset
48-57	72-87	16	CALCOEF	Slope and offset coefficients used for Temperature, Voltage, Bias, and TXPOWER internal calibration
58-5F	88-95	8	SCRATCH	OEM scratchpad area
60-86	96-134	39	TCTRLUT	LUT to temperature-compensate temperature results and/or temperature to be used by parameters compensation LUT.
87-8F	135-143	9	SCRATCH	OEM scratchpad area.
90-9B	144-155	12	BIASLUT2	Bias temperature compensation L.U.T. additional 12 entries.
9C-9F	156-159	4	SCRATCH	OEM scratchpad area
A0-AB	160-171	12	MODLUT2	Modulation temperature compensation L.U.T. additional 12 entries.
AC-AF	172-175	14	SCRATCH	OEM scratchpad area.
B0-BB	176-187	12	IFTLUT2	Bias current fault threshold temperature compensation L.U.T. additional 12 entries.
BC-BF	188-191	4	SCRATCH	OEM scratchpad area
C0-CB	192-203	12	HATLUT2	Bias current high alarm threshold temperature compensation L.U.T. additional 12 entries.
CC-CF	204-207	4	SCRATCH	OEM scratchpad area
D0-DD	208-221	14	RXLUTSEG	RXPWR calibration segments delimiters. Each of the eight segments can have its own slope and offset.
DE-FA	222-250	128	SCRATCH	OEM scratchpad area
FB-FC	251-252	2	POH	Power on hour meter result; read only
FD	253	1	Data Ready Flags	Data ready bits for each measured parameter; read only
FE	254	1	MFG_ID	Manufacturer identification (Micrel = 42 = 2Ah)
FF	255	1	DEV_ID	Device and die revision

Table 4. OEM Configuration Registers, Serial Address = $A6_h$

Block Diagram

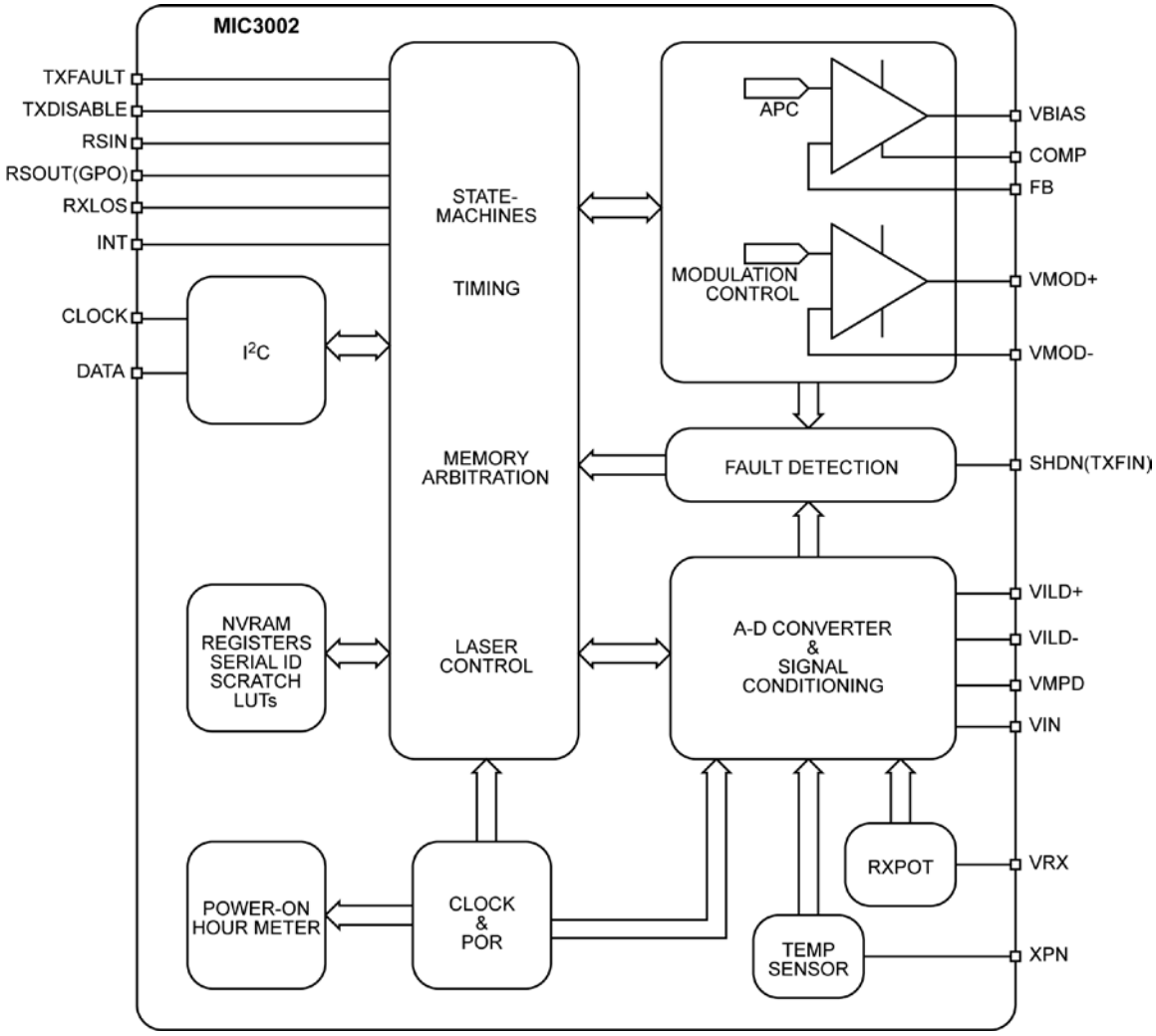


Figure 1. MIC3002 Block Diagram

Analog-to-Digital Converter/Signal Monitoring

A block diagram of the monitoring circuit is shown below. Each of the five analog parameters monitored by the MIC3002 are sampled in sequence. All five parameters are sampled and the results updated within the t_{CONV} internal given in the "Electrical Characteristics" section. In $\overline{OEM}$ Mode, the channel that is normally used to measure V_{IN} may be assigned to measure the level of the V_{DDA} pin or one of five other nodes. This provides a kind of analog loopback for debug and test purposes. The V_{AUX} bits in OEMCFG0 control which voltage source is being sampled. The various V_{AUX} channels are level-shifted differently depending on the signal source, resulting in different LSB values and signal ranges. See Table 5.

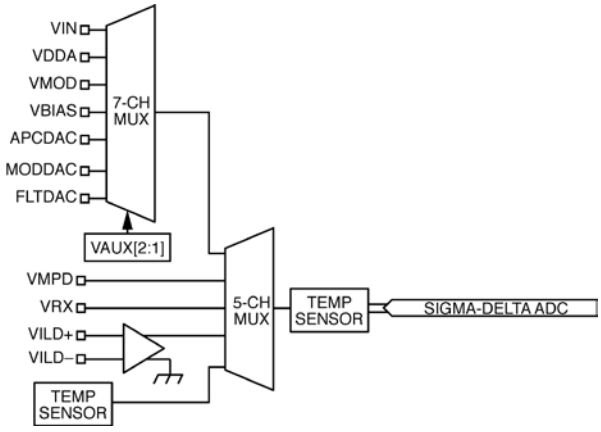


Figure 2. Analog-to-Digital Converter Block Diagram

Channel	ADC Resolution (bits)	Conditions	Input Range (V)	LSB[1]
TEMP	8 or 9		N/A	1°C or 0.5°C
VAUX	8	See Table 6		
VMPD	8	GAIN = 0; BIASREF = 0	GNDA - V_{REF}	4.77mV
		GAIN = 0; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF})	
		GAIN = 1; BIASREF = 0	GNDA - V_{REF}/4	1.17mV
		GAIN = 1; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF}/4)	
VILD	8	VILD- = VDDA	V_{DDA} – (V_{DDA} – V_{REF})	4.77mV
		VILD- = GNDA	GNDA - V_{REF}	
VRX	12	RXPOT = 00	0 - V_{REF}	0.298mV

Table 5. A/D Input Signal Ranges and Resolutions

Note:

1. Assumes typical VREF value of 1.22V.

Channel	VAUX [2:0]	Input Range (V)	LSB[1] (mV)
V_{IN}	000 = 00_h	0.5V to 5.5V	25.6mV
V_{DDA}	0001 = 01_h	0.5V to 5.5V	25.6mV
V_{BIAS}	010 = 02_h	0.5V to 5.5V	25.6mV
V_{MOD}	011 = 03_h	0.5V to 5.5V	25.6mV
APCDAC	100 = 04_h	0V to V_{REF}	4.77mV
MODDAC	101 = 05_h	0V to V_{REF}	4.77mV
FLTDAC	110 = 06_h	0V to V_{REF}	4.77mV

Table 6. V_{AUX} Input Signal Ranges and Resolutions

Note:

1. Assumes typical V_{REF} value of 1.22V.

Temperature Reading Compensation

The sensed temperature by the MIC3002 can be temperature compensated and converted to the optical module case temperature to be monitored or used for modulation and other parameters (L.U.T.s). There are 39 entries (bytes) at address A6: 96-134 (60-86h) where the OEM can enter the temperature difference between the chip (sensed) temperature and the measured module case temperature over the operating temperature range. Table 7 shows the correspondence between the entries and temperature intervals.

The resolution of this table is 0.5ºC/bit. The number entered should be twice the temperature difference. For example if the chip-case temperature difference is 5ºC, the value to be entered should be 2x5=10.

Entry	Address	Temperature Range
0	A6: 96 (60h)	t ≤ -45 ºC
1	A6: 97 (61h)	-44 ºC ≤ t ≤ -41 ºC
2	A6: 98 (62h)	-40 ºC ≤ t ≤ -37 ºC
…… ……		
36	A6: 97 (61h)	96 ºC ≤ t ≤ 99 ºC
37	A6: 97 (61h)	100 ≤ t ≤ 103 ºC
38	A6: 134 (86h)	t ≥ 104 ºC

Table 7. L.U.T. for Temperature Reading Compensation

Alarms and Warnings Interrupt Source Masking

Alarms and warnings set the flags and Interrupt when they are asserted if they are not masked (default). If an alarm or warning is masked, it will not set the Interrupt. Table 8 shows the locations of the masking bits. The warning or alarm is masked if the corresponding bit is set to 1.

Serial Address A2h		Default Value	Description
Byte	Bit		
248	7	0	Masking bit for Temp High Alarm interrupt source
	6	0	Masking bit for Temp Low Alarm interrupt source
	5	0	Masking bit for Voltage High Alarm interrupt source
	4	0	Masking bit for Voltage Low Alarm interrupt source
	3	0	Masking bit for Bias High Alarm interrupt source
	2	0	Masking bit for Bias Low Alarm interrupt source
	1	0	Masking bit for TX Power High Alarm interrupt source
	0	0	Masking bit for TX Power Low Alarm interrupt source
249	7	0	Masking bit for RX Power High Alarm interrupt source
	6	1	Masking bit for RX Power Low Alarm interrupt source
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

Table 8. Alarms Interrupt Sources Masking Bits

Serial Address A2h		Default Value	Description
Byte	**Bit**		
250	7	0	Masking bit for Temp High Warning interrupt source
	6	0	Masking bit for Temp Low Warning interrupt source
	5	0	Masking bit for Voltage High Warning interrupt source
	4	0	Masking bit for Voltage Low Warning interrupt source
	3	0	Masking bit for Bias High Warning interrupt source
	2	0	Masking bit for Bias Low Warning interrupt source
	1	0	Masking bit for TX Power High Warning interrupt source
	0	0	Masking bit for TX Power Low Warning interrupt source
251	7	0	Masking bit for RX Power High Warning interrupt source
	6	1	Masking bit for RX Power Low Warning interrupt source
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

Table 9. Warnings Interrupt Sources Masking Bits

Alarms and Warnings as TXFAULT Source

Alarms and warnings are not sources for TXFAULT with the default setting. To set alarms as a TXFAULT source set OEMCFG4 bit 6 to 1. To set warnings as a TXFAULT, source set OEMCFG4 bit 7 to 1. The alarms and warnings TXFAULT sources can be masked individually in the same way shown in Tables 7 and 8.

Alarms and Warnings Latch

Alarms and warnings are latched with the default setting, i.e., the flags once asserted remain ON until the register is read or TXDSABLE is toggled. If OEMCFG4 bit 5 is set to 1, the warnings are not latched and will be set and reset with the warning condition. Reading the register or toggling TXDISABLE will clear the flag. If OEMCFG4 bit 4 is set to 1, the alarms are not latched and will be set and reset with the alarm condition. Reading the register or toggling TXDISABLE will clear the flag.

SMBus Multipart Support

If more than one MIC3002 device shares the same serial interface and multipart mode is selected on them (OEMCFG5 bit 3 = 1), then pin 7 and pin 20 become SMBus address bits 3 and 4 respectively. Therefore, the parts should have a different setting on those pins to create four address combinations based upon pin 7 and pin 20 state, (00, 01, 10, 11) where 0 is a pull down to GND and 1 is a pull up to VCC. The parts come from the factory with the same address (A0) and multipart mode OFF (OEMCFG5 bit 3 = 0). After power up, write 1 to OEMCFG5 bit 3 to turn ON multipart mode, which is done to all parts at the same time since they all respond to serial address A0 at this point. With multipart mode ON, the parts have different addresses based on the states of pins 7 and 20. Another option is to access each part individually, set their single mode address in OEMCFG2 bits [4-7] to different values and then turn OFF multipart mode to return to normal mode where the parts have new different address.

Calibration Modes

The default mode of calibration in the MIC3002 is external calibration, for which INTCAL bit (bit 0 in OEMCF3 register) is set to 0. The internal calibration mode is selected by setting INTCAL bit to 1.

A/ External Calibration

The voltage and temperature values returned by the MIC3002's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl and VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration.

SFF-8472 calls for a set of calibration constants to be stored by the transceiver OEM at specific non-volatile memory locations; refer to SFF-8472 specifications for memory map of calibration coefficient. The MIC3002 provides the non-volatile memory required for the storage of these constants. The Digital Diagnostic Monitoring Interface specification should be consulted for full details. Slopes and offsets are stored for use with voltage, temperature, bias current, and transmitted power measurements. Coefficients for a fourth-order polynomial are provided for use with received power measurements. The host system can retrieve these constants and use them to process the measured data.

Voltage

The voltage values returned by the MIC3002's A/D converter are internally calibrated. The binary values of VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration. Since VINh:VINl requires no processing, the corresponding slope should be set to one and the offset to zero.

Temperature

The temperature values returned by the MIC3002's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl are in the format called for by SFF-8472 under Internal Calibration.

Bias Current

Bias current is sensed via an external sense resistor as a voltage appearing between VILD+ and VILD-. The value returned by the A/D is therefore a voltage analogous to bias current. Bias current, IBIAS, is simply V_{VILD}/R_{SENSE}. The binary value in IBIASh (IBIASl is always zero) is related to bias current by:

$$I_{BIAS} = \frac{(0.300V)\left(\frac{IBIASh}{256}\right)}{R_{SENSE}} \quad (1)$$

The value of the least significant bit (LSB) of IBIASh is given by:

$$LSB(IBIASh) = \frac{0.300V}{256 \times R_{SENSE}} Amps = \frac{300mV}{256 \times R_{SENSE}} mA = \frac{1171.9}{R_{SENSE}} \mu A \quad (2)$$

Per SFF-8472, the value of the bias current LSB is 2µA. The conversion factor, "slope", needed is therefore:

$$Slope = \frac{1171.9\mu A}{512\mu A \times R_{SENSE}} = 2.289 \div R_{SENSE}$$

The tolerance of the sense resistor directly impacts the accuracy of the bias current measurement. It is recommended that the sense resistor chosen be 1% accurate or better. The offset correction, if needed, can be determined by shutting down the laser, i.e., asserting TXDISABLE, and measuring the bias current. Any non-zero result gives the offset required. The offset will be equal and opposite to the result of the "zero current" measurement.

TX Power

Transmit power is sensed via a resistor carrying the monitor photodiode current. In most applications, the signal at VMPD will be feedback voltage on FB. The VMPD voltage may be measured relative to GND or V_{DDA} depending on the setting of the BIASREF bit in OEMCFG1. The value returned by the A/D is therefore a voltage analogous to transmit power. The binary value in TXOPh (TXOPl is always zero) is related to transmit power by:

$$P_{TX}(mW) = \frac{K \times VREF\left(\frac{TXOPh}{256}\right)}{R_{SENSE}} = \frac{K \times (1220mV)\left(\frac{TXOPh}{256}\right)}{R_{SENSE}}$$
$$= \frac{K \times 4.7656 \times TXOPh}{R_{SENSE}} mW \quad (3)$$

For a given implementation, the value of R_{SENSE} is known. It is either the value of the external resistor or the chosen value of RFB used in the application. The constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends on the monitoring photodiode responsivity and coupling efficiency.

It should be noted that the APC circuit acts to hold the transmitted power constant. The value of transmit power reported by the circuit should only vary by a small amount as long as APC is functioning correctly.

RX Power

Received power is sensed as a voltage appearing at VRX. It is assumed that this voltage is generated by a sense resistor carrying the receiver photodiode current or by the RSSI circuit of the receiver. The value returned by the A/D is therefore a voltage analogous to received power. The binary values in RXOPh and RXOPl are related to receive power by:

$$RX(mW) = K \times VREF \times (256 \times RXOPh + RXOPl/16)/65536 \quad (4)$$

For a given implementation, the constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends upon the gain and efficiencies of the receiver. In SFF-8472 implementations, the external calibration constants can describe up to a fourth-order polynomial in case K is nonlinear.

B/ Internal Calibration

If the INTCAL bit in OEMCFG3 is set to 1 (internal calibration selected), the MIC3002 will process each piece of data coming out of the A/D converter before storing the result in memory. Linear slope/offset correction will be applied on a per-channel basis to the measured values for voltage, bias current, TX power, and RX power. Only compensation is applied to temperature.

The user must store the appropriate slope/offset parameters in memory at the time of transceiver calibration. In the case of RX power, a look-up table is provided that implements eight-segment piecewise-linear correction. This correction may be performed as a compensation of the receiver non-linearity over receive power level. If static slope/offset correction for RX power is desired, the eight coefficient sets can simply be made the same. The memory maps for these coefficients are shown in Tables 11 and 12. The user must enter the seven delimiters of the intervals that fit better the receiver response. The diagram in Figure 3 shows the link between the delimiters and the sets of slopes/offsets.

The slopes allow for the correction of gain errors. Each slope coefficient is an unsigned, sixteen-bit, fixed-point binary number in the format:

[mmmmmmmm.llllllll], where m is a data bit in the most-significant byte and l is a data bit in the least significant byte (5)

Slopes are always positive. The binary point is in between the two bytes, i.e., between bits 7 and 8. This provides a numerical range of 1/256 (0.00391) to 255.997 in steps of 1/256. The most significant byte is always stored in memory at the lower numerical address.

The offsets correct for constant errors in the measured data. Each offset is a signed, sixteen-bit, fixed-point binary number. The bit-weights of the offsets are the same as that of the final results. The sixteen-bit offsets provide a numerical range of –32768 to +32767 for voltage, bias current, transmit power, and receive power. The numerical range for the temperature offset is –32513 (–128°) to +32512 (+127°) in increments of 256 (1°). The format for offsets is:

[Smmmmmmmllllllll], where S is the sign bit (0 = positive, 1 = negative), m is a data bit in the most-significant byte and l is a data bit in the least significant byte (6)

The most significant byte is always stored in memory at the lower numerical address.

Calibration of voltage, bias current, and TX power are performed using the following calculation:

RESULTn = ADC_RESULTn x SLOPEn + OFFSETn (7)

Calibration of RX power is performed using the following calculation:

RESULT = ADC_RESULT x SLOPE(m) + OFFSET(m) (9)

where m represents one of the eight linearization intervals corresponding to the RX power level.

The results of these calculations are rounded to sixteen bits in length. If the seventeenth most significant bit is a one, the result is rounded up to the next higher value. If the seventeenth most significant bit is zero, the upper sixteen bits remain unchanged. The bit-weights of the offsets are the same as that of the final results. For SFF-8472 compatible applications, these bit-weights are given in Table 10.

Parameter	Magnitude of LSB
Voltage	100µV
Bias Current	2µA
TX Power	0.1µW
RX Power	0.1µW

Table 10. LSB Values of Offset Coefficients

Address(s)		Field Size	Name	Description
HEX	DEC			
48-49	72-73	2	RESERVED	Reserved. (There is no slope for temperature.) Do not write; reads undefined.
4A-4B	74-75	2	RESERVED	Reserved. (There is no offset for temperature.) Do not write; reads undefined.
4C-4D	76-77	2	VSLPh:VSLPl	Voltage slope; unsigned fixed-point; MSB is at lower physical address.
4E-4F	78-79	2	VOFFh:VOFFl	Voltage offset; signed fixed point; MSB is at lower physical address.
50-51	80-81	2	ISLPh:ISLPl	Bias current slope; unsigned fixed-point; MSB is at lower physical address.
52-53	82-83	2	IOFFh:IOFFl	Bias current offset; signed fixed point; MSB is at lower physical address.
54-55	84-85	2	TXSLPh: TXSLPl	TX power slope; unsigned fixed-point; MSB is at lower physical address.
56-57	86-87	2	TXOFFh: TXOFFl	TX power offset; signed fixed point; MSB is at lower physical address.

Table 11. Internal Calibration Coefficient Memory Map – Part I

Address(s)		Field Size	Name	Description
HEX	DEC			
28-29	40-41	2	RXSLP0h: RXSLP0l	RX power slope 0; unsigned fixed-point; MSB is at lower physical address.
2A-2B	42-43	2	RXOFF0h: RXOFF0l	RX power offset 0; signed twos-complement; MSB is at lower physical address.
2C-2D	44-45	2	RXSLP1h: RXSLP1l	RX power slope 1; unsigned fixed-point; MSB is at lower physical address.
2E-2F	46-47	2	RXOFF1h: RXOFF1l	RX power offset 1; signed twos-complement; MSB is at lower physical address.
30-31	48-49	2	RXSLP2h: RXSLP2l	RX power slope 2; unsigned fixed-point; MSB is at lower physical address.
32-33	50-51	2	RXOFF2h: RXOFF2l	RX power offset 2; signed twos-complement; MSB is at lower physical address.
34-35	52-53	2	RXSLP3h: RXSLP3l	RX power slope 3; unsigned fixed-point; MSB is at lower physical address.
36-37	54-55	2	RXOFF3h: RXOFF3l	RX power offset 3; signed twos-complement; MSB is at lower physical address.
38-39	56-57	2	RXSLP4h: RXSLP4l	RX power slope 4; unsigned fixed-point; MSB is at lower physical address.
3A-3B	58-59	2	RXOFF4h: RXOFF4l	RX power offset 4; signed twos-complement; MSB is at lower physical address.
3C-3D	60-61	2	RXSLP5h: RXSLP5l	RX power slope 5; unsigned fixed-point; MSB is at lower physical address.
3E-3F	62-63	2	RXOFF5h: RXOFF5l	RX power offset 5; signed twos-complement; MSB is at lower physical address.
40-41	64-65	2	RXSLP6h: RXSLP6l	RX power slope 6; unsigned fixed-point; MSB is at lower physical address.
42-43	66-67	2	RXOFF6h: RXOFF6l	RX power offset 6; signed twos-complement; MSB is at lower physical address.
44-45	68-69	2	RXSLP7h: RXSLP7l	RX power slope 7; signed twos-complement; MSB is at lower physical address.
46-47	70-71	2	RXOFF7h: RXOFF7l	RX power offset 7; signed fixed-point; MSB is at lower physical address.

Table 12. Internal Calibration Coefficient Memory Map – Part II

Address(s)		
HEX	DEC	Name
28-29 2A-2B	40-41 42-43	RXSLP0h: RXSLP0l RXOFF0h: RXOFF0l
2C-2D 2E-2F	44-45 46-47	RXSLP1h: RXSLP1l RXOFF1h: RXOFF1l
30-31 32-33	48-49 50-51	RXSLP2h: RXSLP2l RXOFF2h: RXOFF2l
34-35 36-37	52-53 54-55	RXSLP3h: RXSLP3l RXOFF3h: RXOFF3l
38-39 3A-3B	56-57 58-59	RXSLP4h: RXSLP4l RXOFF4h: RXOFF4l
3C-3D 3E-3F	60-61 62-63	RXSLP5h: RXSLP5l RXOFF5h: RXOFF5l
40-41 42-43	64-65 66-67	RXSLP6h: RXSLP6l RXOFF6h: RXOFF6l
44-45 46-47	68-69 70-71	RXSLP7h: RXSLP7l RXOFF7h: RXOFF7l

RXPWR <= Delimiter #1

Delimiter #1 < RXPWR <= Delimiter #2

Delimiter #2 < RXPWR <= Delimiter # 3

Delimiter #3 < RXPWR <= Delimiter #4

Delimiter #4 < RXPWR <= Delimiter #5

Delimiter #5 < RXPWR <= Delimiter #6

Delimiter #6 < RXPWR <= Delimiter #7

RXPWR > Delimiter #7

Delimiter	Address(s)	
	HEX	DEC
Delimiter #1	D0-D1	208-209
Delimiter #2	D2-D3	210-211
Delimiter #3	D4-D5	212-213
Delimiter #4	D6-D7	214-215
Delimiter #5	D8-D9	216-217
Delimiter #6	DA-DB	218-219
Delimiter #7	DC-DD	220-221

Figure 3. Internal Calibration RX Power Linear Approximation

Temperature Offset

In both internal and external calibration, the temperature offset is set in the temperature reading compensation LUT (see subsection above). Bit 5 in OMCFG5 (A6:1Ah) must be set to 1 in order to enable temperature reading compensation. Since the resolution of that L.U.T. is 0.5ºC, the entered value should be twice the real value. For example, if the content of the L.U.T. is 0 for all the entries and the offset is 5ºC, then the offset value to be added to the entries content is 10. The new content of the L.U.T. entries will be 0+10=10.

C/ ADC Result Registers Reading

The ADC result registers should be read as 16-bit registers under internal calibration while under external calibration they should be read as 8-bit or 16-bit registers at the MSB address. For example, TX power should be read under internal calibration as 16 bits at address $A2_h$: 66–67 and under external calibration as 8 bits at address $A2_h$: 66_h. 9-bit temperature results and 12-bit receive power results should always be read as 16-bit quantities.

RXPOT

A programmable, non-volatile digitally controlled potentiometer is provided for adjusting the gain of the receive power measurement signal chain in the analog domain. Five bits in the RXPOT register are used to set and adjust the position of potentiometer. RXPOT functions as a programmable divider or attenuator. It is adjustable in steps from 1:1 (no divider action) down to 1/32 in steps of 1/32. If RXPOT is set to zero, then the divider is bypassed completely. There will be no scaling of the input signal, and the resistor network will be disconnected from the VRX pin. At all other settings of RXPOT, there will be a 32kΩ (typical) load seen on VRX.

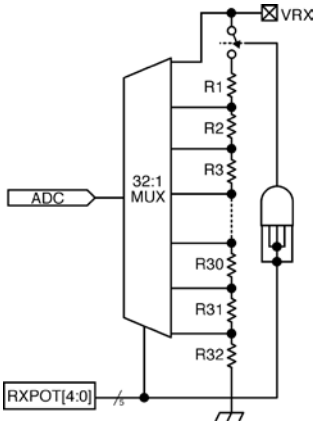


Figure 4. RXPOT Block Diagram

Laser Diode Bias Control

The MIC3002 can be configured to generate a constant bias current using electrical feedback, or regulate average transmitted optical power using a feedback signal from a monitor photodiode, refer to Figure 5. An operational amplifier is used to control laser bias current via the V_{BIAS} output. The VBIAS pin can drive a maximum of ±10mA. An external bipolar transistor provides current gain. The polarity of the op amp's output is programmable BIASREF in OEMCFG1 in order to accommodate either NPN or PNP transistors that drive common anode and common cathode laser, respectively. Additionally, the polarity of the feedback signal is programmable for use with either common-emitter or emitter-follower transistor circuits.