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MIC3003GFL

FOM Management IC with Internal Calibration

General Description

The MIC3003GFL is a fiber optic module controller which enables the implementation of sophisticated, hot-pluggable fiber optic transceivers with intelligent laser control and an internally calibrated Digital Diagnostic Monitoring Interface per SFF-8472. It essentially integrates all non-data path functions of an SFP/SFP+ transceiver into a tiny (3mm x 3mm) MLF® package. It also works well as a microcontroller peripheral in transponders or 10Gbps transceivers. The MIC3003GFL uses the same die as the MIC3003 with all its functions, but in a smaller package and different pin out.

A highly configurable automatic power control (APC) circuit controls laser bias. Bias and modulation are temperature compensated using dual DACs, an on-chip temperature sensor, and NVRAM look-up tables. A programmable internal feedback resistor provides a wide dynamic range for the APC. Controlled laser turn-on.

An analog-to-digital converter converts the measured temperature, voltage, bias current, transmit power, and received power from analog to digital. An EEPOT provides front-end adjustment of RX power. Each parameter is compared against user-programmed warning and alarm thresholds. Analog comparators and DACs provide fast monitoring of received power and critical laser operating parameters. Data can be reported as either internally calibrated or externally calibrated.

An interrupt output, power-on hour meter, and data-ready bits add user friendliness beyond SFF-8472. The interrupt output and data-ready bits reduce overhead in the host system. The power-on hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM.

In addition to the features listed above, the MIC3003 features an extended temperature range, options to mask alarms and warnings interrupt and TXFAULT, a reset signal source, and the ability to support up to four chips with the same address on the serial interface. It also supports eight-byte SMBus block writes.

Communication with the MIC3003 is via an industry standard 2-wire SMBus serial interface. Nonvolatile memory is provided for serial ID, configuration, and separate OEM and user scratchpad spaces.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

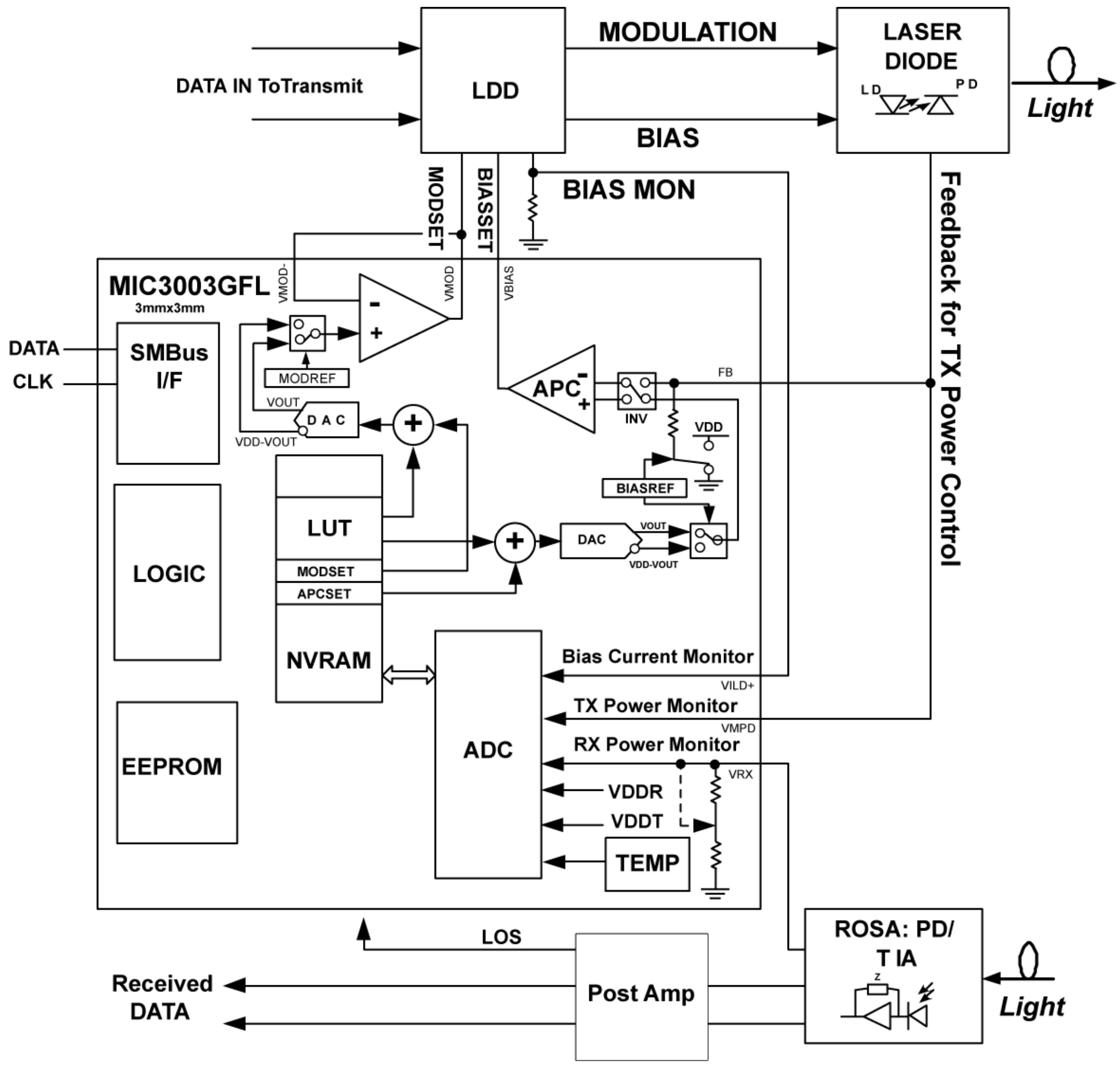
Features

- Packaged in a ultra small (3mm x 3mm) 24-pin MLF® package
- Extended temperature range
- Alarms and warnings interrupt and TXFAULT masks
- Capability to support up to four devices on one SMBus
- APC or constant-current laser bias
- Turbo mode for APC loop start-up and shorter laser turn on time
- Supports multiple laser types and bias circuit topologies
- Integrated digital temperature sensor
- Temperature compensation of modulation, bias, bias fault and alarm thresholds via NVRAM look-up tables
- NVRAM to support GBIC/SFP serial ID function
- User writable EEPROM scratchpad
- Reset signal compatible with some new systems requirements
- Diagnostic monitoring interface per SFF-8472
  - Monitors and reports critical parameters: temperature, bias current, TX and RX optical power, and supply voltage
  - S/W control and monitoring of TXFAULT, RXLOS, RATESELECT, and TXDISABLE
  - Internal or external calibration
  - EEPOT for adjusting RX power measurement
- Power-on hour meter
- Interrupt capability
- Extensive test and calibration features
- 2-wire SMBus-compatible serial interface
- SFP/SFP+ MSA and SFF-8472 compliant
- 3.0V to 3.6V power supply range
- 5V-tolerant I/O

Applications

- SFP/SFP+ optical transceivers
- SONET/SDH transceivers and transponders
- Fibre Channel transceivers
- 10Gbps transceivers
- Free space optical communications
- Proprietary optical links

Typical Application



Ordering Information

Part Number	Package Marking	Junction Temp. Range	Package Type	Lead Finish
MIC3003GFL	GFL 3003 with Pb-Free bar-line indicator	–45°C to +105°C	24-pin (3mm x 3mm) MLF®	Pb-Free, NiPdAu
MIC3003GFLTR(1)	GFL 3003 with Pb-Free bar-line indicator	–45°C to +105°C	24-pin (3mm x 3mm) MLF®	Pb-Free, NiPdAu

Note:

1. Tape and Reel.

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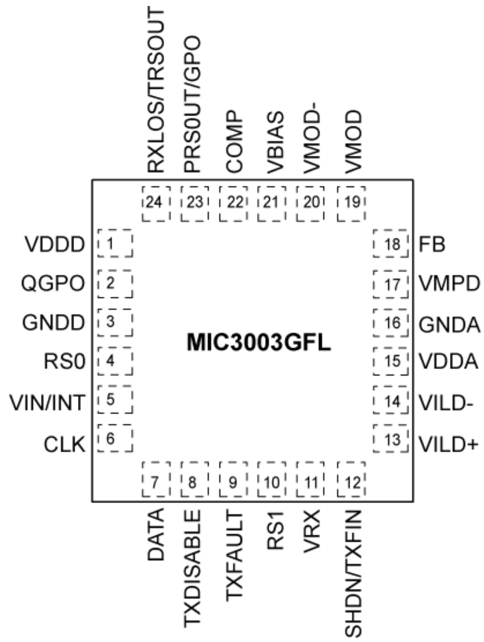
Pin Configuration



24-Pin MLF® (ML)

Pin Description (MIC3003GFL only)

Pin Number	Pin Name	Pin Function
1	VDDD	Power supply input for digital functions.
2	QGPO	Open-drain output. Can be selected (via OEMCFG3 bit 7) to be an open-drain GPO or an active-low, open-drain, pulsed reset signal output controlled by the status of bits [0-2] of byte A2h: FFh.
3	GNDD	Ground return for digital functions.
4	RS0	Digital input. Receiver Rate Select input. OR'ed with soft rate select bit SRS0 to determine the state of the RRSOUT pin. The state of this pin is always reflected in the RS0S bit.
5	VIN/INT	If bit 4 (IE) in the USRCTL register is set to 0 (its default value), this pin is configured as an analog input. If IE bit is set to 1, this pin is configured as an open-drain output. Analog input: Multiplexed A/D input for monitoring supply voltage, with a 0V to 5.5V input range. Open-drain output: outputs the internally generated active-low interrupt signal /INT.
6	CLK	Digital input. Serial clock input.
7	DATA	Digital I/O, open-drain, bi-directional serial data input/output.
8	TXDISABLE	Digital input; Active high. The transmitter is disabled when this input is high or the STXDIS bit is set to 1. The state of this input is always reflected in the TXDIS bit.
9	TXFAULT	Digital Output; Open-Drain, with programmable polarity. If OEMCFG5 bit 4 is set to 0, a high level indicates a hardware fault impeding transmitter operation. If OEMCFG5 bit 4 is set to 1, a low level indicates a hardware fault impeding transmitter operation. The state of this pin is always reflected in the TXFLT bit.
10	RS1	Digital Input; Transmitter Rate Select Input; OR'ed with soft rate select bit SRS1 to determine the state of the TRSOUT pin. The state of this pin is always reflected in the RS1S bit.
11	VRX	Analog Input. Multiplexed A/D converter input for monitoring received optical power. The input range is 0 to V_{REF}. A 5-bit programmable EEPOT on this pin provides coarse calibration and ranging of the RX power measurement.

Pin Number	Pin Name	Pin Function
12	SHDN/TXFIN	Digital output/Input; programmable polarity. When used as shutdown output (SHDN), OEMCFG3 bit 2 set to 0, SHDN is asserted at the detection of a fault condition if OEMCFG4 bit 7 is set to 0. If OEMCFG4 bit 7 is set to 1, a fault condition will not assert SHDN. When programmed as TXFIN, it is an input for external fault signals to be OR'ed with the internal fault sources to drive TXFAULT.
13	VILD+	Analog Input. Multiplexed A/D input for monitoring laser bias current via a sense resistor (signal input); accommodates inputs referenced to V_{DD} or GND (see pin 14 description).
14	VILD–	Analog Input. Reference terminal for the multiplexed pseudo-differential A/D converter inputs for monitoring laser bias current via a sense resistor (VILD+ is the sensing input). Tie to V_{DD} or GND to reference the voltage sensed on VILD+ to V_{DD} or GND, respectively.
15	VDDA	Power supply input for analog functions.
16	GNDA	Ground return for analog functions.
17	VMPD	Analog Input. Multiplexed A/D converter input for monitoring transmitted optical power via a monitor photodiode. In most applications, VMPD will be connected directly to FB. The input range is 0 - V_{REF} or 0 - V_{REF}/4 depending upon the setting of the APC configuration bits
18	FB	Analog Input. Feedback voltage for the APC loop op-amp. Polarity and scale are programmable via the APC configuration bits I OEMCFG1. Connect to V_{BIAS} if APC is not used.
19	VMOD	Analog Output. Buffered DAC output to set the modulation current on the laser driver IC. Operates with either a 0– V_{REF} or a (V_{DD}–V_{REF}) – V_{DD} output swing so as to generate either a ground-referenced or a V_{DD} referenced programmed voltage. A simple external circuit can be used to generate a programmable current for those drivers that require a current rather than a voltage input.
20	VMOD–	Analog input. This pin is the inverting terminal of the VMOD buffer op-amp. Connect to VMOD (gain = 1) or a feedback resistor network to set a different gain value.
21	VBIAS	Analog output. Buffered DAC output capable of sourcing or sinking up to 10mA under control of the APC function to drive an external transistor or the APCSET pin of a laser diode driver for laser diode DC bias. The output and feedback polarity are programmable to accommodate either an NPN or a PNP transistor to drive a common-anode or common-cathode laser diode.
22	COMP	Analog output. Compensation terminal for the APC loop. Connect a capacitor between this pin and GNDA or V_{DDA} with the appropriate value to tune the APC loop time constant to a desirable value.
23	RRSOUT/ GPO	Digital Output. Open-Drain or push-pull. If OEMCFG3 bit 4 is set to 0, RRSOUT is selected. It represents the receiver rate select as per SFF. This output is controlled by the SRS0 bit OR'ed with RS0 input and is open drain only. If OEMCFG3 bit 4 is set to 1, GPO is selected. General-purpose, non-volatile output, it is controlled by the GPO configuration bits in OEMCFG3.
24	RXLOS/ TRSOUT	Digital output. This programmable polarity, open-drain outputs has two purposes: If OEMCFG6 bit 2 = 0, indicates the loss of the received signal as indicated by a level of received optical power below the programmed RXLOS comparator threshold; may be wire-OR'ed with external signals. Normal operation is indicated by a low level when OEMCFG6 bit 3 is set to 0 and a high level when OEMCFG6 bit 3 is set to 1. RXLOS is de-asserted when VRX > LOSFLTn. The LOS bit reflects the state of RXLOS whether driven by the MIC3003 or an external circuit. If OEMCFG6 bit 2 = 1, TRSOUT is selected. This signal represents the transmitter rate select as per the SFF specification. This output is controlled by the SRS1 bit OR'ed with the RS1 input.

Absolute Maximum Ratings(1)

Power Supply Voltage, V_{DD} ....+3.8V
Voltage on CLK, DATA, TXFAULT, VIN, RXLOS,
TXDISABLE, RS0, RS1 .... –0.3V to +6.0V
Voltage On Any Other Pin.....................–0.3V to V_{DD}+0.3V
Power Dissipation, T_A = 85°C 1.5W
Junction Temperature (T_J) .... 150°C
Storage Temperature (T_S)...................... –65°C to +150°C
Soldering (20 sec.) 260ºC
ESD Ratings(3)
Human Body Model... 2kV
Machine Model 300V

Operating Ratings(2)

Power Supply Voltage, V_{DDA}/V_{DDD} .... +3.0V to +3.6V
Ambient Temperature Range (T_A) ....–40°C to +105°C
Package Thermal Resistance
MLF® (θ_{JA}) ....60°C/W

Electrical Characteristics

For typical values, T_A = 25°C, V_{DDA} = V_{DDD} = +3.3V, unless otherwise noted. **Bold** values are guaranteed for +3.0V ≤ (V_{DDA} = V_{DDD}) ≤ 3.6V, $T_{(min)} \le T_A \le T_{(min)}$, (8)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
I_{DD}	Supply Current	CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE low; all DACs at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
		CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE high; FLTDAC at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
V_{POR}	Power-on Reset Voltage	All registers reset to default values; A/D conversions initiated.		2.9	2.98	V
V_{UVLO}	Under-Voltage Lockout Threshold	Note 5	2.5	2.73		V
V_{HYST}	Power-on Reset Hysteresis Voltage			170		mV
t_{POR}	Power-on Reset Time	V_{DD} > $V_{POR,}$ Note 4		50		µs
V_{REF}	Reference Voltage		1.210	1.225	1.240	V
$\Delta V_{REF}/\Delta V_{DDA}$	Voltage Reference Line Regulation			1.7		mV/V
Temperature-to-Digital Converter Characteristics						
	Local Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C, Note 6		±1	±3	°C
t_{CONV}	Conversion Time	Note 4			60	ms
t_{SAMPLE}	Sample Period				100	ms
Voltage-to-Digital Converter Characteristics (V_{RX}, V_{AUX}, V_{BIAS}, V_{MPD}, V_{ILD}±)						
	Voltage Measurement Error	–40°C ≤ T_A ≤ +105°C, Note 6		±1	±2.0	%fs
t_{CONV}	Conversion Time	Note 4			10	ms
t_{SAMPLE}	Sample Period	Note 4			100	ms

Notes:
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.
5. The MIC3003 will attempt to enter its shutdown state when V_{DD} falls below V_{UVLO}. This operation requires time to complete. If the supply voltage falls too rapidly, the operation may not be completed.
6. Does not include quantization error.

Voltage Input, V_{IN} (Pin 5 used as an ADC Input)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	$-0.3\ V \le V_{DD} \le 3.6V$	GNDA		5.5	V
I_{LEAK}	Input Current	$V_{IN} = V_{DD}$ or GND; $V_{AUX} = V_{IN}$		55		µA
C_{IN}	Input Capacitance			10		pF

Digital-to-Voltage Converter Characteristics (V_{MOD}, V_{BIAS})

	Accuracy	$-40°C \le T_A \le +105°C$, Note 7		±1	2.0	%fs
t_{CONV}	Conversion Time	Note 8			20	ms
DNL	Differential Non-linearity Error	Note 8		±0.5	±1	LSB

Bias Current Sense Inputs, $V_{ILD}+$, $V_{ILD}-$

V_{ILD}	Differential Input Signal Range, $\lvert V_{ILD}^+ - V_{ILD}^- \rvert$		0		$V_{REF}/4$	mV
I_{IN+}	V_{ILD}^+ input current				±1	µA
I_{IN-}	V_{ILD}^- input current	V_{ILD}^- referred to V_{DDA}		+150		µA
	$\lvert V_{ILD}^+ - V_{ILD}^- \rvert = 0.3V$	V_{ILD}^- referred to GND		-150		µA
C_{IN}	Input Capacitance			10		pF

APC Op Amp, FB, V_{BIAS}, COMP

GBW	Gain Bandwidth Product	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient(4)			1		µV/°C
V_{OUT}	Output Voltage Swing	I_{OUT} = 10mA, SRCE bit = 1	GNDA		1.25	V
		I_{OUT} = -10mA, SRCE bit = 0	V_{DDA} -1.25		V_{DDA}	V
I_{SC}	Output Short-Circuit Current			55		mA
t_{SC}	Short Circuit Withstand Time	$T_J \le 150°C$, Note 8				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; gain = 1, to GND		55		dB
		C_{COMP} = 20pF; gain = 1, to V_{DD}		40		
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF, note 8			1	V/V
ΔV/Δt	Slew Rate	C_{COMP} = 20pF; gain = 1		3		V/µs
ΔRFB	Internal Feedback Resistor Tolerance			±20		%
ΔRFB/Δt	Internal Feedback Resistor Temperature Coefficient			25		ppm/C
I_{START}	Laser Start-up Current Magnitude	START = 01_h		0.375		mA
		START = 02_h		0.750		mA
		START = 04_h		1.500		mA
		START = 08_h		3.000		mA
C_{IN}	Pin Capacitance			10		pF

Notes:

7. Does not include quantization error.
8. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{MOD} Buffer Op-Amp, VMOD, V_{MOD}–						
GBW	Gain Bandwidth	C_{COMP} = 20pF; gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient			1		µV/°C
I_{BIAS}	V_{MOD}– Input Current			±0.1	±1	µA
V_{OUT}	Output Voltage Swing	I_{OUT} = ±1mA	GNDA+75		V_{DDA}-75	mV
I_{SC}	Output Short-Circuit Current			35		mA
t_{SC}	Short Circuit Withstand Time	T_J ≤ 150°C, Note 9				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; gain = 1, to GND		65		dB
		C_{COMP} = 20pF; gain = 1, to V_{DD}		44		dB
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF			1	V/V
ΔV/ΔT	Slew Rate	C_{COMP} = 20pF; gain = 1		1		V/µs
C_{IN}	Pin Capacitance			10		pF
Control and Status I/O, TXDISABLE, TXFAULT, RS0, RRSOUT(GPO), SHDN(TXFIN), RXLOS(TRSOUT), /INT, RS1, QGPO						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.0			V
V_{OL}	Low Output Voltage	I_{OL} ≤ 3mA			0.3	V
V_{OH}	High Output Voltage (applies to SHDN only)	I_{OH} ≤ 3mA			V_{DDD}–0.3	V
I_{LEAK}	Input Current				±1	µA
C_{IN}	Input Capacitance			10		pF
Transmit Optical Power Input, V_{MPD}						
V_{IN}	Input Voltage Range	Note 9	GNDA		V_{DDA}	V
V_{RX}	Input Signal Range	BIASREF=0			V_{REF}	V
		BIASREF=1	V_{DDA}–V_{REF}		V_{DDA}	V
C_{IN}	Input Capacitance	Note 9		10		pF
I_{LEAK}	Input Current				±1	µA
Received Optical Power Input, VRX, RXPOT						
	Input Voltage Range	Note 9	GNDA		V_{DDA}	V
V_{RX}	Valid Input Signal Range (ADC Input Range)		0		V_{REF}	V
$R_{RXPOT(32)}$	End-to-End Resistance	RXPOT = $1F_h$		32		KΩ
ΔRXPOT	Resistor Tolerance			±20		%
ΔRXPOT/ΔT	Resistor Temperature Coefficient			25		ppm/ºC
$\Delta V_{RX}/V_{RXPOT}$	Divider Ratio Accuracy	00 ≤ RXPOT ≤ $1F_h$	-5		+5	%
I_{LEAK}	Input Current	RXPOT = 0 (disconnected)			±1	µA
C_{IN}	Input Capacitance	Note 9		10		pF
I_{LEAK}	Input Current				±1	µA

Note:
9. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Control and Status I/O Timing, TXFAULT, TXDISABLE, RS0, RRSOUT, and RXLOS						
t_{OFF}	TXDISABLE Assert Time	From input asserted to optical output at 10% of nominal, C_{COMP} = 10nF.			**10**	µs
t_{ON}	TXDISABLE De-assert Time	From input de-asserted to optical output at 90% of nominal, C_{COMP} = 10nF.			**1**	ms
t_{INIT}	Initialization Time	From power on or transmitter enabled to optical output at 90% of nominal and TX_FAULT de-asserted. Note 10.			**300**	ms
t_{INIT2}	Power-on Initialization Time	From power on to APC loop-enabled.			**200**	ms
t_{FAULT}	TXFAULT Assert Time	From fault condition to TXFAULT assertion. Note 10.			95	µs
t_{RESET}	Fault Reset Time	Length of time TXDISABLE must be asserted to reset fault condition.	**10**			µs
t_{LOSS_ON}	RXLOS Assert Time	From loss of signal to RXLOS asserted.			95	µs
t_{LOSS_OFF}	RXLOS De-assert Time	From signal acquisition to LOS de-asserted.			**100**	µs
t_{DATA}	Analog Parameter Data Ready	From power on to valid analog parameter data available. Note 10			**400**	ms
t_{PROP_IN}	TXFAULT, TXDISABLE, RXLOS, RS0, RS1 Input Propagation Time	Time from input change to corresponding internal register bit set or cleared. Note 10.			**1**	µs
t_{PROP_OUT}	TXFAULT, TRSOUT, TRRSOUT, /INT, QGPO Output Propagation Time	From an internal register bit set or cleared to corresponding output change. Note 10.			**1**	µs
Fault Comparators						
FLTTMR	Fault Suppression Timer Clock Period	Note 10.	**0.475**	0.5	**0.525**	ms
	Accuracy		-3		+3	%/fs
t_{REJECT}	Glitch Rejection	Maximum length pulse that will not cause output to change state. Note 10.	4.5			µs
V_{SAT}	Saturation Detection Threshold	High level		95		%VDDA
		Low level		5		%VDDA
Power-On Hour Meter						
	Timebase Accuracy	0°C ≤ T_A ≤ +70°, Note 10.	**+5**		**-5**	%
		–40°C ≤ T_A ≤ +105°C	**+10**		**-10**	%
	Resolution	Note 10.		10		hours
Non-Volatile (FLASH) Memory						
t_{WR}	Write Cycle Time, Note 11	Measured from the SMBus STOP condition of a one-byte to eight-byte write transaction. Note 10.			**13**	ms
	NVRAM Data Retention		**100**			years
Endurance	Maximum permitted number of write cycles to any single NVRAM location		**10,000**			cycles

Notes:

10. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.
11. The MIC3003 will not respond to serial bus transactions during an EEPROM write cycle. The host will receive a NACK response during t_{WR}.

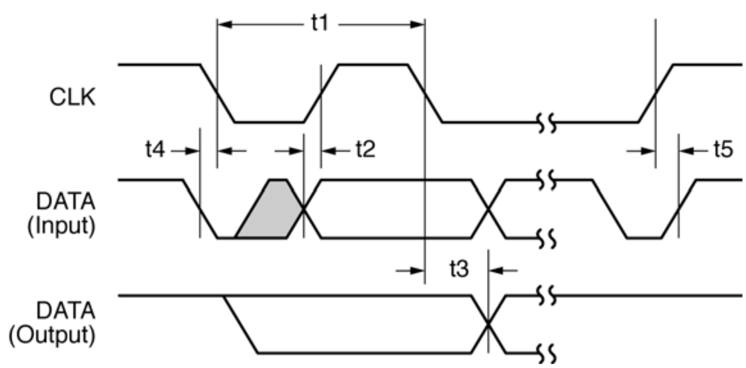
Serial Data I/O Pin, Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Output Voltage	I_{OL} = 3mA			**0.4**	V
		I_{OL} = 6mA			**0.6**	V
V_{IL}	Low Input Voltage				**0.8**	V
V_{IH}	High Input Voltage		**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 12		10		pF
Serial Clock Input, CLK						
V_{IL}	Low Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V			**0.8**	V
V_{IH}	High Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V	**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 12		10		pF
Serial Interface Timing(4)						
t_1	CLK (clock) Period		**2.5**			µs
t_2	Data In Setup Time to CLK High		**100**			ns
t_3	Data Out Stable After CLK Low		**300**			ns
t_4	Data Low Setup Time to CLK Low	Start Condition	**100**			ns
t_5	Data High Hold Time After CLK High	Stop Condition	**100**			ns
t_{DATA}	Data Ready Time	From power on to completion of one set of ADC conversions; analog data available via serial interface.			**400**	ms
QGPO Reset Pulse Timing						
t_1	QGPO reset pulse low duration	OEMCFG3 bit 7 = 1 A2h:255 (FFh) [2-0] switch to 111	**112.5**	125	137.5	µs
t_2	QGPO reset de-assertion to the clearing of A2:FFh bits 2:0	OEMCFG3 bit 7 = 1 A2h:255 (FFh) [2-0] ≠ 111	**20.25**	22.5	24.75	ms

Note:

12. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Serial Interface Timing Diagram



Serial Interface Timing

Serial Interface Address Maps

Address (Decimal)	Field Size (Bytes)	Name	Description
0 –95	96	Serial ID defined by SFP MSA	General-purpose NVRAM; R/W under valid OEM password.
96 – 127	32	Vendor Specific	Vendor specific EEPROM
128 – 255	128	Reserved	Reserved for future use. General-purpose NVRAM; R/W under valid OEM password.

Table 1. Serial Interface Address Map, Device Address = $A0_h$

Address(s)		Field Size (Bytes)		
Hex	**Dec**		**Name**	**Description**
00-27	0-39	40	Alarm and Warning Thresholds	High/low limits for warnings and alarms; writeable using the OEM password; read-only otherwise.
28-37	40-55	16	Reserved	Reserved – do not write; reads undefined.
38-5B	56-91	36	Calibration Constants	Numerical constants for external calibration; writeable using the OEM password; read-only otherwise.
5C-5E	92-94	3	Reserved	Reserved – do not write; reads undefined.
5F	95	1	Checksum	General-purpose NVRAM; writeable using the OEM password; read-only otherwise.
60-69	96-105	10	Analog Data	Real time analog parameter data.
6A-6D	106-109	4	Reserved	Reserved – do not write; reads undefined.
6E	110	1	Control/Status Register	Control and status bits.
6F	111	1	Rate Select Control	Bits [7-6] control the use of the RS0 and RS1 inputs and the SRS0 and SRS1 register bits.
70-71	112-113	2	Alarm Flags	Alarm status bits; read-only.
72-73	114-115	2	Reserved	Reserved – do not write; reads undefined.
74-75	116-117	2	Warning Flags	Warning status bits; read-only.
76	118	1	Extended Control/Status Register	Additional control and status bits.
77	119	1	Reserved	Reserved – do not write; reads undefined.
78-7E	120-126	7	OEMPW	OEM password entry field. The four-byte OEM password location can be selected to be 78h-7Bh (120-123) by setting OEMCFG5 bit 2 to 0 (default) or 7Bh-7Eh (123-126) by setting OEMCFG5 bit 2 to a one.
7F	127	1	Vendor-specific	Vendor specific. Reserved – do not write; reads undefined.
80-F7	128-247	120	User Scratchpad	User-writeable EEPROM. General-purpose NVRAM.
F8-F9	248-249	2	Alarms Masks	Bit = 0: Corresponding alarm not masked. Bit = 1: Corresponding alarm masked.
FA-FB	250-251	2	Warnings Masks	Bit = 0: Corresponding warning not masked. Bit = 1: Corresponding warning masked.
FC-FD	252-253	2	Reserved	Reserved – do not write; reads undefined.
FE	254	1	USRCTL	End-user control and status bits.
FF	255	1	RESETOUT	Bits [2:0] of this register control the QGPO reset output (pin 2) If OEMCFG3 bit 7 is set to 1.

Table 2. Serial Interface Address Map, Device Address = A2

Address(s)		Field Size (Bytes)	Name	Description
Hex	Dec			
00-3F	0-63	64	BIASLUT1	First 64 entries of the bias current temperature compensation LUT (Look-up Table) The additional 12 entries are located in A6: 58h – 63h.
40-7F	64-127	64	MODLUT1	First 64 entries of the modulation current temperature compensation LUT. The additional 12 entries are located in A6:.64h – 6Fh.
80-BF	128-191	64	IFTLUT1	First 64 entries of the bias current fault threshold temperature compensation LUT. The additional 12 entries are located in A6: 70h - 7Bh.
C0-FF	192-255	64	HATLUT1	First 64 entries of the bias current high alarm threshold temperature compensation LUT. The additional 12 entries are located in A6: 7C-87h.

Table 3. Serial Interface Address Map (Temperature Compensation Tables), Device Address = $A4_h$

Address(s)		Field Size (Bytes)	Name	Description
Hex	Dec			
00	0	1	OEMCFG0	OEM configuration register 0
01	1	1	OEMCFG1	OEM configuration register 1
02	2	1	OEMCFG2	OEM configuration register 2
03	3	1	APCSET0	APC setpoint register 0
04	4	1	APCSET1	APC setpoint register 1
05	5	1	APCSET2	APC setpoint register 2
06	6	1	MODSET0	Modulation setpoint register 0
07	7	1	IBFLT	Bias current fault-comparator threshold. This register is temperature compensated.
08	8	1	TXPFLT	TX power fault threshold
09	9	1	LOSFLT	RX LOS fault-comparator threshold
0A	10	1	FLTTMR	Fault comparator timer setting
0B	11	1	FLTMSK	Fault source mask bits
0C-0F	12-15	4	OEMPWSET	Password for access to OEM areas
10	16	1	OEMCAL0	OEM calibration register 0
11	17	1	OEMCAL1	OEM calibration register 1
12	18	1	LUTINDX	Look-up table index read-back
13	19	1	OEMCFG3	OEM configuration register 3
14	20	1	APCDAC	Reads back current APC DAC value (setpoint+offset)
15	21	1	MODDAC	Reads back current modulation DAC value (setpoint+offset)
16	22	1	OEMREAD	Reads back OEM calibration data
17	23	1	LOSFLTn	LOS de-assert threshold
18	24	1	RXPOT	RXPOT tap selection
19	25	1	OEMCFG4	OEM configuration register 4
1A	26	1	OEMCFG5	OEM configuration register 5
1B	27	1	OEMCFG6	OEM configuration register 6
1C-1D	28-29	2	SCRATCH	Reserved – do not write; reads undefined.
1E	30	1	MODSET 1	Modulation setpoint register 1

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
1F	31	1	MODSET 2	Modulation setpoint register 2
20-27	32-39	8	POHDATA	Power-on hour meter scratchpad
28-47	40-71	32	RXLUT	RX power internal calibration coefficient table. Eight sets of slope and offset coefficients provide a piecewise-linear transform for the receive power ADC result.
48-57	72-87	16	CALCOEF	Slope and offset coefficients used for temperature, voltage, bias current, and transmit power internal calibration
58-63	88-99	12	IFTLUT2	Additional 12 entries of the bias current fault threshold temperature compensation LUT.
64-6F	100-111	12	BIASLUT2	Additional 12 entries of the bias current temperature compensation LUT.
70-7B	112-123	12	MODLUT2	Additional 12 entries of the modulation current temperature compensation LUT.
7C-87	124-135	12	HATLUT2	Additional 12 entries of the bias current high alarm threshold temperature compensation LUT.
88-CF	136-207	72	SCRATCH	OEM scratchpad area
D0-DD	208-221	14	RXLUTSEG/ SCRATCH	Receive power calibration segment delimiters. Each of the eight segments can have its own slope and offset coefficient. Used to refine the shape of the piecewise-linear function used for receive power in internal calibration mode. These bytes may also be part of the OEM scratch pad if the hard coded delimiters option is selected, see the description of OEMCFG6
DE-FA	222-250	29	SCRATCH	OEM scratchpad area
FB-FC	251-252	2	POH	Power on hour meter result; read-only
FD	253	1	Data Ready Flags	Data ready bits for each measured parameter; read-only
FE	254	1	MFG_ID	Manufacturer identification (Micrel's manufacturer ID is 42, 2Ah)
FF	255	1	DEV_ID	Device ID and die revision

Table 4. Serial Interface Address Map (OEM Configuration Registers), Device Address = $A6_h$

Block Diagram

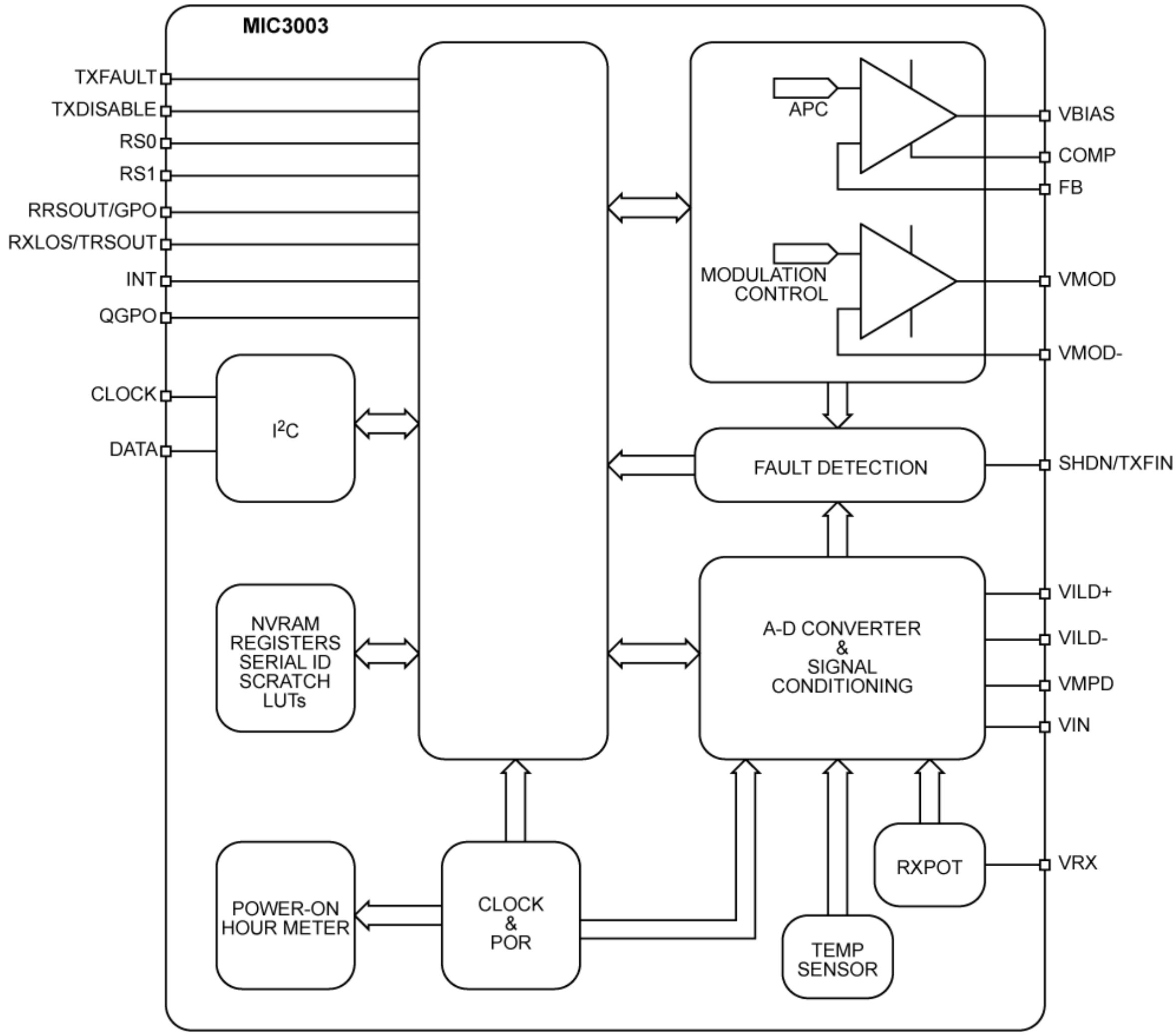


Figure 1. MIC3003 Block Diagram

Analog-to-Digital Converter/Signal Monitoring

A block diagram of the monitoring circuit is shown below. Each of the five analog parameters monitored by the MIC3003 is sampled in sequence. All five parameters are sampled and the results updated within the t_{CONV} duration given in the "Electrical Characteristics" section. In OEM mode, the channel that is normally used to measure V_{IN} may be assigned to measure the level of the V_{DDA} pin or one of five other nodes. This provides a kind of analog loopback for debug and test purposes. The V_{AUX} bits in OEMCFG0 control which voltage source is being sampled. The various V_{AUX} channels are level-shifted differently depending on the signal source, resulting in different LSB values and signal ranges. See Table 5.

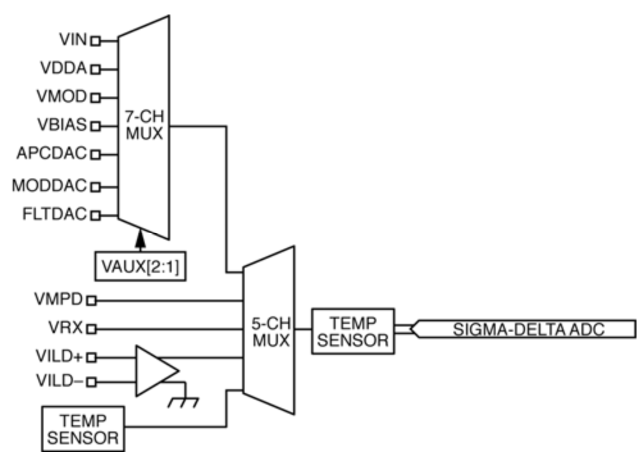


Figure 2. Analog-to-Digital Converter Block Diagram

Channel	ADC Resolution (bits)	Conditions	Input Range (V)	LSB[1]
TEMP	8 or 9		N/A	1°C or 0.5°C
VAUX	8	See Table 6		
VMPD	8	GAIN = 0; BIASREF = 0	GNDA - V_{REF}	4.77mV
		GAIN = 0; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF})	
		GAIN = 1; BIASREF = 0	GNDA - V_{REF}/4	1.17mV
		GAIN = 1; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF}/4)	
VILD	8	VILD- = VDDA	V_{DDA} – (V_{DDA} – V_{REF})	4.77mV
		VILD- = GNDA	GNDA - V_{REF}	
VRX	12	RXPOT = 00	0 - V_{REF}	0.298mV

Table 5. A/D Input Signal Ranges and Resolutions

Note:

1. Assumes typical VREF value of 1.22V.

Channel	VAUX [2:0]	Input Range (V)	LSB[1] (mV)
V_{IN}	000 = 00_h	0.5V to 5.5V	25.6mV
V_{DDA}	001 = 01_h	0.5V to 5.5V	25.6mV
V_{BIAS}	010 = 02_h	0.5V to 5.5V	25.6mV
V_{MOD}	011 = 03_h	0.5V to 5.5V	25.6mV
APCDAC	100 = 04_h	0V to V_{REF}	4.77mV
MODDAC	101 = 05_h	0V to V_{REF}	4.77mV
FLTDAC	110 = 06_h	0V to V_{REF}	4.77mV

Table 6. V_{AUX} Input Signal Ranges and Resolutions

Note:

1. Assumes typical V_{REF} value of 1.22V.

Alarms and Warnings Interrupt Source Masking

Alarm and warning violations set the flags in the Alarm and Warning Status Registers, and also assert the interrupt output if they are not masked. If an alarm or warning is masked, it will not set the interrupt. Table 8 shows the locations of the masking bits. The warning or alarm is masked if the corresponding bit is set to 1.

Serial Address A2h		Default Value	Description
Byte	Bit		
248	7	0	Masking bit for Temperature High Alarm interrupt source
	6	0	Masking bit for Temperature Low Alarm interrupt source
	5	0	Masking bit for Voltage High Alarm interrupt source
	4	0	Masking bit for Voltage Low Alarm interrupt source
	3	0	Masking bit for Bias High Alarm interrupt source
	2	0	Masking bit for Bias Low Alarm interrupt source
	1	0	Masking bit for TX Power High Alarm interrupt source
	0	0	Masking bit for TX Power Low Alarm interrupt source
249	7	0	Masking bit for RX Power High Alarm interrupt source
	6	1	Masking bit for RX Power Low Alarm interrupt source
	[5-0]	Reserved	

Table 7. Alarms Interrupt Sources Masking Bits

Serial Address A2h		Default Value	Description
Byte	Bit		
250	7	0	Masking bit for Temperature High Warning interrupt source
	6	0	Masking bit for Temperature Low Warning interrupt source
	5	0	Masking bit for Voltage High Warning interrupt source
	4	0	Masking bit for Voltage Low Warning interrupt source
	3	0	Masking bit for Bias High Warning interrupt source
	2	0	Masking bit for Bias Low Warning interrupt source
	1	0	Masking bit for TX Power High Warning interrupt source
	0	0	Masking bit for TX Power Low Warning interrupt source
251	7	0	Masking bit for RX Power High Warning interrupt source
	6	1	Masking bit for RX Power Low Warning interrupt source
	[5-0]	Reserved	

Table 8. Warnings Interrupt Sources Masking Bits

hbwhelp@micrel.com or (408) 955-1690

Alarms and Warnings as TXFAULT Source

Alarms and warnings are not sources for TXFAULT with the default setting. To set alarms as a TXFAULT source set OEMCFG4 bit 6 to 1. To set warnings as a TXFAULT, source set OEMCFG4 bit 7 to 1. The alarms and warnings TXFAULT sources can be masked individually in the same way shown in Tables 7 and 8.

Latching of Alarms and Warnings

Alarms and warnings are latched by default, i.e., once asserted the flags remain ON until the register is read or TXDSABLE is toggled. If OEMCFG4 bit 5 is set to 1, the warnings are not latched and will be set and reset with the warning condition. Reading the register or toggling TXDISABLE will clear the flag. If OEMCFG4 bit 4 is set to 1, the alarms are not latched and will be set and reset with the alarm condition. Reading the register or toggling TXDISABLE will clear the flag.

SMBus Multipart Support

If more than one MIC3003GFL device shares the same serial interface and multipart mode is selected on them (OEMCFG5 bit 3 = 1), then pin 12 and pin 23 become SMBus address bits 3 and 4 respectively. Therefore, the parts should have a different setting on those pins to create four address combinations based upon the state of pin 12 and pin 23 state, (00, 01, 10, 11) where 0 is a pull down to GND and 1 is a pull up to VCC. The parts come from the factory with the same address (A0) and multipart mode off (OEMCFG5 bit 3 is 0). After power up, write 1 to OEMCFG5 bit 3 to turn ON multipart mode, which is done to all parts at the same time since they all respond to serial address A0 at this point. With multipart mode on, the parts have now different addresses based on the states of pins 12 and 23. Another option is to access each part individually, set their single mode address in OEMCFG2 bits [4-7] to different values and then turn off multipart mode to return to normal mode where the parts have new different addresses.

QGOP Pin Function

QGOP can be used in GOP mode as a general purpose output by setting OEMCFG3 bit 7 to 0, or as in RESET mode as a reset signal output by setting OEMCFG3 bit 7 to 1.

If RESET mode is selected, the reset signal state is controlled by RSETOUT (A2:FFh bits [2-0]). By default, these three bits are 000, and the QGPO output is undriven (state: High). When the three bits are written to 111, QGPO's open-drain output will be driven low for 125 µs (typical), after which QGPO reenters the undriven state. The RESETOUT field is cleared from 111 to 000 22.5 ms (typical) after the de-assertion edge of QGPO. Other values of this delay may be selected by setting TRSTCLR (OEMCFG2 bits [2-0]) to different values as shown on table.

If Reset mode in OEMCFG3 is not selected, these three bits have no function.

TRSTCLR [2-0]	Delay from QGPO Switching high to RESETOUT clear
000	Zero delay
001	17.5 ms typical
010	22.5 ms typical (default)
011	27 ms typical
100	45 ms typical

Table 9. RESETOUT Clear Delay

Calibration Modes

The default mode of calibration in the MIC3003 is external calibration, for which the INTCAL bit (bit 0 in OEMCFG3 register) is set to 0. The internal calibration mode is selected by setting INTCAL to 1.

A/ External Calibration

The voltage and temperature values returned by the MIC3003's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl and VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration.

SFF-8472 calls for a set of calibration constants to be stored by the transceiver OEM at specific non-volatile memory locations; refer to the SFF-8472 specifications for the memory map of the calibration coefficients. The MIC3003 provides the non-volatile memory required for the storage of these constants. The Digital Diagnostic Monitoring Interface specification should be consulted for full details. Slopes and offsets are stored for use with voltage, temperature, bias current, and transmitted power measurements. Coefficients for a fourth-order polynomial are provided for use with received power measurements. The host system can retrieve these constants and use them to process the measured data.

Voltage

The voltage values returned by the MIC3003's A/D converter are internally calibrated. The binary values of VOLTh:VOLTl are in the format called for by SFF-8472 under Internal Calibration. Since VINh:VINl requires no processing, the corresponding slope should be set to one and the offset to zero.

Temperature

The temperature values returned by the MIC3003's A/D converter are internally calibrated. The binary values of TEMPh:TEMPl are in the format called for by SFF-8472 under Internal Calibration.

The temperature value may be offset by storing a value in A6:74(4Ah). The temperature offset is a six-bit signed quantity with .5 degrees C resolution.

The temperature offset coefficient at A6:74(4Ah) is used in the same way in both internal and external calibration modes.

Bias Current

Bias current is sensed via an external sense resistor as a voltage appearing between VILD+ and VILD-. The value returned by the A/D is therefore a voltage analogous to bias current. Bias current, IBIAS, is simply V_{VILD}/R_{SENSE}. The binary value in IBIASh (IBIASl is always zero) is related to bias current by:

$$I_{BIAS} = \frac{(0.3V)\frac{IBIASh}{255}}{R_{SENSE}} \qquad \textbf{(1)}$$

The value of the least significant bit (LSB) of IBIASh is given by:

$$LSB(IBIASh) = \frac{0.3v}{255 \times R_{SENSE}} Amps = \frac{300mV}{255 \times R_{SENSE}}$$

$$mA = \frac{1176.9}{R_{SENSE}} \mu A \qquad \textbf{(2)}$$

Per SFF-8472, the value of the bias current LSB is 2μA. The necessary conversion factor, "slope", is therefore:

$$Slope = \frac{1176.5\mu A}{512\mu A \times R_{SENSE}} = 2.298 + R_{SENSE}$$

The tolerance of the sense resistor directly impacts the accuracy of the bias current measurement. It is recommended that the sense resistor chosen be 1% accurate or better. The offset correction, if needed, can be determined by shutting down the laser, i.e., asserting TXDISABLE, and measuring the bias current. Any non-zero result gives the offset required. The offset will be equal and opposite to the result of the "zero current" measurement.

TX Power

Transmit power is sensed via a resistor carrying the monitor photodiode current. In most applications, the signal at VMPD will be feedback voltage on FB. The VMPD voltage may be measured relative to GND or V_{DDA} depending on the setting of the BIASREF bit in OEMCFG1. The value returned by the A/D is therefore a voltage analogous to transmit power. The binary value in TXOPh (TXOPl is always zero) is related to transmit power by:

$$PTX(mW) = \frac{K \times VREF \frac{TXOPh}{255}}{R_{SENSE}} = \frac{K \times (1220mV)\frac{TXOPh}{255}}{R_{SENSE}}$$

$$= \frac{K \times 4.7843 \times TXOPh}{R_{SENSE}} mW \qquad \textbf{(3)}$$

For a given implementation, the value of R_{SENSE} is known. It is either the value of the external resistor or the selected internal value of R_{FB}. The constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends on the monitoring photodiode responsively and coupling efficiency.

It should be noted that the APC circuit acts to hold the transmitted power constant. The value of transmit power reported by the circuit should only vary by a small amount as long as the APC is functioning correctly.

RX Power

Received power is sensed as a voltage appearing at VRX. It is assumed that this voltage is generated by a sense resistor carrying the receiver photodiode current or by the RSSI circuit of the receiver. The value returned by the A/D is therefore a voltage analogous to received power. The binary values in RXOPh and RXOPl are related to receive power by:

$$RX(mW) = K \times VREF \times (256 \times RXOPh + RXOPl/16) \bullet 65536 \quad \textbf{(4)}$$

For a given implementation, the constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends upon the gain and efficiencies of the receiver. In SFF-8472 implementations, the external calibration constants can describe up to a fourth-order polynomial in case K is nonlinear.

B/ Internal Calibration

If the INTCAL bit in OEMCFG3 is set to 1 (internal calibration selected), the MIC3003 will process each piece of data coming out of the A/D converter before storing the result in result register. Linear slope/offset correction will be applied on a per-channel basis to the measured values for voltage, bias current, TX power, and RX power. Only offset is applied to temperature.

The user must store the appropriate slope/offset coefficients in memory at the time of transceiver calibration. In the case of RX power, a look-up table is provided that implements eight-segment piecewise-linear correction. This correction may be performed as a compensation of the receiver non-linearity over temperature or receive power level. If static slope/offset correction for RX power is desired, the eight coefficient sets can simply be made the same. The user has the option to select between using preset hard-coded delimiters values or programmable delimiters where delimiters corresponding to the best linear approximation intervals of a specific receiver can be entered. The latter option will use an additional fourteen (14) bytes from the OEM scratch pad A6h:208-221(DO_h-DD_h). OEMCFG6 bits [6:5] are used to select between these options. The memory maps for the calibration coefficients are shown in Tables 11 and 12. If the programmable delimiters option is selected, the user must enter the seven delimiters of the intervals that best fit the receiver response. The diagram in Figure 3 shows the link between the delimiters and the sets of slopes and offsets.

Slopes Coefficients

The slopes allow for the correction of gain errors. Each slope coefficient is an unsigned, sixteen-bit, fixed-point binary number in the format:

$$[mmmmmmmm.llllllll] \quad \textbf{(5)}$$

where m is a data bit in the most-significant byte and l is a data bit in the least significant byte

Slopes are always positive. The decimal point is in between the two bytes, i.e., between bits 7 and 8. This provides a numerical range of 1/256 (0.00391) to 255.997 in steps of 1/256. The most significant byte is always stored in memory at the lower numerical address.

Offset coefficients

The offsets correct for constant errors in the measured data. Each offset, apart from temperature, is a signed, sixteen-bit, fixed-point binary number. The bit-weights of the offsets are the same as that of the final results. The sixteen-bit offsets provide a numerical range of –32768 to +32767 for voltage, bias current, transmit power, and receive power.

The numerical range for the six-bit temperature offset is –32 (–16 °C) to +31 (+15.5 °C) in increments of .5 °C. The two most significant bits of the temperature offset coefficient are ignored by the MIC3003.

Computing Internal Calibration Results

Calibration of voltage, bias current, and TX power are performed using the following calculation:

$$RESULTn = ADC\_RESULTn \times SLOPEn + OFFSETn \quad \textbf{(6)}$$

Calibration of RX power is performed using the following calculation:

$$RESULT = ADC\_RESULT \times SLOPE(m) + OFFSET(m) \quad \textbf{(7)}$$

where m represents one of the eight linearization intervals corresponding to the RX power level.

The results of these calculations are rounded to sixteen bits. If the seventeenth bit is a one, the result is rounded up to the next higher value. If the seventeenth bit is zero, the upper sixteen bits remain unchanged. The bit-weights of the offsets are the same as that of the final results. For SFF-8472 compatible applications, these bit-weights are given in Table 10.

Parameter	Magnitude of LSB
Voltage	100µV
Bias Current	2µA
TX Power	0.1µW
RX Power	0.1µW

Table 10. LSB Values of Offset Coefficients

Address(s)		Field Size	Name	Description
HEX	DEC			
48-49	72-73	2	RESERVED	Reserved. There is no slope for temperature. Do not write; reads undefined.
4A-4B	74-75	2	TOFFh:TOFFl	Temperature offset; signed six-bit integer offset with an LSB resolution of .5 degrees C per bit. The two most significant bits of TOFFh are ignored. TOFFl is not used. Note that TOFFh is also used in external calibration mode.
4C-4D	76-77	2	VSLPh:VSLPl	Voltage slope; unsigned fixed-point; MSB is at lower physical address.
4E-4F	78-79	2	VOFFh:VOFFl	Voltage offset; signed integer; MSB is at lower physical address.
50-51	80-81	2	ISLPh:ISLPl	Bias current slope; unsigned fixed-point; MSB is at lower physical address.
52-53	82-83	2	IOFFh:IOFFl	Bias current offset; signed integer; MSB is at lower physical address.
54-55	84-85	2	TXSLPh: XSLPl	TX power slope; unsigned fixed-point; MSB is at lower physical address.
56-57	86-87	2	TXOFFh: TXOFFl	TX power slope; unsigned fixed-point; MSB is at lower physical address.

Table 11. Internal Calibration Coefficient Memory Map – Part I

Address(s)		Field Size	Name	Description
HEX	DEC			
28-29	40-41	2	RXSLP0h: RXSLP0l	RX power slope 0; unsigned fixed-point; MSB is at lower physical address.
2A-2B	42-43	2	RXOFF0h: RXOFF0l	RX power offset 0; signed integer; MSB is at lower physical address.
2C-2D	44-45	2	RXSLP1h: RXSLP1l	RX power slope 1; unsigned fixed-point; MSB is at lower physical address.
2E-2F	46-47	2	RXOFF1h: RXOFF1l	RX power offset 1; signed integer; MSB is at lower physical address.
30-31	48-49	2	RXSLP2h: RXSLP2l	RX power slope 2; unsigned fixed-point; MSB is at lower physical address.
32-33	50-51	2	RXOFF2h: RXOFF2l	RX power offset 2; signed integer; MSB is at lower physical address.
34-35	52-53	2	RXSLP3h: RXSLP3l	RX power slope 3; unsigned fixed-point; MSB is at lower physical address.
36-37	54-55	2	RXOFF3h: RXOFF3l	RX power offset 3; signed integer; MSB is at lower physical address.
38-39	56-57	2	RXSLP4h: RXSLP4l	RX power slope 4; unsigned fixed-point; MSB is at lower physical address.
3A-3B	58-59	2	RXOFF4h: RXOFF4l	RX power offset 4; signed integer; MSB is at lower physical address.
3C-3D	60-61	2	RXSLP5h: RXSLP5l	RX power slope 5; unsigned fixed-point; MSB is at lower physical address.
3E-3F	62-63	2	RXOFF5h: RXOFF5l	RX power offset 5; signed integer; MSB is at lower physical address.
40-41	64-65	2	RXSLP6h: RXSLP6l	RX power slope 6; unsigned fixed-point; MSB is at lower physical address.
42-43	66-67	2	RXOFF6h: RXOFF6l	RX power offset 6; signed integer; MSB is at lower physical address.
44-45	68-69	2	RXSLP7h: RXSLP7l	RX power slope 7; signed integer; MSB is at lower physical address.
46-47	70-71	2	RXOFF7h: RXOFF7l	RX power offset 7; signed fixed-point; MSB is at lower physical address.

Table 12. Internal Calibration Coefficient Memory Map – Part II

Address(s)		Name
HEX	DEC	
28-29 2A-2B	40-41 42-43	RXSLP0h: RXSLP0l RXOFF0h: RXOFF0l
2C-2D 2E-2F	44-45 46-47	RXSLP1h: RXSLP1l RXOFF1h: RXOFF1l
30-31 32-33	48-49 50-51	RXSLP2h: RXSLP2l RXOFF2h: RXOFF2l
34-35 36-37	52-53 54-55	RXSLP3h: RXSLP3l RXOFF3h: RXOFF3l
38-39 3A-3B	56-57 58-59	RXSLP4h: RXSLP4l RXOFF4h: RXOFF4l
3C-3D 3E-3F	60-61 62-63	RXSLP5h: RXSLP5l RXOFF5h: RXOFF5l
40-41 42-43	64-65 66-67	RXSLP6h: RXSLP6l RXOFF6h: RXOFF6l
44-45 46-47	68-69 70-71	RXOFF7h: RXOFF7l RXSLP7h: RXSLP7l

RXPWR <= Delimiter #1
Delimiter #1 < RXPWR <= Delimiter #2
Delimiter #2 < RXPWR <= Delimiter # 3
Delimiter #3 < RXPWR <= Delimiter #4
Delimiter #4 < RXPWR <= Delimiter #5
Delimiter #5 < RXPWR <= Delimiter #6
Delimiter #6 < RXPWR <= Delimiter #7
RXPWR > Delimiter #7

Delimiter	Address(s)	
	HEX	DEC
Delimiter #1	D0-D1	208-209
Delimiter #2	D2-D3	210-211
Delimiter #3	D4-D5	212-213
Delimiter #4	D6-D7	214-215
Delimiter #5	D8-D9	216-217
Delimiter #6	DA-DB	218-219
Delimiter #7	DC-DD	220-221

Figure 3. Internal Calibration RX Power Linear Approximation

C/ Reading the ADC Result Registers

The ADC result registers should be read as 16-bit registers under internal calibration while under external calibration they should be read as 8-bit or 16-bit registers at the MSB address. For example, TX power should be read under internal calibration as 16 bits at address A2h: 66h–67h and under external calibration as 8 bits at address A2h: 66h. 9-bit temperature results and 12-bit receive power results should always be read as 16-bit quantities.

Reading the result registers using two-byte burst reads on the SMBus guarantees that the two bytes are coherent with each other—that is, they form a matched result pair. If the two bytes were read separately, it is possible that the internal result could be updated between the reads, leading to an incorrect ADC result.

RXPOT

A programmable, non-volatile digitally controlled potentiometer is provided for adjusting the gain of the receive power measurement signal chain in the analog domain. Five bits in the RXPOT register are used to set and adjust the position of potentiometer. RXPOT functions as a programmable divider or attenuator. It is adjustable in steps from 1:1 (no divider action) down to 1/32 in steps of 1/32. If RXPOT is set to zero, then the divider is bypassed completely. There will be no scaling of the input signal, and the resistor network will be disconnected from the VRX pin. At all other settings of RXPOT, there will be a 32kΩ (typical) load seen on VRX.

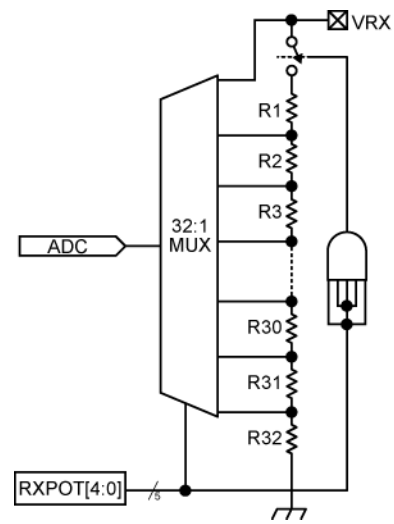


Figure 4. RXPOT Block Diagram

Laser Diode Bias Control

The MIC3003 can be configured to generate a constant bias current using electrical feedback, or regulate average transmitted optical power using a feedback signal from a monitor photodiode, as shown in Figure 5. An operational amplifier is used to control laser bias current via the VBIAS output. The VBIAS pin can drive a maximum of ±10mA. An external bipolar transistor provides current gain. The polarity of the op amp's output is programmable with BIASREF (bit-5 in OEMCFG1) in order to accommodate either NPN or PNP transistors that drive common anode and common cathode laser, respectively. Additionally, the polarity of the feedback signal is programmable for use with either common-emitter or emitter-follower transistor circuits.