Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MIC4606

85V Full-Bridge MOSFET Drivers with Adaptive Dead Time and Shoot-Through Protection

Features

- 5.5V to 16V Gate Drive Supply Voltage Range
- Advanced Adaptive Dead Time
- Intelligent Shoot-Through Protection
- MIC4606-1: 4 Independent TTL Inputs
- MIC4606-2: 2 PWM Inputs
- Enable Input For On/Off Control
- On-Chip Bootstrap Diodes
- Fast 35 ns Propagation Times
- Drives 1000 pF Load With 20 ns Rise And Fall Times
- Low Power Consumption: 235 µA Total Quiescent Current
- Separate High- And Low-Side Undervoltage Protection
- –40°C to +125°C Junction Temperature Range

Applications

- Full-Bridge Motor Drives
- Power Inverters
- High Voltage Step-Down Regulators
- Distributed Power Systems
- Stepper Motors

General Description

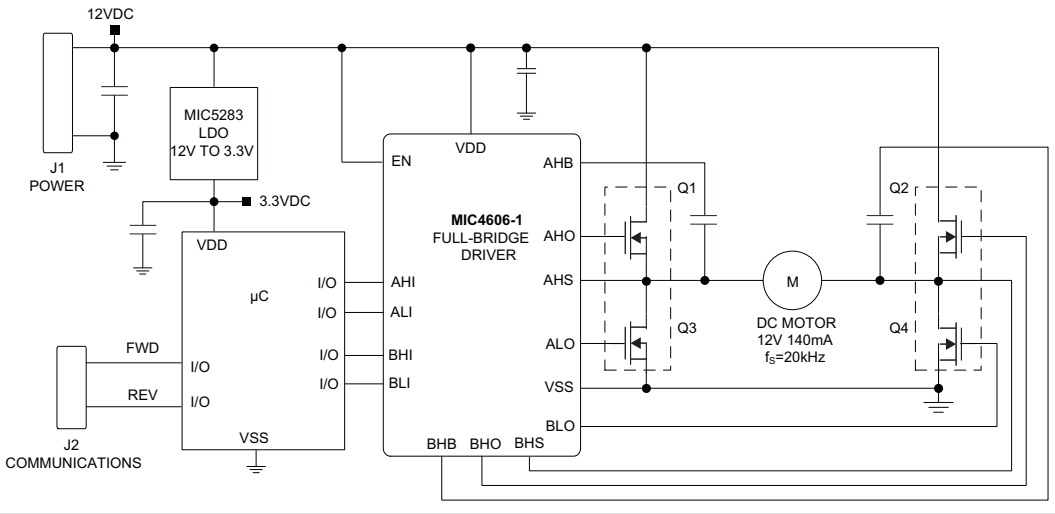
The MIC4606 is an 85V full-bridge MOSFET driver that features adaptive dead time and shoot-through protection. The adaptive dead time circuitry actively monitors both sides of the full-bridge to minimize the time between high-side and low-side MOSFET transitions, thus maximizing power efficiency. Antishoot-through circuitry prevents erroneous inputs and noise from turning both MOSFETs of each side of the bridge on at the same time.

The MIC4606 also offers a wide 5.5V to 16V operating supply range to maximize system efficiency. The low 5.5V operating voltage allows longer run times in battery-powered applications. Additionally, the MIC4606's adjustable gate drive sets the gate drive voltage to V_{DD} for optimal MOSFET $R_{DS(ON)}$, which minimizes power loss due to the MOSFET's $R_{DS(ON)}$.

The MC4606-1 features four independent inputs while the MIC4606-2 utilizes two PWM inputs, one for each side of the H-bridge. The MIC4606-1 and MIC4606-2 are available in a 16-pin 4 x 4 QFN and a 16-pin 4 x 5 TSSOP package with an operating temperature range of –40°C to 125°C.

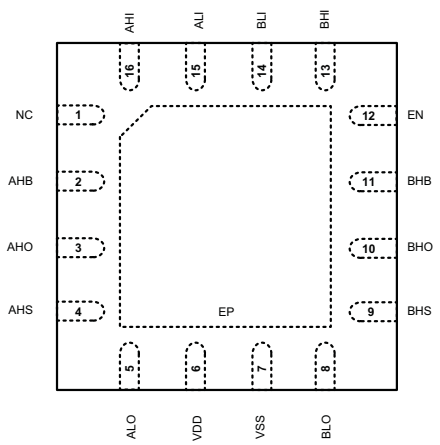
Typical Application Circuit

MIC4606
4x4 QFN
(12V Motor Drive Configuration)

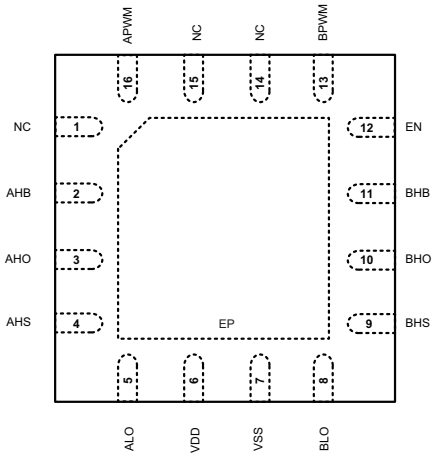


Package Types

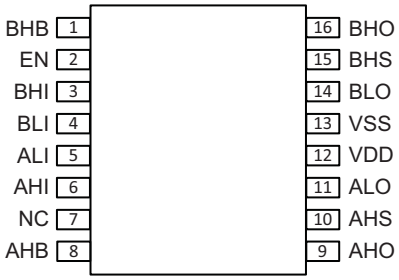
MIC4606-1
16-pin VQFN (NUA)
4 mm x 4 mm



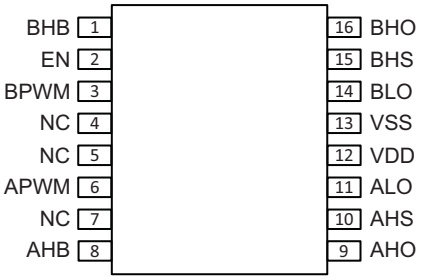
MIC4606-2
16-pin VQFN (NUA)
4 mm x 4 mm



MIC4606-1
16-pin TSSOP (D8X)
4 mm x 5 mm



MIC4606-2
16-pin TSSOP (D8X)
4 mm x 5 mm



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings † (Note 1)

Supply Voltage, V_{DD}, $V_{xHB} – V_{xHS}$ ..... –0.3V to +18V
Input Voltage, V_{xLI}, V_{xHI}, V_{EN} ..... –0.3V to V_{DD} +0.3V
Voltage on xLO (V_{xLO}) ..... –0.3V to V_{DD} +0.3V
Voltage on xHO (V_{xHO}) ..... V_{HS} – 0.3V to V_{HB} +0.3V
Voltage on xHS (continuous) ..... –1V to 90V
Voltage on xHB 108V
Average Current in VDD to HB Diode ..... 100 mA
ESD Protection On All Pins (Note 2) ..... ±1 kV HBM, ±200V MM

Operating Ratings ††

Supply Voltage, V_{DD}, [decreasing V_{DD}] ..... 5.25V to 16V
Supply Voltage, V_{DD}, [increasing V_{DD}] ..... 5.5V to 16V
Enable Voltage (V_{EN}) ..... 0V to V_{DD}
Voltage on xHS ..... –1V to 85V
Voltage on xHS (100 ns repetitive transient) ..... –5V to 90V
HS Slew Rate 50V/ns
Voltage on xHB ..... V_{HS} to V_{DD}
and/or ..... V_{DD} –1V to V_{DD} +85V

† Notice: Exceeding the absolute maximum ratings may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: "x" in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).

2: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS (Note 1, 2)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current						
V_{DD} Quiescent Current	I_{DD}	—	200	**350**	µA	xLI = xHI = 0V
VDD Shutdown Current	I_{DDSH}	—	2.5	**5**	µA	EN = 0V with xHS = floating;
		—	40	**100**		EN = 0V, xLI, xHI = 12V or 0V
V_{DD} Operating Current	I_{DDO}	—	0.35	**0.5**	mA	f_S = 20 kHz
Total xHB Quiescent Current	I_{HB}	—	35	**75**	µA	xLI = xHI = 0V or xLI = 0V and xHI =5V

Note 1: Specification for packaged product only.

2: x in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: xLI/xHI mode with inputs non-overlapping, assumes xHS low before xLI goes high and xLO low before xHI goes high).

5: PWM mode (MIC4606-2) or LI/HI mode (MIC4606-1) with overlapping xLI/xHI inputs.

ELECTRICAL CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Total xHB Operating Current	I_{HBO}	—	30	**400**	µA	f_S = 20 kHz
xHB to V_{SS} Quiescent Current	I_{HBS}	—	0. 5	5	µA	V_{xHS} = V_{xHB} = 90V
xHB to VSS Operating Current	I_{HBSO}	—	3	**10**	µA	f_S = 20 kHz
Input (TTL: xLI, xHI, EN) (Note 2, 3)						
Low-Level Input Voltage	V_{IL}	**—**	—	**0.8**	V	—
High-Level Input Voltage	V_{IH}	**2.2**	—	**—**	V	—
Input Voltage Hysteresis	V_{HYS}	**—**	0.1	**—**	V	—
Input Pull-Down Resistance	R_I	**100**	300	**500**	kΩ	xHI/xLI inputs
		50	150	**250**	kΩ	xPWM inputs
Under-Voltage Protection						
V_{DD} Falling Threshold	V_{DDR}	**4.0**	4.4	**4.9**	V	—
V_{DD} Threshold Hysteresis	V_{DDH}	—	0.25	—	V	—
xHB Falling Threshold	V_{HBR}	**4.0**	4.4	**4.9**	V	—
xHB Threshold Hysteresis	V_{HBH}	—	0.25	—	V	—
Bootstrap Diode						
Low-Current Forward Voltage	V_{DL}	—	0.4	**0.70**	V	$I_{VDD-xHB}$ = 100 µA
High-Current Forward Voltage	V_{DH}	—	0.7	**1.0**	V	$I_{VDD-xHB}$ = 50 mA
Dynamic Resistance	R_D	—	3	**5.0**	Ω	$I_{VDD-xHB}$ = 50 mA
LO Gate Driver						
Low-Level Output Voltage	V_{OLL}	—	0.3	**0.6**	V	I_{xLO} = 50 mA
High-Level Output Voltage	V_{OHL}	—	0.5	**1.0**	V	I_{xLO} = –50 mA, V_{OHL} = V_{DD} - V_{xLO}
Peak Sink Current	I_{OHL}	—	1	—	A	V_{xLO} = 0V
Peak Source Current	I_{OLL}	—	1	—	A	V_{xLO} = 12V
HO Gate Driver						
Low-Level Output Voltage	V_{OLH}	—	0.3	**0.6**	V	I_{xHO} = 50 mA

Note 1: Specification for packaged product only.

2: x in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: xLI/xHI mode with inputs non-overlapping, assumes xHS low before xLI goes high and xLO low before xHI goes high).

5: PWM mode (MIC4606-2) or LI/HI mode (MIC4606-1) with overlapping xLI/xHI inputs.

ELECTRICAL CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
High-Level Output Voltage	V_{OHH}	—	0.5	**1.0**	V	I_{xHO} = –50 mA, V_{OHH} = V_{xHB} - V_{xHO}
Peak Sink Current	I_{OHH}	—	1	—	A	V_{xHO} = 0V
Peak Source Current	I_{OLH}	—	1	—	A	V_{xLO} = 12V
Switching Specifications (Note 4)						
Lower Turn-Off Propagation Delay (xLI Falling to xLO Falling)	t_{LPHL}	—	35	**75**	ns	—
Upper Turn-Off Propagation Delay (xHI Falling to xHO Falling)	t_{HPHL}	—	35	**75**	ns	—
Lower Turn-On Propagation Delay (xLI Rising to xLO Rising)	t_{LPLH}	—	35	**75**	ns	—
Upper Turn-On Propagation Delay (xHI Rising to xHO Rising)	t_{HPLH}	—	35	**75**	ns	—
Output Rise/Fall Time	t_R/t_F	—	20	—	ns	C_L = 1000 pF
Output Rise/Fall Time (3V to 9V)	t_R/t_F	—	0.8	—	µs	C_L = 0.1 µF
Minimum Input Pulse Width that Changes the Output	t_{PW}	—	50	—	ns	—
Switching Specifications (Note 5)						
Delay from xPWM High (or xLI Low) to xLO Low	t_{LOOFF}	—	35	75	ns	—
xLO Output Voltage Threshold for Low-Side FET to be Considered Off	V_{LOOFF}	—	1.9	—	V	—
Delay from xLO off to xHO High	t_{HOON}	—	35	75	ns	—
Delay from xPWM Low (or xHI Low) to xHO Low\	t_{HOOFF}	—	35	75	ns	—

Note 1: Specification for packaged product only.

2: x in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: xLI/xHI mode with inputs non-overlapping, assumes xHS low before xLI goes high and xLO low before xHI goes high).

5: PWM mode (MIC4606-2) or LI/HI mode (MIC4606-1) with overlapping xLI/xHI inputs.

ELECTRICAL CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{xHS} = 0V; No load on xLO or xHO; T_A = 25°C. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switch Node Voltage Threshold Signaling xHO is Off	V_{SWTH}	1	2.2	4	V	—
Delay Between xHO FET being considered Off to xLO Turning On	t_{LOON}	—	35	75	ns	—
For xHS Low/xLI High, Delay from xPWM/xHI Low to xLO High	t_{LOONHI}	—	80	**150**	ns	—
Force xLO On if V_{SWTH} is Not Detected	t_{SWTO}	**100**	250	**500**	ns	—

Note 1: Specification for packaged product only.

2: x in front of a pin name refers to either A or B. (e.g. xHI can be either AHI or BHI).

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: xLI/xHI mode with inputs non-overlapping, assumes xHS low before xLI goes high and xLO low before xHI goes high).

5: PWM mode (MIC4606-2) or LI/HI mode (MIC4606-1) with overlapping xLI/xHI inputs.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–60	—	+150	°C	—
Junction Operating Temperature	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, QFN-16Ld	θ_{JA}	—	51	—	°C/W	—
Thermal Resistance, TSSOP-16Ld	θ_{JA}	—	97.5	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TIMING DIAGRAMS

2.1 Non-Overlapping LI/HI Input Mode (MIC4606-1)

In LI/HI input mode, external xLI/xHI inputs are delayed to the point that xHS is low before xLI is pulled high and similarly xLO is low before xHI goes high

xHO goes high with a high signal on xHI after a typical delay of 35 ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35 ns (t_{HPHL}).

Likewise, xLI going high forces xLO high after typical delay of 35 ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35 ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

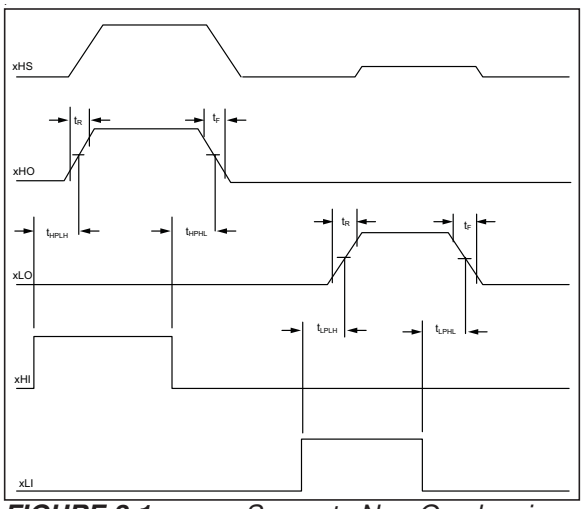


FIGURE 2-1: *Separate Non-Overlapping LI/HI Input Mode (MIC4606-1)*

2.2 Overlapping LI/HI Input Mode (MIC4606-1)

When xLI/xHI input high conditions overlap, xLO/xHO output states are dominated by the first output to be turned on. If xLI goes high (on) while xHO is high, xHO stays high until xHI goes low. After a delay of t_{HOOFF} and when xHS < 2.2V, xLO goes high with a delay of t_{LOON}. If xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250 ns will set “HS latch” allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35 ns delay gated by HI going low. Conversely, xHI going high (on) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to < 1.9V. Delay from xLI going low to xLO falling is t_{LOOFF} and delay from xLO < 1.9V to xHO being on is t_{HOON}.

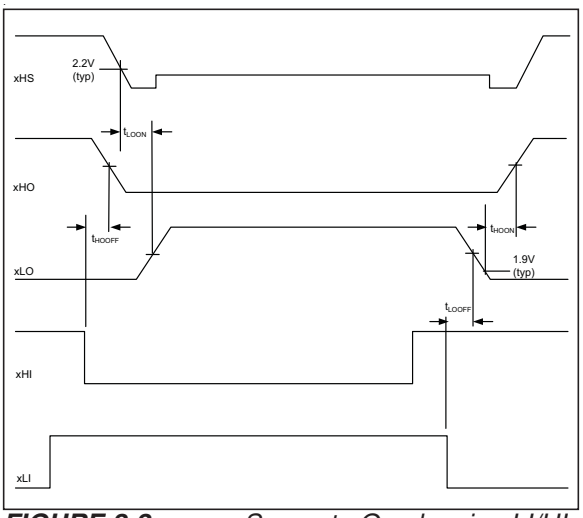


FIGURE 2-2: *Separate Overlapping LI/HI Input Mode (MIC4606-1).*

2.3 PWM Input Mode (MIC4606-2)

A low xPWM signal applied to the MIC4606-2 causes the xHO to go low, typically to 35 ns (t_{HOOFF}) after the xPWM input goes low. At this point, the switch node xHS, falls (1 − 2).

When the xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and the xLO goes high, typically within 35 ns (t_{LOON}) (3-4). The xHS falling below 2.2V sets a latch that can only be reset by the xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250 ns will set “HS latch” allowing xLO to go high. An 80 ns delay gated by xPWM going low may determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35 ns (t_{LOOFF}) (5− 6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35 ns (t_{HOON}) (7 − 8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

Note: All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

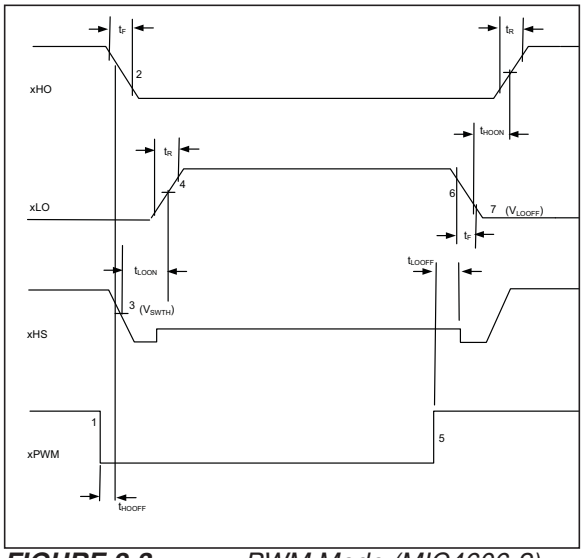


FIGURE 2-3: *PWM Mode (MIC4606-2).*

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

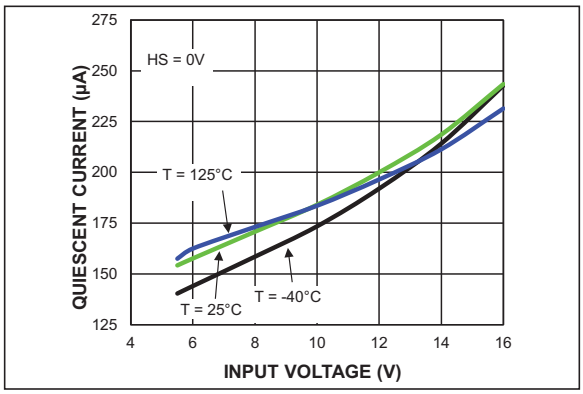


FIGURE 3-1: *V_{DD} Quiescent Current vs. Input Voltage.*

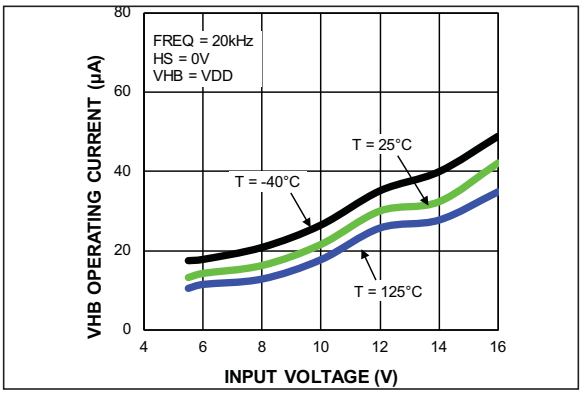


FIGURE 3-4: *V_{HB} Operating Current vs. Input Voltage.*

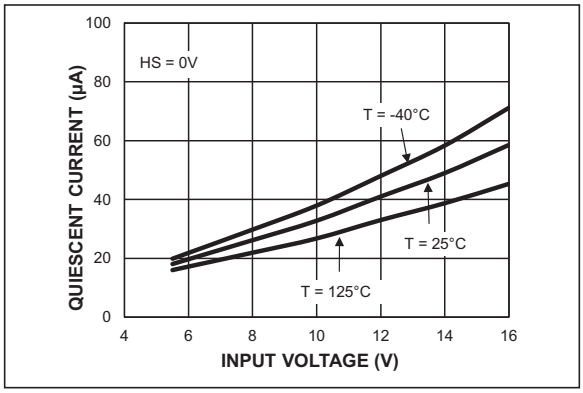


FIGURE 3-2: *Shutdown Current vs. Input Voltage.*

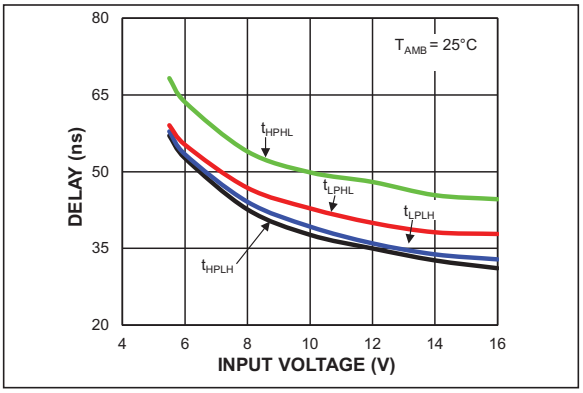


FIGURE 3-5: *Propagation Delay vs. Input Voltage.*

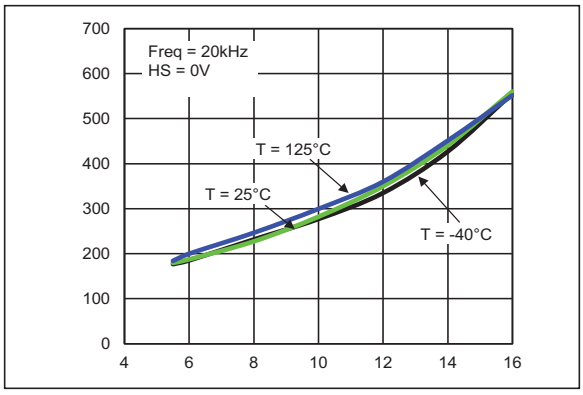


FIGURE 3-3: *V_{DD} Operating Current vs. Input Voltage.*

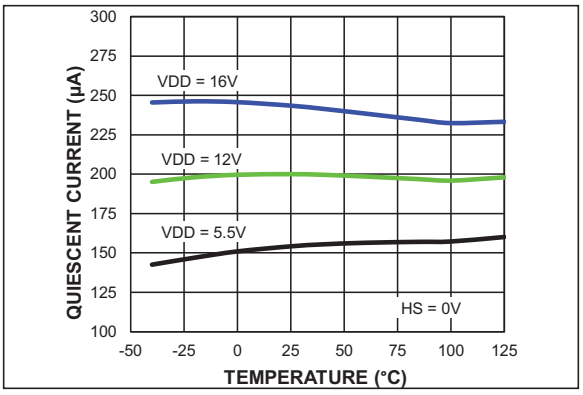


FIGURE 3-6: *V_{DD} Quiescent Current vs. Temperature.*

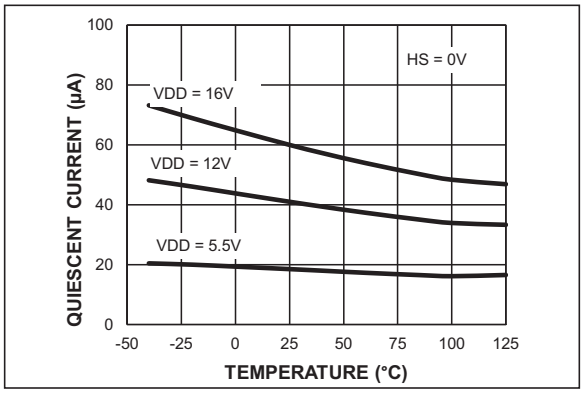


FIGURE 3-7: *Shutdown Current vs. Temperature.*

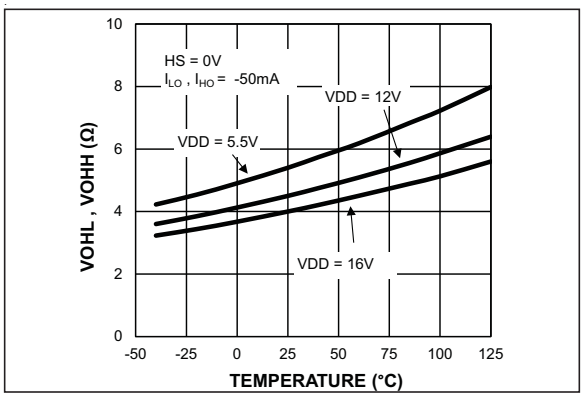


FIGURE 3-10: *High Level Output Resistance vs. Temperature.*

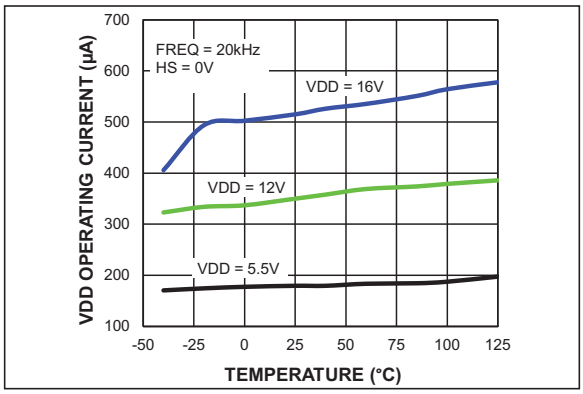


FIGURE 3-8: *V_{DD} Operating Current vs. Temperature.*

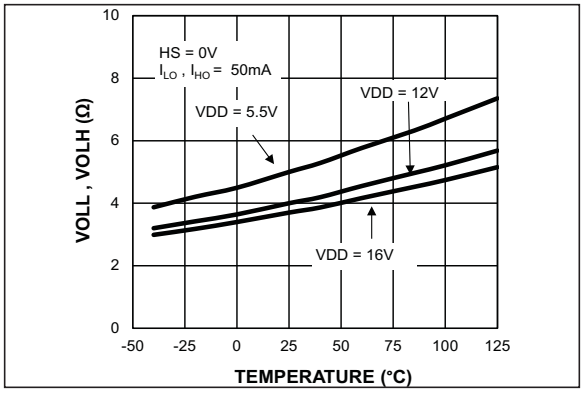


FIGURE 3-11: *Low Level Output Resistance vs. Temperature.*

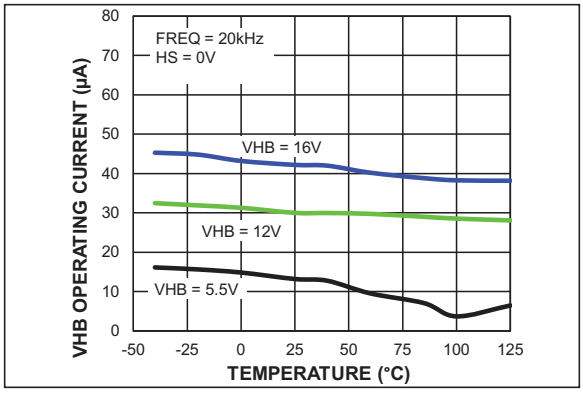


FIGURE 3-9: *V_{HB} Operating Current vs. Temperature.*

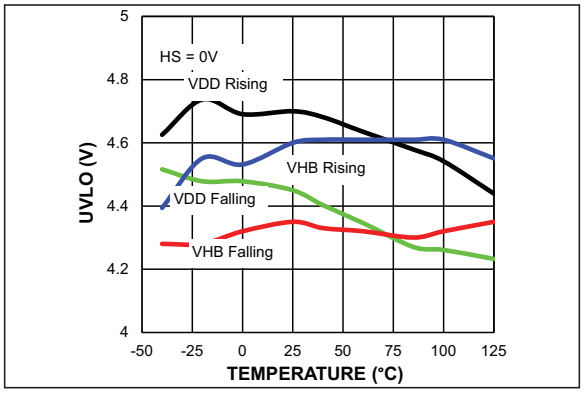


FIGURE 3-12: *UVLO Thresholds vs. Temperature.*

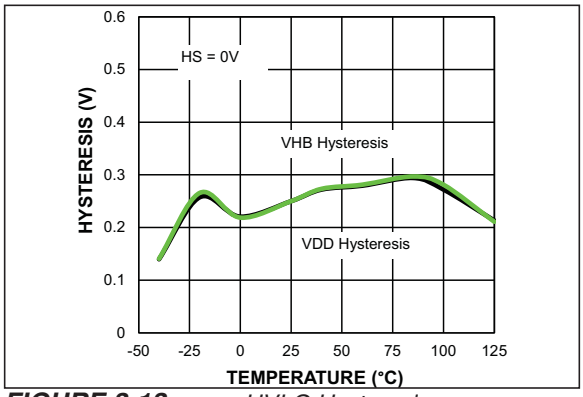


FIGURE 3-13: *UVLO Hysteresis vs. Temperature.*

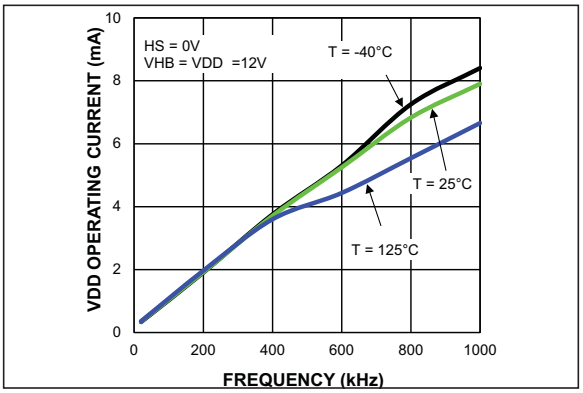


FIGURE 3-16: *V_{DD} Operating Current vs. Frequency.*

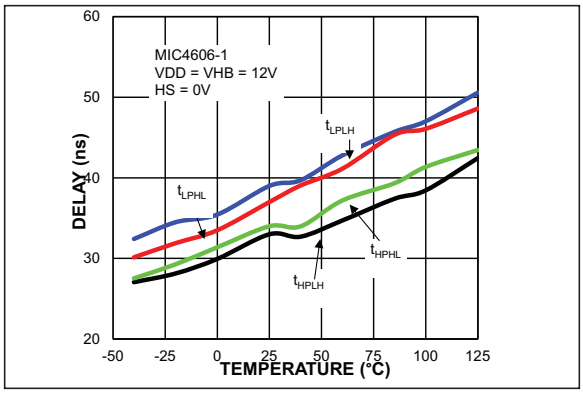


FIGURE 3-14: *Propagation Delay vs. Temperature.*

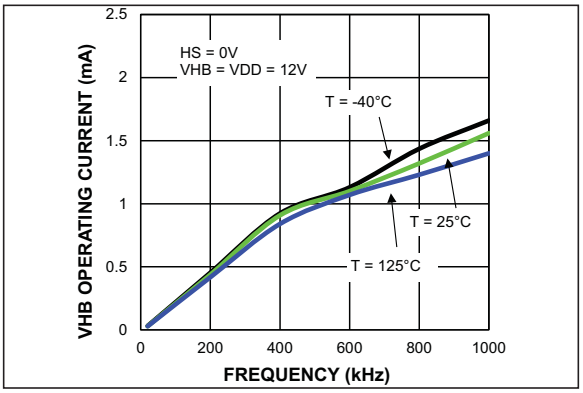


FIGURE 3-17: *V_{HB} Operating Current vs. Frequency.*

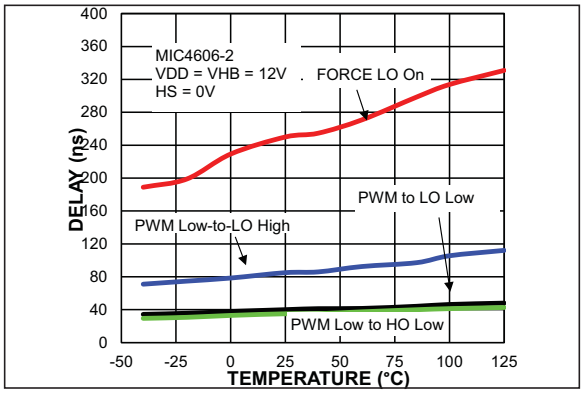


FIGURE 3-15: *Propagation Delay (PWM) vs. Temperature.*

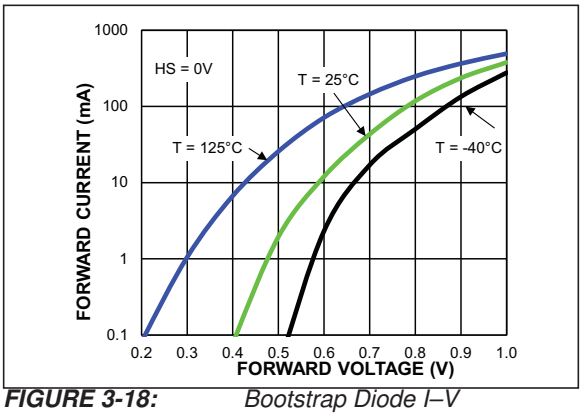


FIGURE 3-18: *Bootstrap Diode I–V Characteristics.*

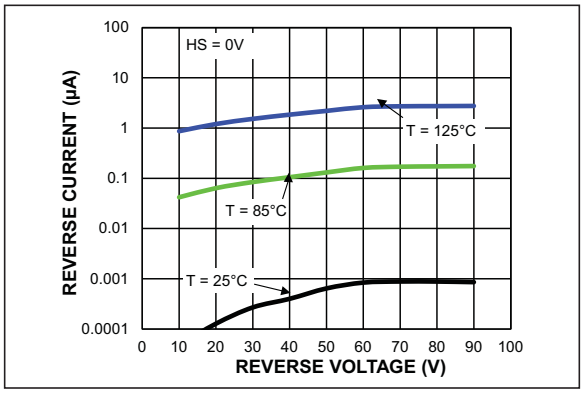


FIGURE 3-19: *Bootstrap Diode Reverse Current.*

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1through .

TABLE 4-1: MIC4606-1 QFN PIN FUNCTION TABLE

Pin Number	MIC4606-1 4x4 QFN	Description
1	NC	No Connect.
2	AHB	Phase A high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. An on-chip bootstrap diode is connected from VDD to AHB.
3	AHO	Phase A high-side drive output. Connect to the external high-side power MOSFET gate.
4	AHS	Phase A high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and AHB.
5	ALO	Phase A low-side drive output. Connect to the external low-side power MOSFET gate.
6	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >1.0 µF capacitor.
7	VSS	Driver reference supply input. Connect to the power ground of the external circuitry.
8	BLO	Phase B low-side drive output. Connect to the external low-side power MOSFET gate.
9	BHS	Phase B high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and BHB.
10	BHO	Phase B high-side drive output. Connect to the external high-side power MOSFET gate.
11	BHB	Phase B high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. An on-chip bootstrap diode is connected from VDD to BHB.
12	EN	Enable input. A logic high on the enable pin results in normal operation. A logic low disables all outputs and places the driver into a low current shutdown mode. Do not leave this pin floating.
13	BHI	Phase B high-side drive input.
14	BLI	Phase B low-side drive input.
15	ALI	Phase A low-side drive input.
16	AHI	Phase A high-side drive input.
EP	ePad	Exposed thermal pad. Connect to VSS. A connection to the ground plane is necessary for optimum thermal performance.

TABLE 4-2: MIC4606-2 QFN PIN FUNCTION TABLE

Pin Number	MIC4606-2 4x4 QFN	Description
1	NC	No Connect.
2	AHB	Phase A high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. An on-chip bootstrap diode is connected from V_{DD} to AHB.
3	AHO	Phase A high-side drive output. Connect to the external high-side power MOSFET gate.
4	AHS	Phase A high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and AHB.
5	ALO	Phase A low-side drive output. Connect to the external low-side power MOSFET gate.
6	VDD	Input supply for gate drivers. Decouple this pin to V_{SS} with a >1.0 µF capacitor.
7	VSS	Driver reference supply input. Connect to the power ground of the external circuitry.
8	BLO	Phase B low-side drive output. Connect to the external low-side power MOSFET gate.
9	BHS	Phase B high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and BHB.
10	BHO	Phase B high-side drive output. Connect to the external high-side power MOSFET gate.
11	BHB	Phase B high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. An on-chip bootstrap diode is connected from V_{DD} to BHB.
12	EN	Enable input. A logic high on the enable pin results in normal operation. A logic low disables all outputs and places the driver into a low current shutdown mode. Do not leave this pin floating.
13	BPWM	Phase B PWM input for single input signal drive.
14	NC	No connect.
15	NC	No connect.
16	APWM	Phase A PWM input for single input signal drive.
EP	ePad	Exposed thermal pad. Connect to V_{SS}. A connection to the ground plane is necessary for optimum thermal performance.

TABLE 4-3: MIC4606-1 TSSOP PIN FUNCTION TABLE

Pin Number	MIC4606-1 4x4 TSSOP	Description
1	BHB	Phase B high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. An on-chip bootstrap diode is connected from V_{DD} to BHB.
2	EN	Enable input. A logic high on the enable pin results in normal operation. A logic low disables all outputs and places the driver into a low current shutdown mode. Do not leave this pin floating.
3	BHI	Phase B high-side drive input.
4	BLI	Phase B low-side drive input.
5	ALI	Phase A low-side drive input.
6	AHI	Phase A high-side drive input.
7	NC	No Connect.
8	AHB	Phase A high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. An on-chip bootstrap diode is connected from V_{DD} to AHB.
9	AHO	Phase A high-side drive output. Connect to the external high-side power MOSFET gate.
10	AHS	Phase A high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and AHB.
11	ALO	Phase A low-side drive output. Connect to the external low-side power MOSFET gate.
12	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >1.0 µF capacitor.
13	VSS	Driver reference supply input. Connect to the power ground of the external circuitry.
14	BLO	Phase B low-side drive output. Connect to the external low-side power MOSFET gate.
15	BHS	Phase B high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and BHB.
16	BHO	Phase B high-side drive output. Connect to the external high-side power MOSFET gate.

TABLE 4-4: MIC4606-2 TSSOP PIN FUNCTION TABLE

Pin Number	MIC4606-2 4x4 TSSOP	Description
1	BHB	Phase B high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. An on-chip bootstrap diode is connected from V_{DD} to BHB.
2	EN	Enable input. A logic high on the enable pin results in normal operation. A logic low disables all outputs and places the driver into a low current shutdown mode. Do not leave this pin floating.
3	BPWM	Phase B PWM input for single input signal drive.
4	NC	No connect.
5	NC	No connect.
6	APWM	Phase A PWM input for single input signal drive.
7	NC	No Connect.
8	AHB	Phase A high-side bootstrap supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. An on-chip bootstrap diode is connected from V_{DD} to AHB.
9	AHO	Phase A high-side drive output. Connect to the external high-side power MOSFET gate.
10	AHS	Phase A high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and AHB.
11	ALO	Phase A low-side drive output. Connect to the external low-side power MOSFET gate.
12	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >1.0 µF capacitor.
13	VSS	Driver reference supply input. Connect to the power ground of the external circuitry.
14	BLO	Phase B low-side drive output. Connect to the external low-side power MOSFET gate.
15	BHS	Phase B high-side drive reference connection. Connect to the external high-side power MOSFET source terminal. Connect a bootstrap capacitor between this pin and BHB.
16	BHO	Phase B high-side drive output. Connect to the external high-side power MOSFET gate.

5.0 FUNCTIONAL DIAGRAM

For xHO to be high, the xHI must be high and the xLO must be low. xHO going high is delayed by xLO falling below 1.9V. The xHI and xLI inputs must not rise at the same time to prevent a glitch from occurring on the output. A minimum 50 ns delay between both inputs is recommended.

xLO is turned off very quickly on the xLI falling edge. xLO going high is delayed by the longer of 35 ns delay of xHO control signal going “off” or the RS latch being set.

The latch is set by the quicker of either the falling edge of xHS or xLI gated delay of 250 ns. The latch is present to lockout xLO bounce due to ringing on xHS. If xHS never adequately falls due to the absence of or the presence of a very weak external pull-down on xHS, the gated delay of 250 ns at xLI will set the latch allowing xLO to transition high. This in turn allows the xLI startup pulse to charge the bootstrap capacitor if the load inductor current is very low and xHS is uncontrolled. The latch is reset by the xLI falling edge.

There is one external enable pin that controls both phases.

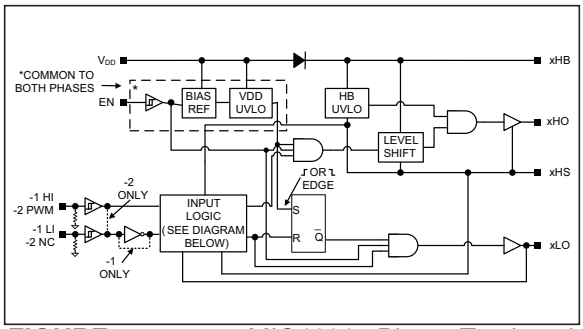


FIGURE 5-1: *MIC4606 xPhase Top Level Block Diagram.*

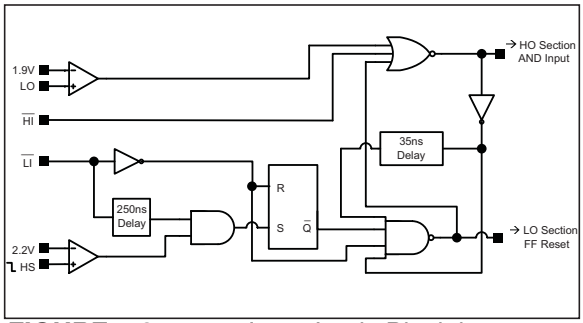


FIGURE 5-2: *Input Logic Block in Figure 5-1.*

6.0 FUNCTIONAL DESCRIPTION

The MIC4606 is a non-inverting, 85V full-bridge MOSFET driver designed to independently drive all four N-Channel MOSFETs in the bridge. The MIC4606 offers a wide 5.5V to 16V operating supply range with either four independent TTL inputs (MIC4606-1) or two PWM inputs, one for each phase (MIC4606-2). Refer to Figure 5-1.

The drivers contain input buffers with hysteresis, three independent UVLO circuits (two high side and one low side), and four output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to its HS pin. Each phase has an internal diode that is used by the bootstrap circuits to provide the drive voltages for each of the two high-side outputs.

6.1 Startup and UVLO

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the V_{DD} and V_{SS} pins. The high-side UVLO circuits monitor the voltage between the xHB and xHS pins. Hysteresis in the UVLO circuits prevent noise and finite circuit impedance from causing chatter during turn-on.

6.2 Enable Inputs

There is one external enable pin that controls both phases. A logic high on the enable pin (EN) allows for startup of both phases and normal operation. Conversely, when a logic low is applied on the enable pin, both phases turn-off and the device enters a low current shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. Do not leave the EN pin floating.

6.3 Input Stage

All input pins (xLI and xHI) are referenced to the V_{SS} pin. The MIC4606 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the V_{DD} supply voltage and there is no dependence between IV_{DD} and the input signal amplitude. This feature makes the MIC4606 an excellent level translator that will drive high level gate threshold MOSFETs from a low-voltage PWM IC.

6.4 Low-Side Driver

A block diagram of the low-side driver is shown in Figure 6-1. It drives a ground (V_{SS} pin) referenced N-channel MOSFET.

Low impedances in the driver allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures high noise immunity and a low $R_{DS(ON)}$ from the external MOSFET.

A high level applied to xLI pin causes V_{DD} to be applied to the gate of the external MOSFET. A low level on the xLI pin grounds the gate of the external MOSFET.

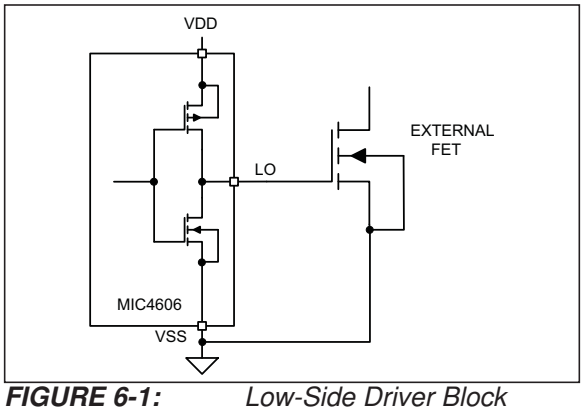


FIGURE 6-1: *Low-Side Driver Block Diagram.*

6.5 High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 6-2. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

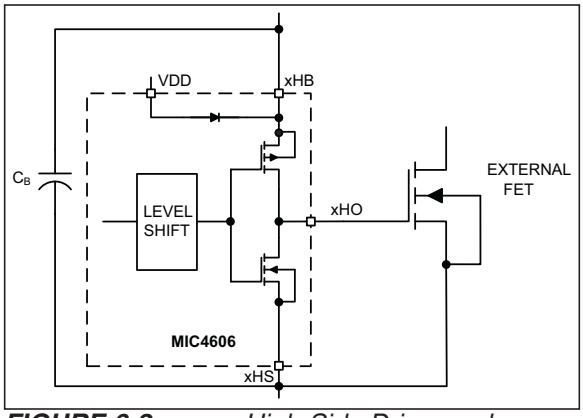


FIGURE 6-2: *High-Side Driver and Bootstrap Circuit Block Diagram.*

A low-power, high-speed, level-shifting circuit isolates the low side (V_{SS} pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 6-3 (only Phase A illustrated), the AHS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor C_B to charge up to V_{DD}-V_F during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is

applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor CB from discharging.

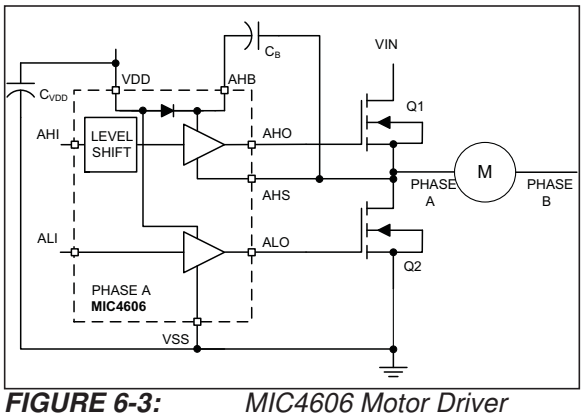


FIGURE 6-3: *MIC4606 Motor Driver Example.*

6.6 Programmable Gate Drive

The MIC4606 offers programmable gate drive, which means the MOSFET gate drive (gate to source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in driving the MOSFETs. Different MOSFETs require different V_{GS} characteristics for optimum RDSON performance. Typically, the higher the gate voltage (up to 16V), the lower the R_{DSON} achieved. For example, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but R_{DSON} is 5.2 mΩ. If driven to 10V, R_{DSON} is 4.1 mΩ – a decrease of 20%. In low-current applications, the losses due to R_{DSON} are minimal, but in battery-powered high-current motor drive applications such as power tools, the difference in R_{DSON} can cut into the efficiency budget, reducing run time.

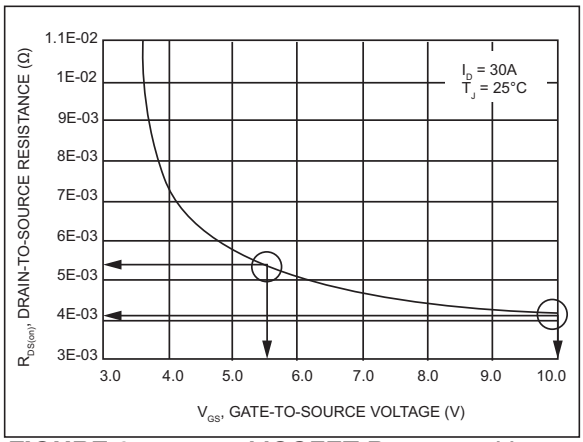


FIGURE 6-4: *MOSFET R_{DSON} vs. V_{GS}.*

7.0 APPLICATION INFORMATION

7.1 Adaptive Dead Time

The door lock/unlock circuit diagram shown in Figure 7-2 is used to illustrate the importance of the adaptive dead time feature of the MIC4606. For each phase, it is important that both MOSFETs are not conducting at the same time or V_{IN} will be shorted to ground and current will “shoot through” the MOSFETs. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing. The high switching current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive dead time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 7-1 shows an equivalent circuit of the high-side gate drive, including parasitic.

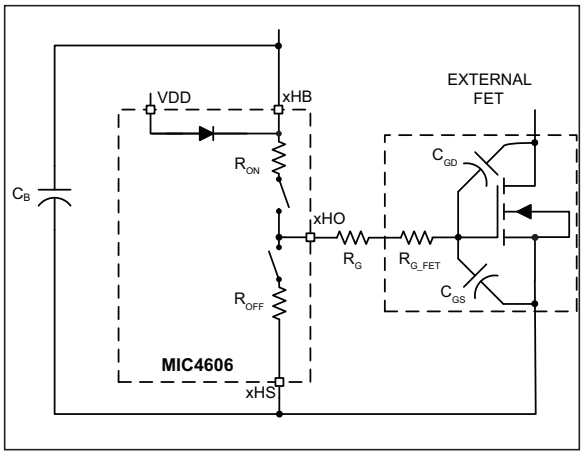


FIGURE 7-1: *MIC4606 Driving an External MOSFET.*

The internal gate resistance (RG_FET) and any external damping resistor (RG) isolate the MOSFET’s gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET datasheet. This delay increases when an external damping resistor is used.

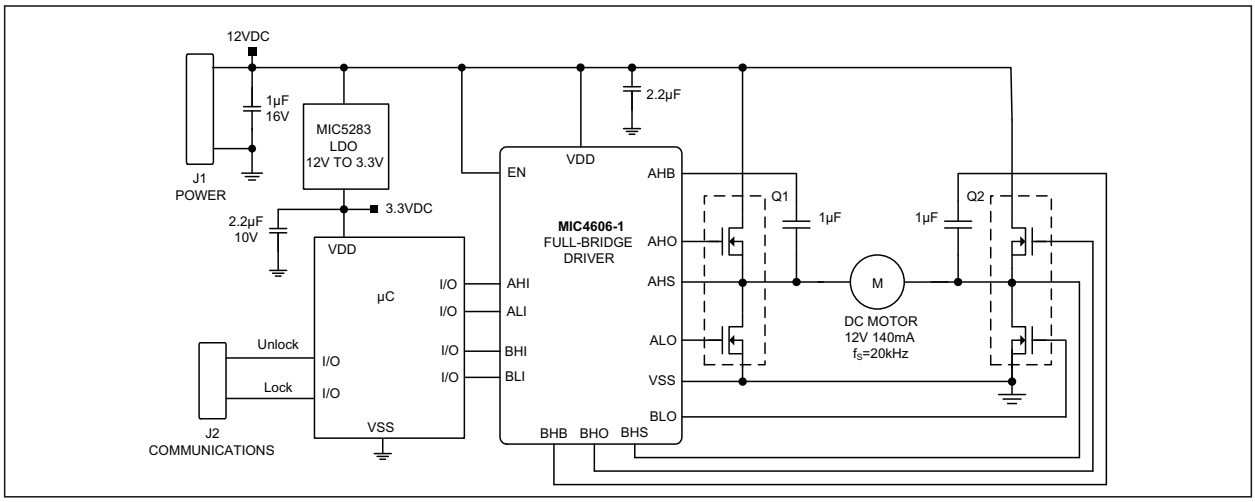


FIGURE 7-2: *Door Lock/Unlock Circuit.*

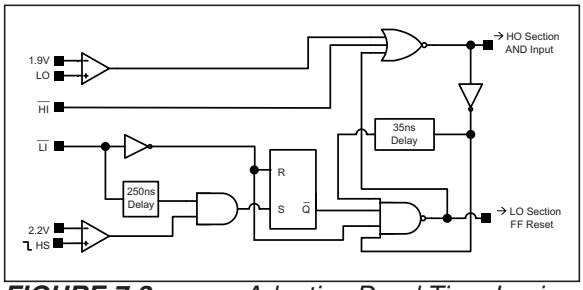


FIGURE 7-3: *Adaptive Dead Time Logic Diagram.*

The MIC4606 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time. Figure 7-3 illustrates how the adaptive dead time circuitry works.

For the MIC4606-2, a high level on the xPWM pin causes /HI to go high and /LI to go low. This causes the xLO pin to go low. The MIC4606 monitors the xLO pin voltage and prevents the xHO pin from turning on until the voltage on the xLO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4606 drives the xHO pin high. Monitoring the xLO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the xLO pin voltage settle out. An external resistor between the xLO output and the MOSFET may affect the performance of the xLO pin monitoring circuit and is not recommended.

A low on the xPWM pin causes /HI to go low and /LI to go high. This causes the xHO pin to go low after a short delay (t_{HOOFF}). Before the xLO pin can go high, the voltage on the switching node (xHS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the xHO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), insuring proper operation.

The internal logic circuits also insure a “first on” priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, the xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead time circuit in the MIC4606 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti shoot-through circuit’s control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 7-4 shows the dead time (<20 ns) between the high and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

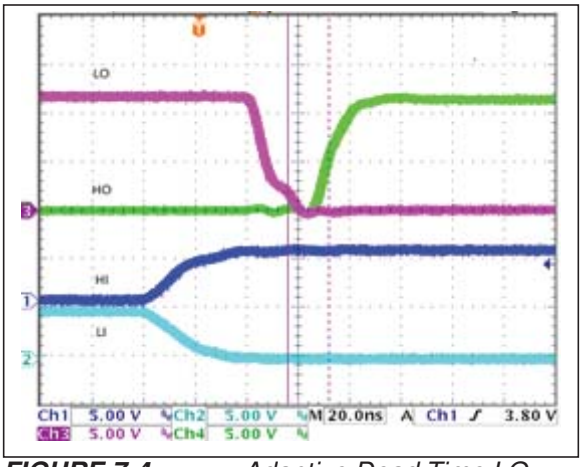


FIGURE 7-4: *Adaptive Dead Time LO (low) to HO (high).*

Table 7-1 contains truth tables for the MIC4606-1 (Independent TTL inputs) and Table 7-2 is for the MIC4606-2 (PWM inputs) that details the “first on” priority as well as the failsafe delay (t_{SWTO}).

TABLE 7-1: MIC4606-1 TRUTH TABLE

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go high until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes low.

TABLE 7-2: MIC4606-2 TRUTH TABLE

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	0	1	xHO will not go high until xLO falls below 1.9V.

7.2 HS Pin Clamp

A resistor/diode clamp between the motor phase node and the xHS pin is necessary to clamp large negative glitches or pulses on the xHS pin.

Figure 7-5 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the xHS pins are rated for negative voltage, it is good practice to clamp the negative voltage on the xHS pin with a resistor and diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the xHS pin voltage exceeds 0.7V, a diode between the xHS pin and ground is recommended. The diode reverse voltage rating must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

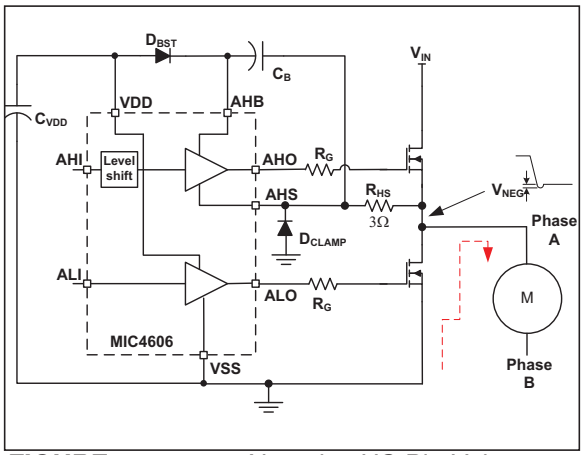


FIGURE 7-5: *Negative HS Pin Voltage.*

7.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

7.4 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

EQUATION 7-1:

$$I_{F(AVE)} = Q_{gate} \times f_S$$

where:

Q_{gate} = total gate charge at V_{HB} - V_{HS}

f_s = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 7-2:

$$Pdiode_{fwd} = I_{F(AVE)} \times V_F$$

where:

V_F = diode forward voltage drop

There are two phases in the MIC4606. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3 µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode (Figure 7-6). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

EQUATION 7-3:

$$Pdiode_{REV} = I_R \times V_{REV} \times (1 - D)$$

Where:

I_R	=	reverse current flow at V_{REV} and T_J
V_{REV}	=	diode reverse voltage
D	=	duty cycle = $t_{ON} \times f_S$

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

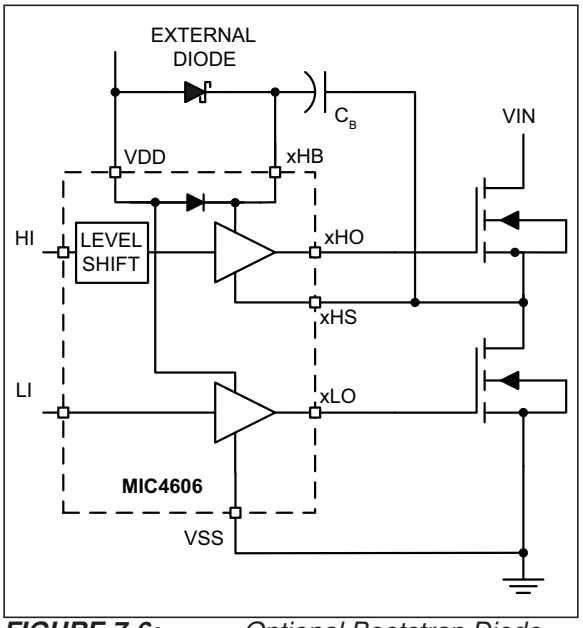


FIGURE 7-6: *Optional Bootstrap Diode.*

7.5 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 7-7 shows a simplified equivalent circuit of the MIC4606 driving an external high-side MOSFET.

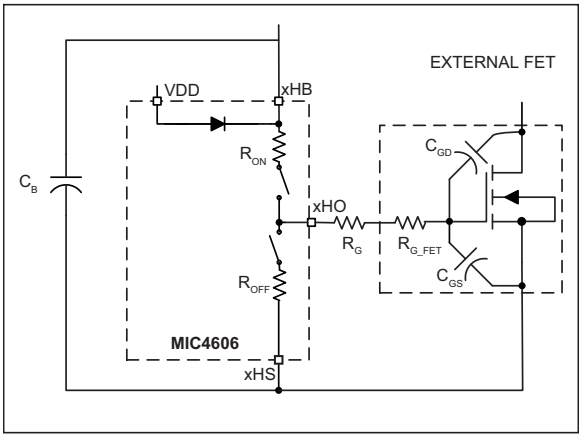


FIGURE 7-7: *MIC4606 Driving an External High-Side MOSFET.*

7.6 Dissipation during the External MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4606. R_G is the series resistor (if any) between the driver and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus V_{GS}. Figure 7-8 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

EQUATION 7-4:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2}$$

but

EQUATION 7-5:

$$Q = C \times V$$

so

EQUATION 7-6:

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where

C_{ISS}	=	total gate capacitance of the MOSFET

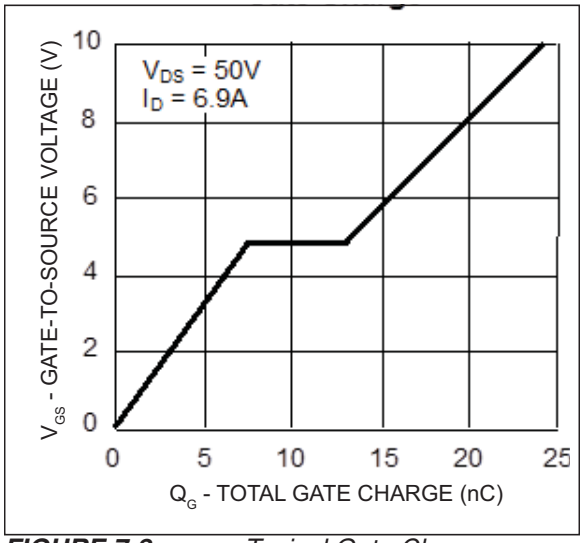


FIGURE 7-8: *Typical Gate Charge vs. V_{GS}.*

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

EQUATION 7-7:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

EQUATION 7-8:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

E_{DRIVER}	=	energy dissipated per switching cycle
P_{DRIVER}	=	power dissipated per switching cycle
Q_G	=	total gate charge at V_{GS}
V_{GS}	=	gate to source voltage on the MOSFET
f_S	=	switching frequency of the gate drive circuit

The power dissipated in the driver equals the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting $R_{ON} = R_{OFF}$, the power dissipated in the driver due to driving the external MOSFET is:

EQUATION 7-9:

$$Pdiss_{driver} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$