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MIC4607

85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection

Features

- Gate Drive Supply Voltage Up To 16V
- Overcurrent Protection
- Drives High-Side And Low-Side N-Channel MOSFETs With Independent Inputs Or With A Single PWM Signal
- TTL Input Thresholds
- On-Chip Bootstrap Diodes
- Fast 35 ns Propagation Times
- Shoot-Through Protection
- Drives 1000 pF Load With 20 ns Rise And Fall Times
- Low Power Consumption
- Supply Undervoltage Protection
- –40°C to +125°C Junction Temperature Range

Applications

- Three-Phase and BLDC Motor Drives
- Three-Phase Inverters

General Description

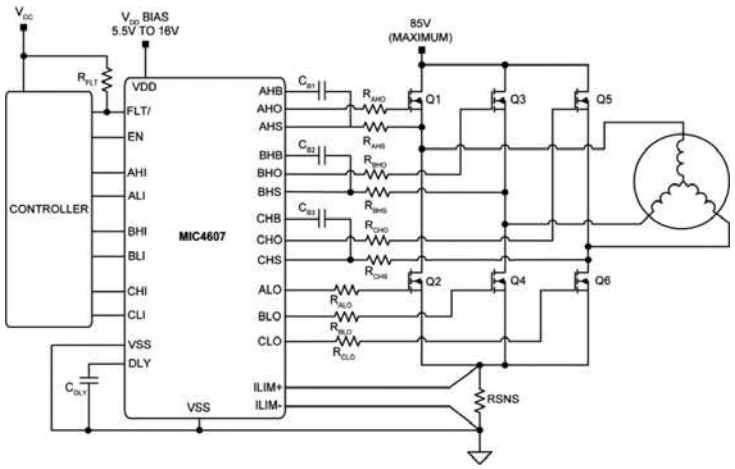
The MIC4607 is an 85V, three-phase MOSFET driver. The MIC4607 features a fast (35 ns) propagation delay time and a 20 ns driver rise/fall time for a 1 nF capacitive load. TTL inputs can be separate high- and low-side signals or a single PWM input with high and low drive generated internally. High- and low-side outputs are guaranteed to not overlap in either mode. The MIC4607 includes overcurrent protection as well as a high-voltage internal diode that charges the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4607 ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

The MIC4607 is available in a both a 28-pin 4 mm × 5 mm QFN and 28-pin TSSOP package with an operating junction temperature range of –40°C to +125°C.

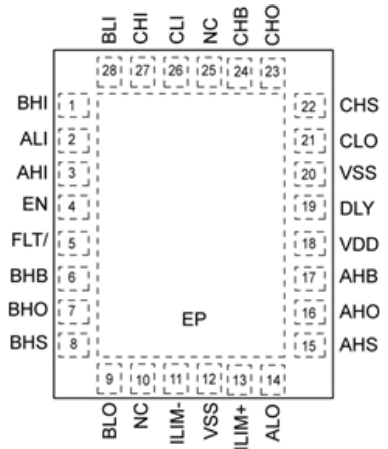
Typical Application Circuit

MIC4607
Three-Phase Motor Driver

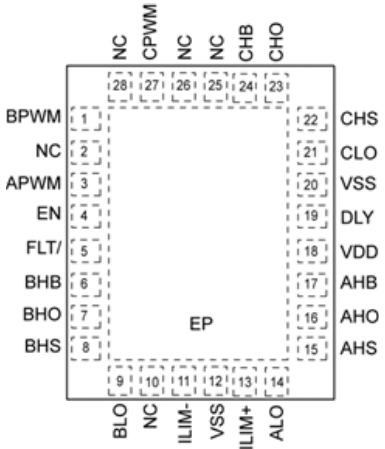


Package Type

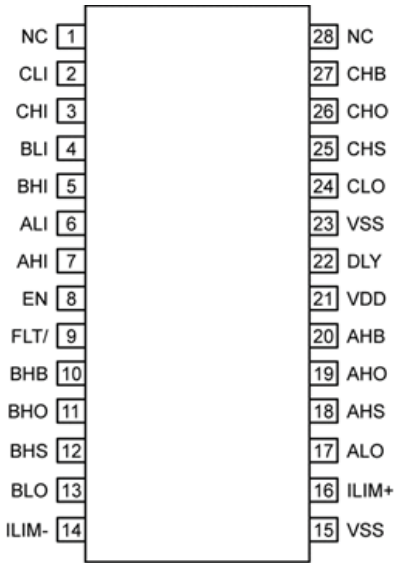
MIC4607-1
28-pin QFN



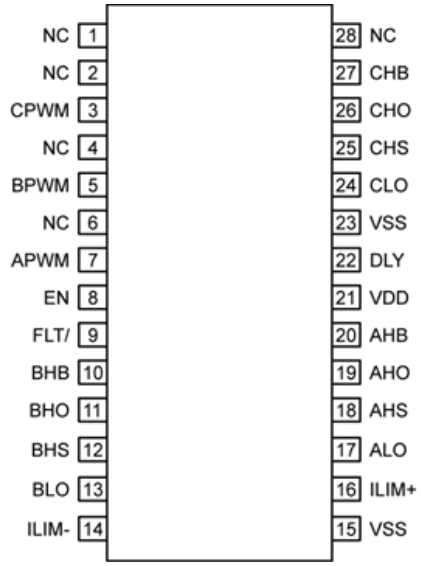
MIC4607-2
28-pin QFN



MIC4607-1
28-pin TSSOP

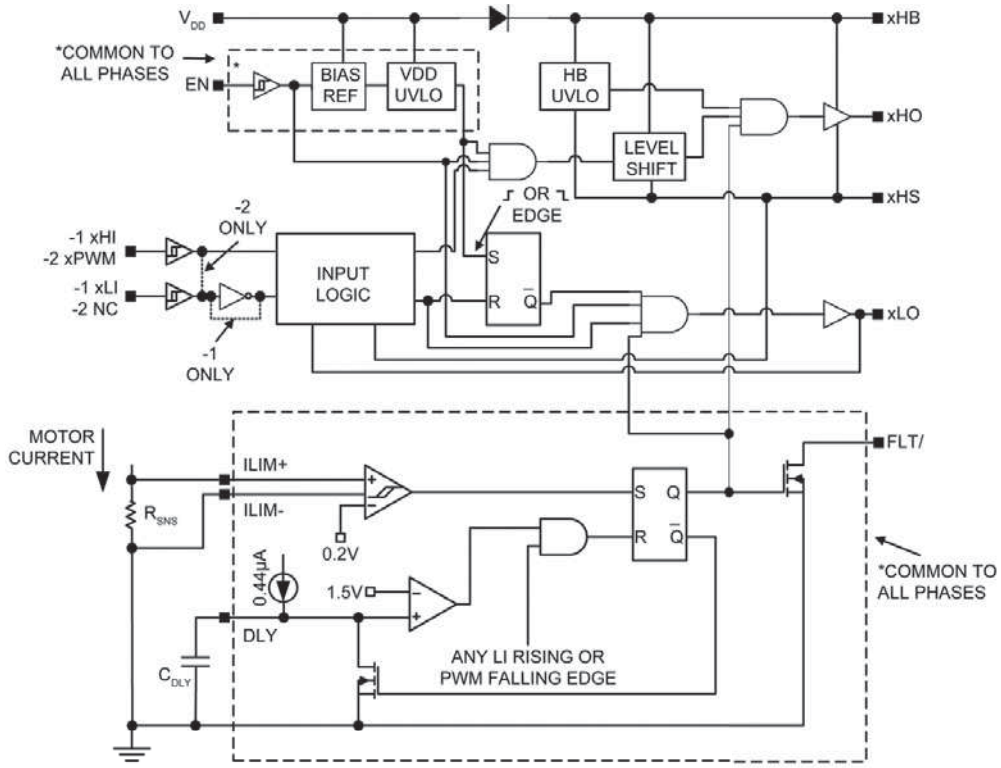


MIC4607-2
28-pin TSSOP



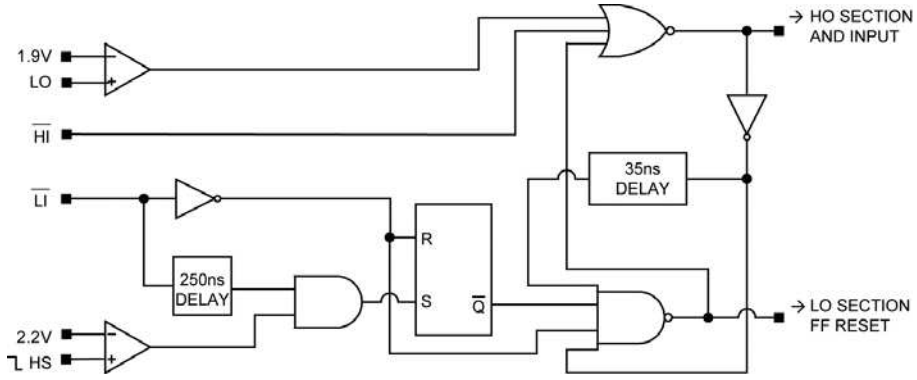
Functional Diagram

MIC4607 xPhase Top-Level Functional Diagram



NOTE:
x = A, B, OR C
-1 = MIC4607-1
-2 = MIC4607-2

Input Logic Block



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †, (Note 2)

Supply Voltage (V_{DD}, $V_{xHB} – V_{xHS}$) ..... –0.3V to 18V
Input Voltages (V_{xLI}, V_{xHI}, V_{xPWM}, V_{EN}) ..... –0.3V to V_{DD} + 0.3V
FLT/ Pin ..... –0.3V to V_{DD} + 0.3V
DLY Pin ..... –0.3V to 18V
Voltage on xLO (V_{xLO}) ..... –0.3V to V_{DD} + 0.3V
Voltage on xHO (V_{xHO}) ..... V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on xHS (Continuous) ..... –1V to 90V
Voltage on xHB 108V
ILIM+ ..... –0.3V to +5V
ILIM– ..... –0.3V to +2V
Average Current in V_{DD} to HB Diode ..... 100 mA
ESD Protection On All Pins (Note 1):
HBM ..... 1 kV
MM 200V
CDM 200V

Operational Characteristics ††, (Note 2)

Supply Voltage (V_{DD}), [decreasing V_{DD}] ..... 5.25V to 16V
Supply Voltage (V_{DD}), [increasing V_{DD}] ..... 5.5V to 16V
Voltage on xHS ..... –1V to 85V
Voltage on xHS (repetitive transient <100 ns) ..... –5V to 90V
HS Slew Rate ..... 50 V/ns
Voltage on xHB ..... V_{HS} + 5.5V to V_{HS} + 16V
and/or ..... V_{DD} –1V to V_{DD} +85V

† Notice: Exceeding the absolute maximum ratings may damage the device.
†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.
2: An “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

DC CHARACTERISTICS (Note 1, 2)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate –40°C< T_J < +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current						
V_{DD} Quiescent Current	I_{DD}	—	390	**750**	µA	xLI = xHI = 0V
V_{DD} Shutdown Current	I_{DDSH}	—	2.2	**10**	µA	xLI = xHI = 0V; EN = 0V with HS = floating
		—	58	**150**		xLI = xHI = 0V ; EN = 0V; HS = 0V
V_{DD} Operating Current	I_{DDO}	—	0.6	**1.5**	mA	f = 20 kHz
Per Channel xHB Quiescent Current	I_{HB}	—	20	**75**	µA	xLI = xHI = 0V or xLI = 0V and xHI = 5V
Per Channel xHB Operating Current	I_{HBO}	—	30	**400**	µA	f = 20 kHz
xHB to V_{SS} Current, Quiescent	I_{HBS}	—	0.05	5	µA	V_{xHS} = V_{xHB} = 90V
xHB to V_{SS} Current, Operating	I_{HBSO}	—	30	**300**	µA	f = 20 kHz
Input (TTL: xLI, xHI, xPWM, EN) (Note 3)						
Low-Level Input Voltage	V_{IL}	—	—	**0.8**	V	—
High-Level Input Voltage	V_{IH}	**2.2**	—	—	V	—
Input Voltage Hysteresis	V_{HYS}		0.1	—	V	—
Input Pull-Down Resistance	R_I	**100**	300	**500**	kΩ	xLI and xHI Inputs (-1 Version)
		50	130	**250**		xPWM Input (-2 Version)
Undervoltage Protection						
V_{DD} Falling Threshold	V_{DDR}	**3.8**	4.4	**4.9**	V	—
V_{DD} Threshold Hysteresis	V_{DDH}	—	0.25	—	V	—
xHB Falling Threshold	V_{HBR}	**4.0**	4.4	**4.9**	V	—
xHB Threshold Hysteresis	V_{HBH}	—	0.25	—	V	—
Overcurrent Protection						
Rising Overcurrent Threshold	V_{ILIM+}	175	200	225	mV	(V_{ILIM+} – $V_{ILIM–}$)
ILIM to Gate Propagation Delay	t_{ILIM_PROP}	—	70	—	ns	V_{ILIM+} = 0.5V peak
Fault Circuit						
FLT/ Output Low Voltage	V_{OLF}	—	0.2	0.5	V	V_{ILIM} = 1V; $I_{FLT/}$ = 1 mA
Rising DLY Threshold	V_{DLY+}	—	1.5	—	V	—
DLY Current Source	I_{DLY}	0.3	0.44	0.6	µA	V_{DLY} = 0V
Fault Clear Time	t_{FCL}	—	670	—	µs	C_{DLY} = 1 nF
Bootstrap Diode						
Low-Current Forward Voltage	V_{DL}	—	0.4	**0.70**	V	$I_{VDD-xHB}$ = 100 µA
High-Current Forward Voltage	V_{DH}	—	0.8	**1**	V	$I_{VDD-xHB}$ = 50 mA

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate –40°C< T_J < +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dynamic Resistance	R_D	—	4	**6**	V	—
xLO Gate Driver						
Low-Level Output Voltage	V_{OLL}	—	0.3	**0.6**	V	I_{xLO} = 50 mA
High-Level Output Voltage	V_{OHL}	—	0.5	**1**	V	I_{xLO} = –50 mA, $V_{OHL} = V_{DD} – V_{xLO}$
Peak Sink Current	I_{OHL}	—	1	—	A	V_{xLO} = 0V
Peak Source Current	I_{OLL}	—	1	—	A	V_{xLO} = 12V
xHO Gate Driver						
Low-Level Output Voltage	V_{OLH}	—	0.3	0.6	V	I_{xHO} = 50 mA
High-Level Output Voltage	V_{OHH}	—	0.5	1	V	I_{xHO} = –50 mA, $V_{OHH} = V_{xHB} – V_{xHO}$
Peak Sink Current	I_{OHH}	—	1	—	A	V_{xHO} = 0V
Peak Source Current	I_{OLH}	—	1	—	A	V_{xHO} = 12V
Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high).						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	—	35	**75**	ns	—
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	—	35	**75**	ns	—
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	—	35	**75**	ns	—
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	—	35	**75**	ns	—
Output Rise/Fall Time	$t_{R/F}$	—	20	—	ns	C_L = 1000 pF
Output Rise/Fall Time (3V to 9V)	$t_{R/F}$	—	0.8	—	µs	C_L = 0.1 µF
Minimum Input Pulse Width that Changes the Output	t_{PW}	—	50	—	ns	Note 4
Switching Specifications PWM Mode (MIC4607-2) or LI/HI mode (MIC4607-1) with Overlapping LI/HI Inputs						
Delay from PWM Going High / LI Low, to LO Going Low	t_{LOOFF}	—	35	**75**	ns	—
LO Output Voltage Threshold for LO FET to be Considered Off	V_{LOOFF}	—	1.9	—	V	—
Delay from LO Off to HO Going High	t_{HOON}	—	35	**75**	ns	—
Delay from PWM or HI Going Low to HO Going Low	t_{HOOFF}	—	35	**75**	ns	—

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate –40°C< T_J < +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switch Node Voltage Threshold Signaling HO is Off	V_{SWTH}	1	2.2	**4**	V	—
Delay between HO FET Being Considered Off to LO Turning On	t_{LOON}	—	35	**75**	ns	—
Forced xLO On if V_{SWTH} is Not Detected	t_{SWTO}	**100**	250	**500**	ns	—

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{IN} = V_{EN} = 12V, V_{BOOST} – V_{SW} = 3.3V, V_{OUT} = 3.3V

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Operating Ambient Temperature Range	T_A	–40	—	+125	°C	—
Lead Temperature	—	—	260	—	°C	Soldering, 10s
Storage Temperature Range	T_S	–60	—	+150	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, 4 mm × 5 mm QFN-28L	θ_{JA}	—	43	—	°C/W	—
Thermal Resistance, 4 mm × 5 mm QFN-28L	θ_{JC}	—	3.4	—	°C/W	—
TSSOP-28L	θ_{JA}	—	70	—	°C/W	—
TSSOP-28L	θ_{JC}	—	20	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

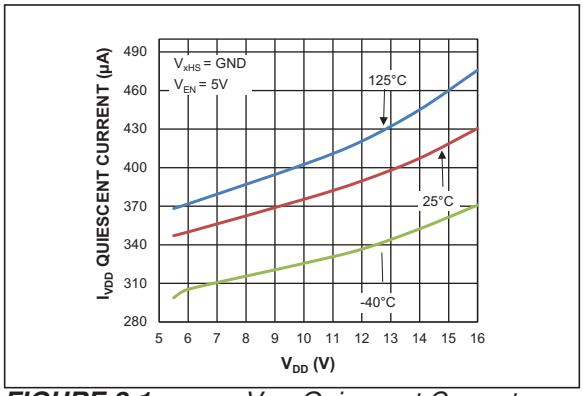


FIGURE 2-1: *V_{DD} Quiescent Current vs. V_{DD} Voltage.*

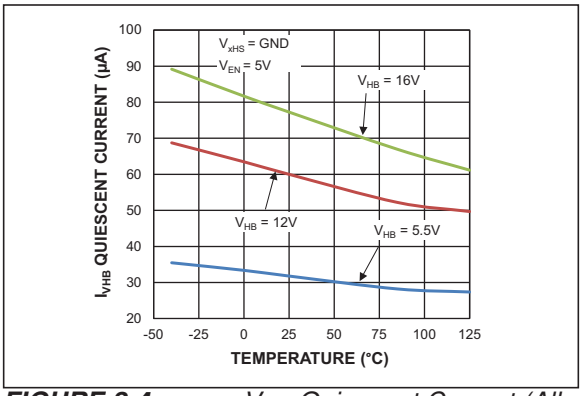


FIGURE 2-4: *V_{HB} Quiescent Current (All Channels) vs Temperature.*

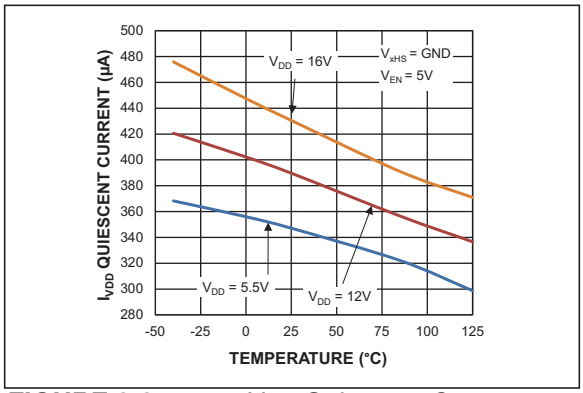


FIGURE 2-2: *V_{DD} Quiescent Current vs. Temperature.*

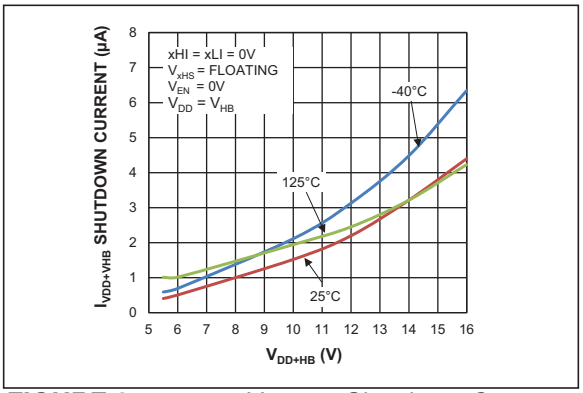


FIGURE 2-5: *V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Voltage.*

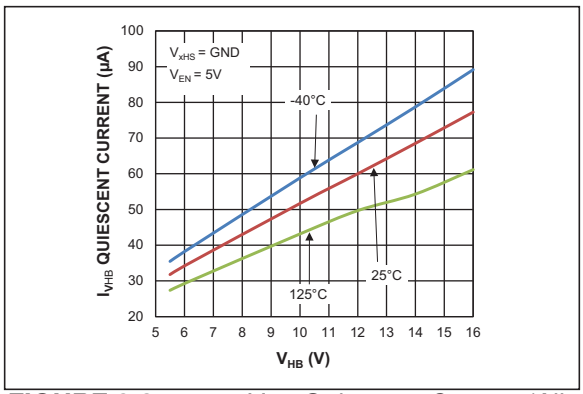


FIGURE 2-3: *V_{HB} Quiescent Current (All Channels) vs. V_{HB} Voltage.*

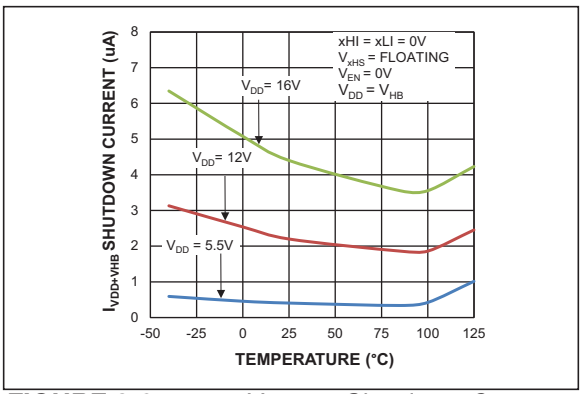


FIGURE 2-6: *V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Temperature.*

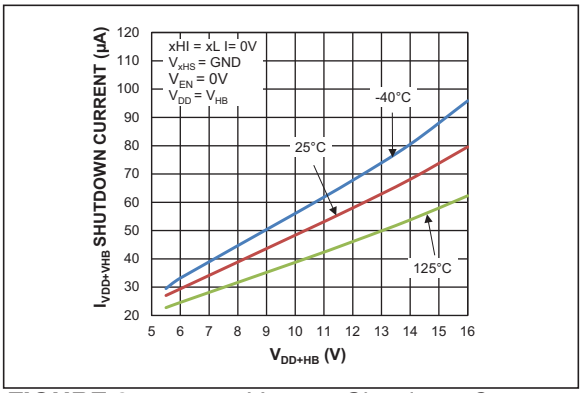


FIGURE 2-7: *V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Voltage.*

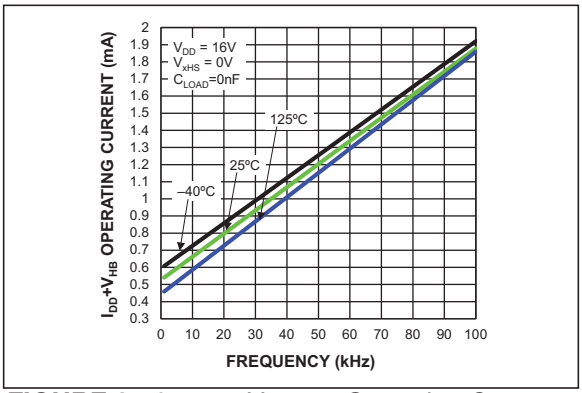


FIGURE 2-10: *V_{DD+HB} Operating Current vs. Switching Frequency.*

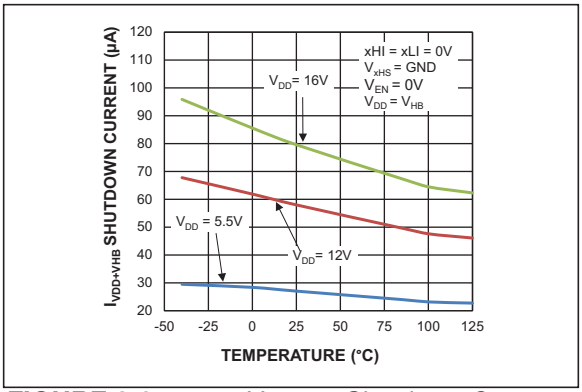


FIGURE 2-8: *V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Temperature.*

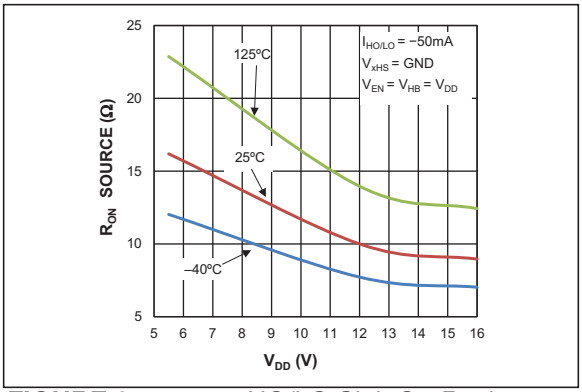


FIGURE 2-11: *HO/LO Sink On-Resistance vs. V_{DD}.*

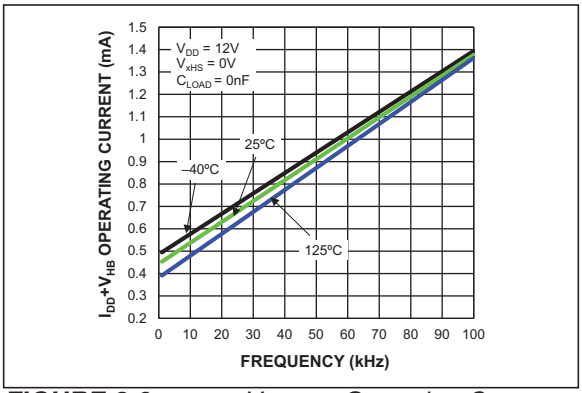


FIGURE 2-9: *V_{DD+HB} Operating Current vs. Switching Frequency.*

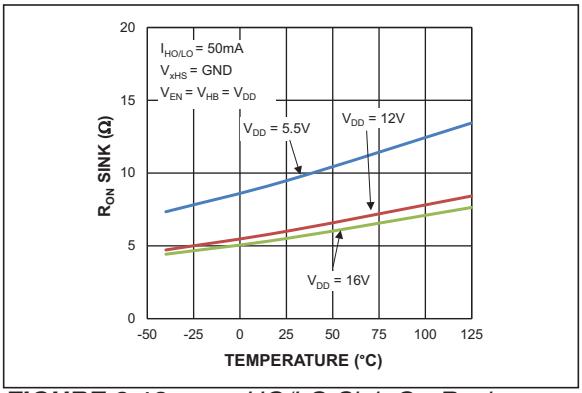


FIGURE 2-12: *HO/LO Sink On-Resistance vs. Temperature.*

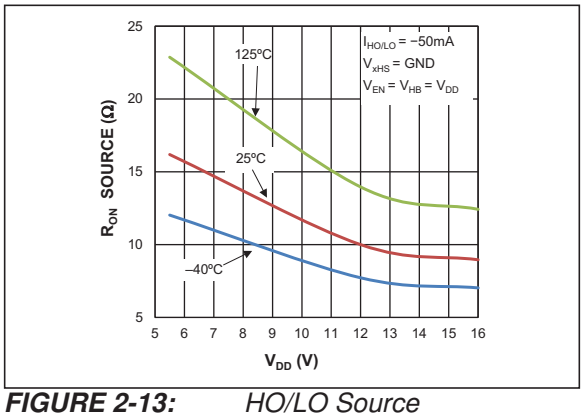


FIGURE 2-13: *HO/LO Source On-Resistance vs. V_{DD}.*

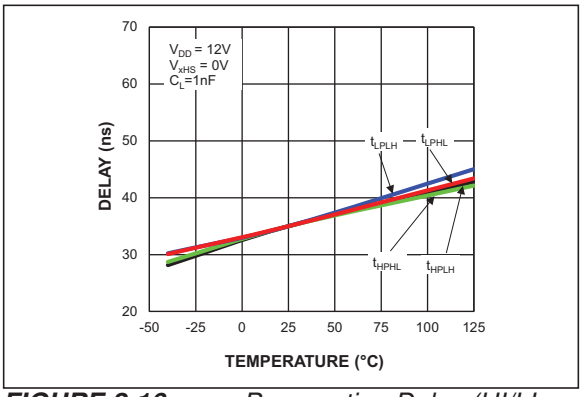


FIGURE 2-16: *Propagation Delay (HI/LI Input) vs. Temperature.*

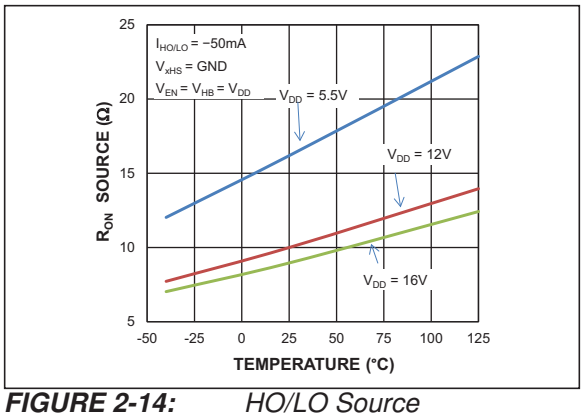


FIGURE 2-14: *HO/LO Source On-Resistance vs. Temperature.*

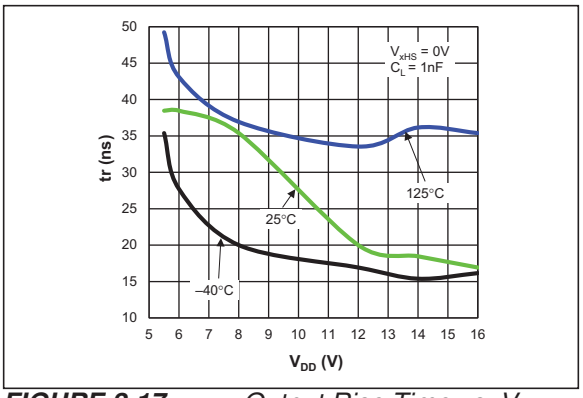


FIGURE 2-17: *Output Rise Time vs. V_{DD} Voltage.*

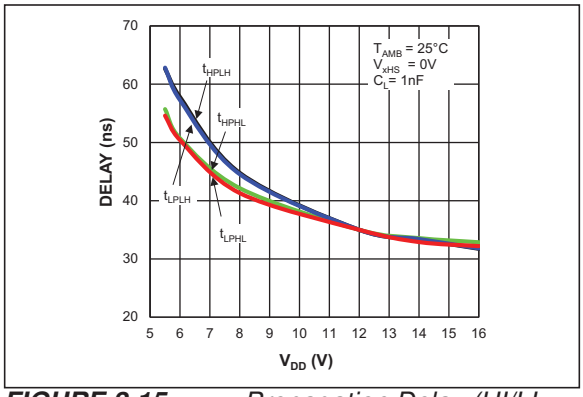


FIGURE 2-15: *Propagation Delay (HI/LI Input) vs. V_{DD} Voltage.*

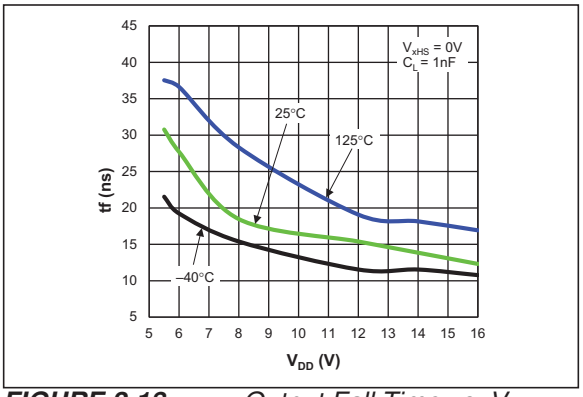


FIGURE 2-18: *Output Fall Time vs. V_{DD} Voltage.*

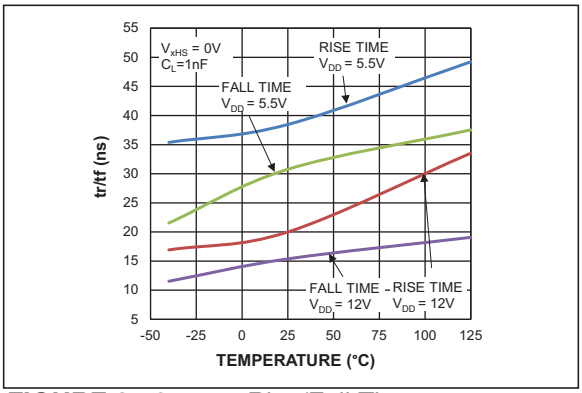


FIGURE 2-19: *Rise/Fall Time vs. Temperature.*

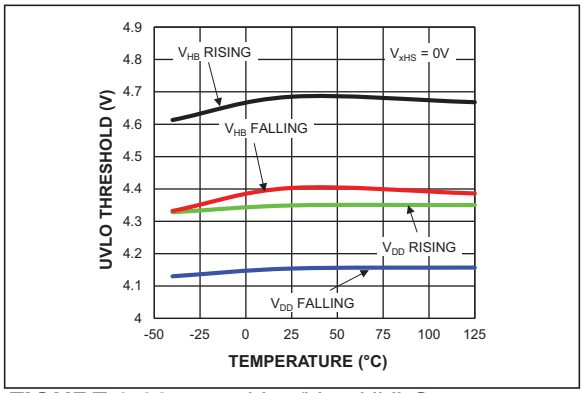


FIGURE 2-22: *V_{DD}/V_{HB} UVLO vs. Temperature.*

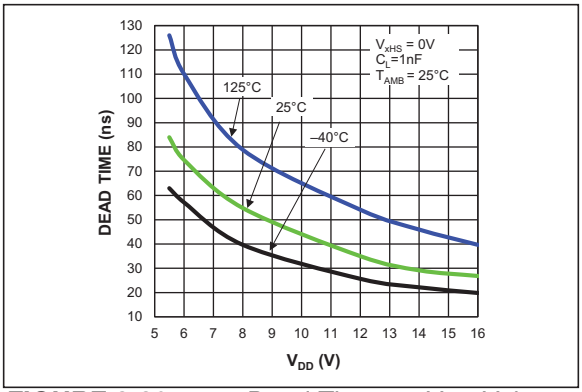


FIGURE 2-20: *Dead Time vs. V_{DD} Voltage.*

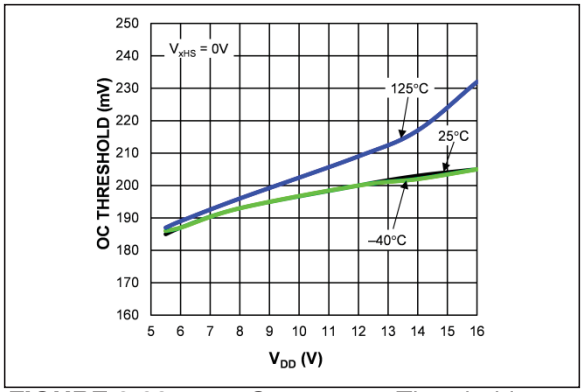


FIGURE 2-23: *Overcurrent Threshold vs. V_{DD} Voltage.*

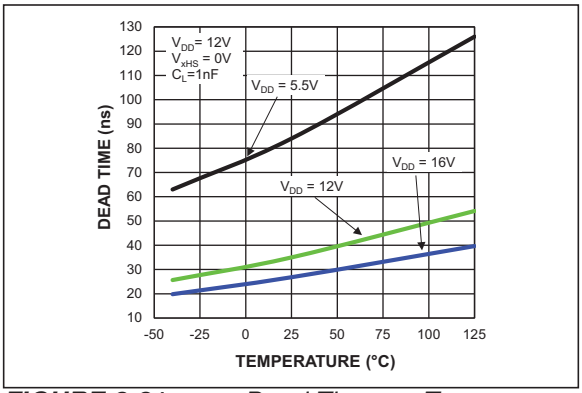


FIGURE 2-21: *Dead Time vs. Temperature.*

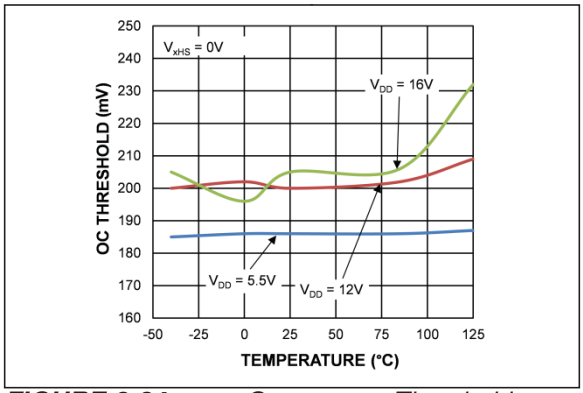


FIGURE 2-24: *Overcurrent Threshold vs. Temperature.*

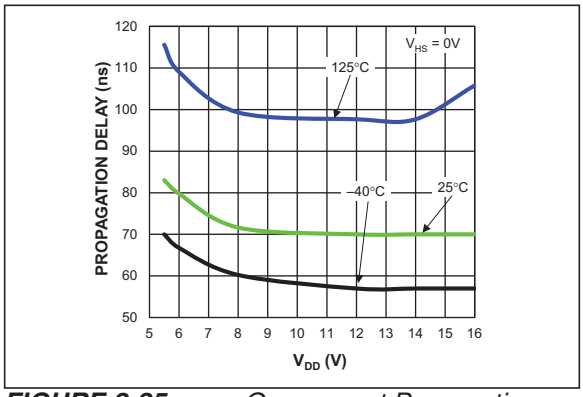


FIGURE 2-25: *Overcurrent Propagation Delay vs. V_{DD} Voltage.*

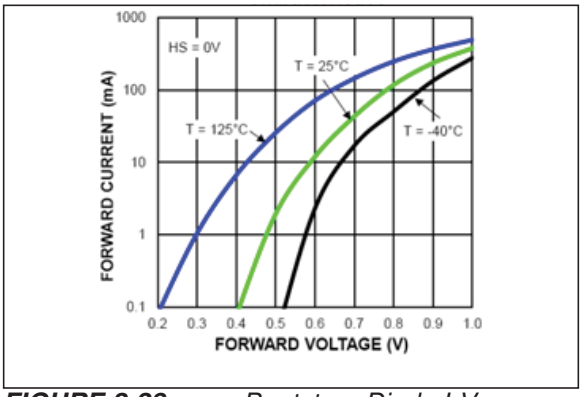


FIGURE 2-28: *Bootstrap Diode I-V Characteristics.*

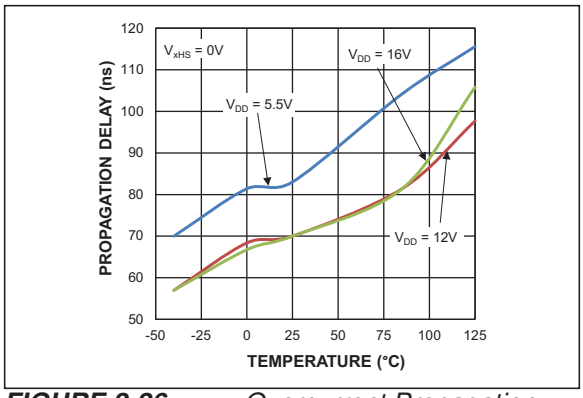


FIGURE 2-26: *Overcurrent Propagation Delay vs. Temperature.*

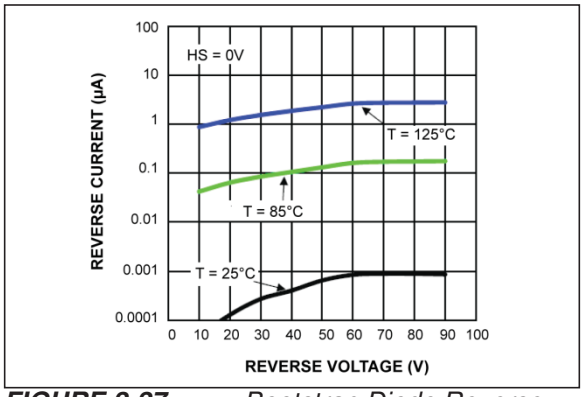


FIGURE 2-27: *Bootstrap Diode Reverse Current.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: QFN PIN FUNCTION TABLE

Pin Number QFN	Pin Name		Description
	MIC4607-1	MIC4607-2	
1	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
2	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
3	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
4	EN	EN	Active high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
5	FLT/	FLT/	Open Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
6	BHB	BHB	Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and B_{HS}. An on-board bootstrap diode is connected from V_{DD} to B_{HB}.
7	BHO	BHO	Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
8	BHS	BHS	Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
9	BLO	BLO	Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
10	NC	NC	No Connect.
11	ILIM-	ILIM-	Differential Current-Limit Input. Connect to most negative end of the external current-sense resistor.
12	VSS	VSS	Power Ground for Phase A and Phase B.
13	ILIM+	ILIM+	Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
14	ALO	ALO	Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
15	AHS	AHS	Phase A High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
16	AHO	AHO	Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
17	AHB	AHB	Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and A_{HS}. An on-board bootstrap diode is connected from V_{DD} to A_{HB}.
18	VDD	VDD	Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to V_{SS} with a minimum 2.2 µF ceramic capacitor.
19	DLY	DLY	Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
20	VSS	VSS	Phase C Power and Control Circuitry Ground.
21	CLO	CLO	Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
22	CHS	CHS	Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.

TABLE 3-1: QFN PIN FUNCTION TABLE

Pin Number QFN	Pin Name		Description
	MIC4607-1	MIC4607-2	
23	CHO	CHO	Phase C High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
24	CHB	CHB	Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and CHS. An on-board bootstrap diode is connected from VDD to CHB.
25	NC	NC	No Connect.
26	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
27	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
28	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
EP	ePad	ePad	Exposed Heatsink Pad: Connect to GND for best thermal performance.

TABLE 3-2: TSSOP PIN FUNCTION TABLE

Pin Number TSSOP	Pin Name		Description
	MIC4607-1	MIC4607-2	
1	NC	NC	No Connect.
2	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
3	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
4	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
5	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
6	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
7	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
8	EN	EN	Active high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
9	FLT/	FLT/	Open Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
10	BHB	BHB	Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and B_{HS}. An on-board bootstrap diode is connected from V_{DD} to B_{HB}.
11	BHO	BHO	Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
12	BHS	BHS	Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
13	BLO	BLO	Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
14	ILIM-	ILIM-	Differential Current-Limit Input. Connect to most negative end of the external current-sense resistor.
15	VSS	VSS	Power Ground for Phase A and Phase B.
16	ILIM+	ILIM+	Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
17	ALO	ALO	Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.

TABLE 3-2: TSSOP PIN FUNCTION TABLE

Pin Number TSSOP	Pin Name		Description
	MIC4607-1	MIC4607-2	
18	AHS	AHS	Phase A High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
19	AHO	AHO	Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
20	AHB	AHB	Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and A_{HS}. An on-board bootstrap diode is connected from V_{DD} to A_{HB}.
21	VDD	VDD	Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to V_{SS} with a minimum 2.2 µF ceramic capacitor.
22	DLY	DLY	Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
23	VSS	VSS	Phase C Power and Control Circuitry Ground.
24	CLO	CLO	Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
25	CHS	CHS	Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
26	CHO	CHO	Phase C High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
27	CHB	CHB	Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and C_{HS}. An on-board bootstrap diode is connected from V_{DD} to C_{HB}.
28	NC	NC	No Connect.

4.0 TIMING DIAGRAMS

4.1 Non-Overlapping LI/HI Input Mode (MIC4607-1)

In non-overlapping LI/HI input mode, enough delay is added between the xLI and xHI inputs to allow xHS to be low before xLI is pulled high and similarly xLO is low before xHI goes high.

xHO goes high with a high signal on xHI after a typical delay of 35 ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35 ns (t_{HPHL}).

Likewise, xLI going high forces xLO high after typical delay of 35 ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35 ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

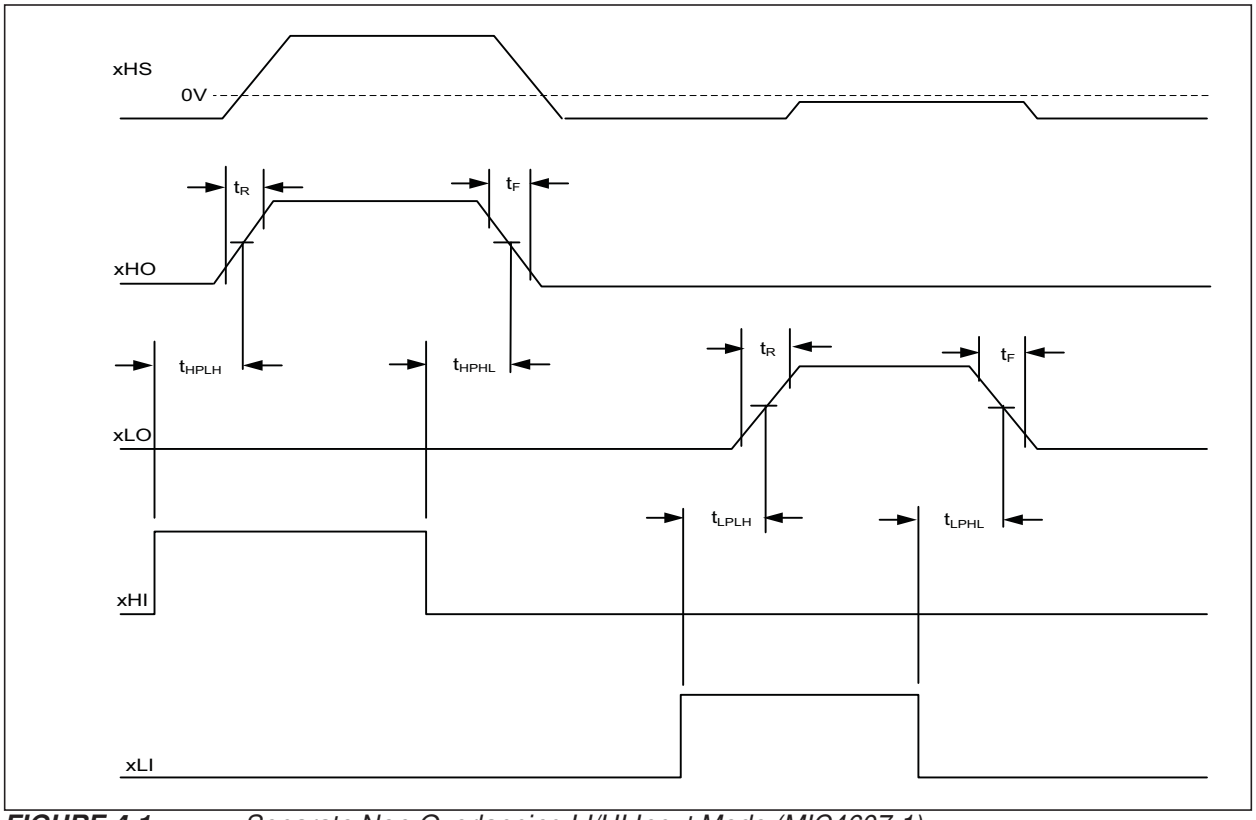


FIGURE 4-1: *Separate Non-Overlapping LI/HI Input Mode (MIC4607-1).*

Note 1: All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

2: “x” in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

4.2 Overlapping LI/HI Input Mode (MIC4607-1)

When xLI/xHI input high signals overlap, xLO/xHO output states are determined by the first output to be turned on. That is, if xLI goes high (ON), while xHO is high, xHO stays high until xHI goes low at which point, after a delay of t_{HOOFF} and when xHS < 2.2V, xLO goes high with a delay of t_{LOON}. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250 ns will set "HS latch" allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35 ns delay gated by HI going low. Conversely, xHI going high (ON) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to < 1.9V. Delay from xLI going low to xLO falling is t_{LOOFF} and delay from xLO < 1.9V to xHO being on is t_{HOON}.

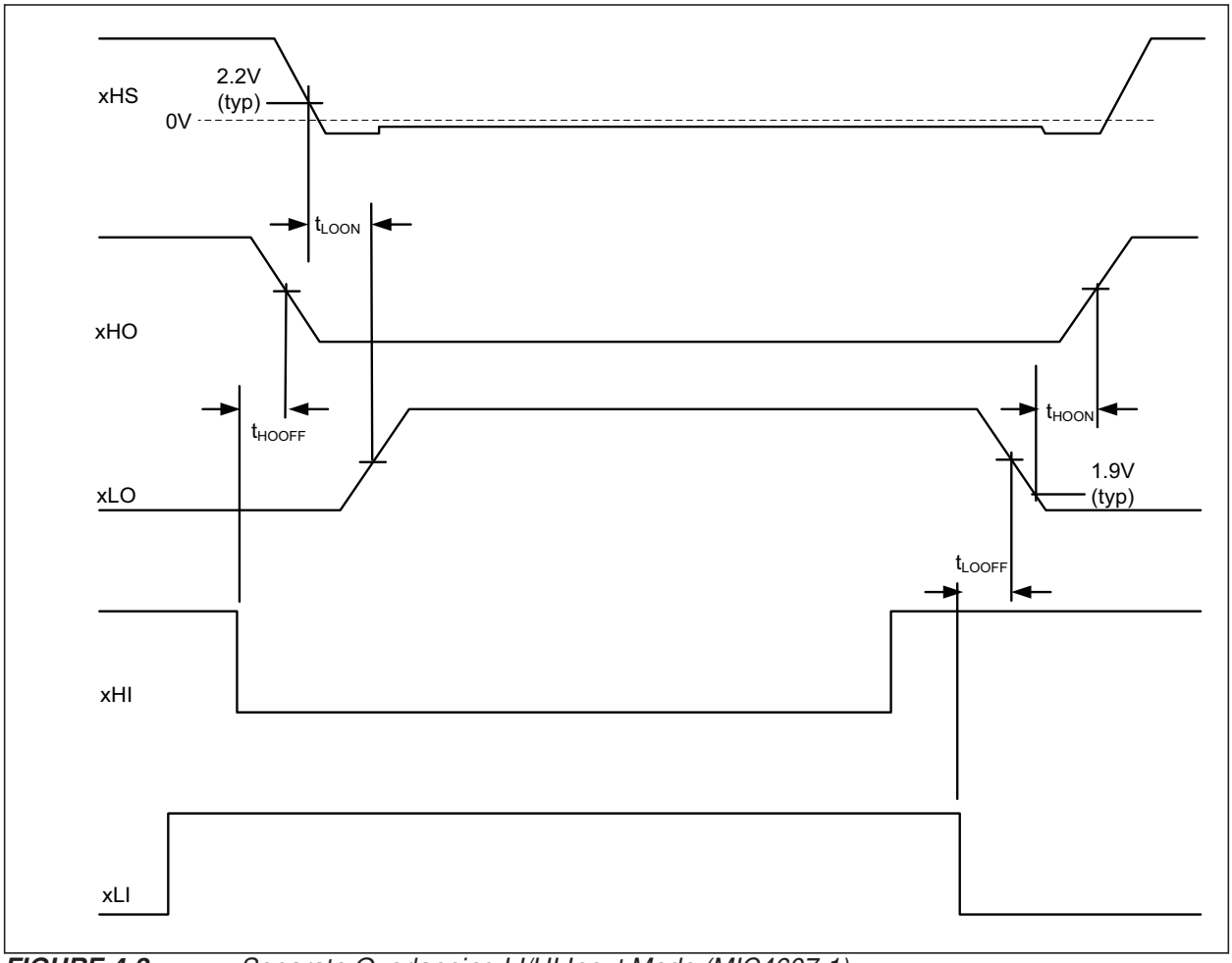


FIGURE 4-2: *Separate Overlapping LI/HI Input Mode (MIC4607-1).*

4.3 PWM Input Mode (MIC4607-2)

A low going xPWM signal applied to the MIC4607-2 causes xHO to go low, typically 35ns (t_{HOOFF}) after the xPWM input goes low, at which point the switch node, xHS, falls (1 – 2).

When xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and xLO goes high, typically within 35 ns (t_{LOON}) (3-4). xHS falling below 2.2V sets a latch that can only be reset by xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250 ns will set “HS latch” allowing xLO to go high.

A 35 ns delay gated by xPWM going low can determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35ns (t_{LOOFF}) (5 – 6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35 ns (t_{HOON}) (7 – 8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

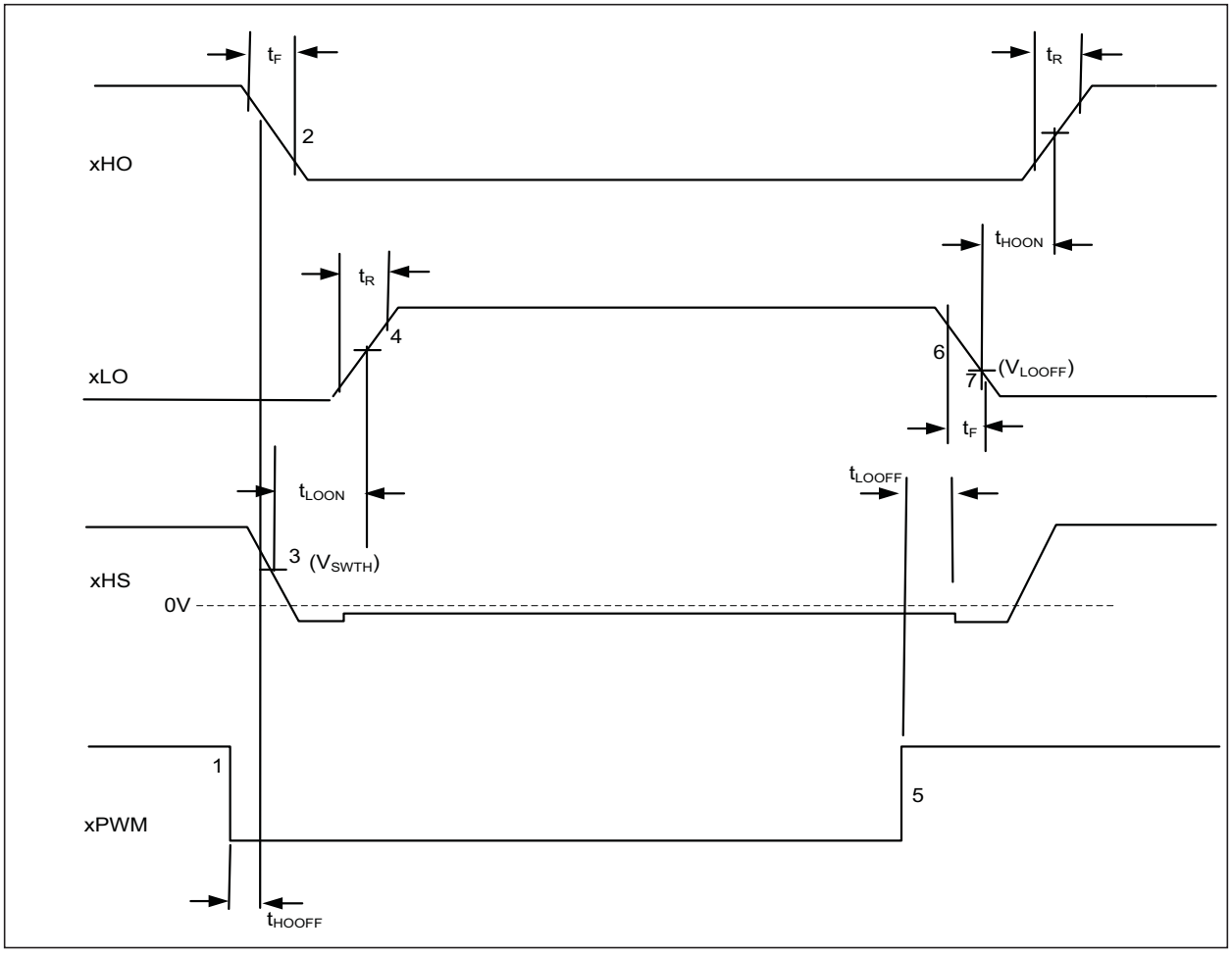


FIGURE 4-3: *PWM Mode (MIC4607-2).*

4.4 Overcurrent Timing Diagram

The motor current is sensed in an external resistor that is connected between the low-side MOSFET's source pins and ground. If the sense resistor voltage exceeds the rising overcurrent threshold (typically 0.2V), all LO and HO outputs are latched off and the FLT/ pin is pulled low. Once the outputs are latched off, an internal current source (typically 0.44 µA) begins to charge up the external C_{DLY} capacitor. The outputs remain latched off and all xLI/xHI (or xPWM) input signals are ignored until the voltage on the C_{DLY} capacitor rises above the V_{DLY+} threshold (typically 1.5V), which resets the latch on the first rising edge of any LI input of the MIC4607-1 (or falling edge on any PWM input for the MIC4607-2).

Once this occurs, the C_{DLY} capacitor is discharged, the FLT/ pin returns to a high impedance state and all outputs will respond to their respective input signals.

On startup, the current limit latch is reset during a rising V_{DD} or a rising EN pin voltage to assure normal operation.

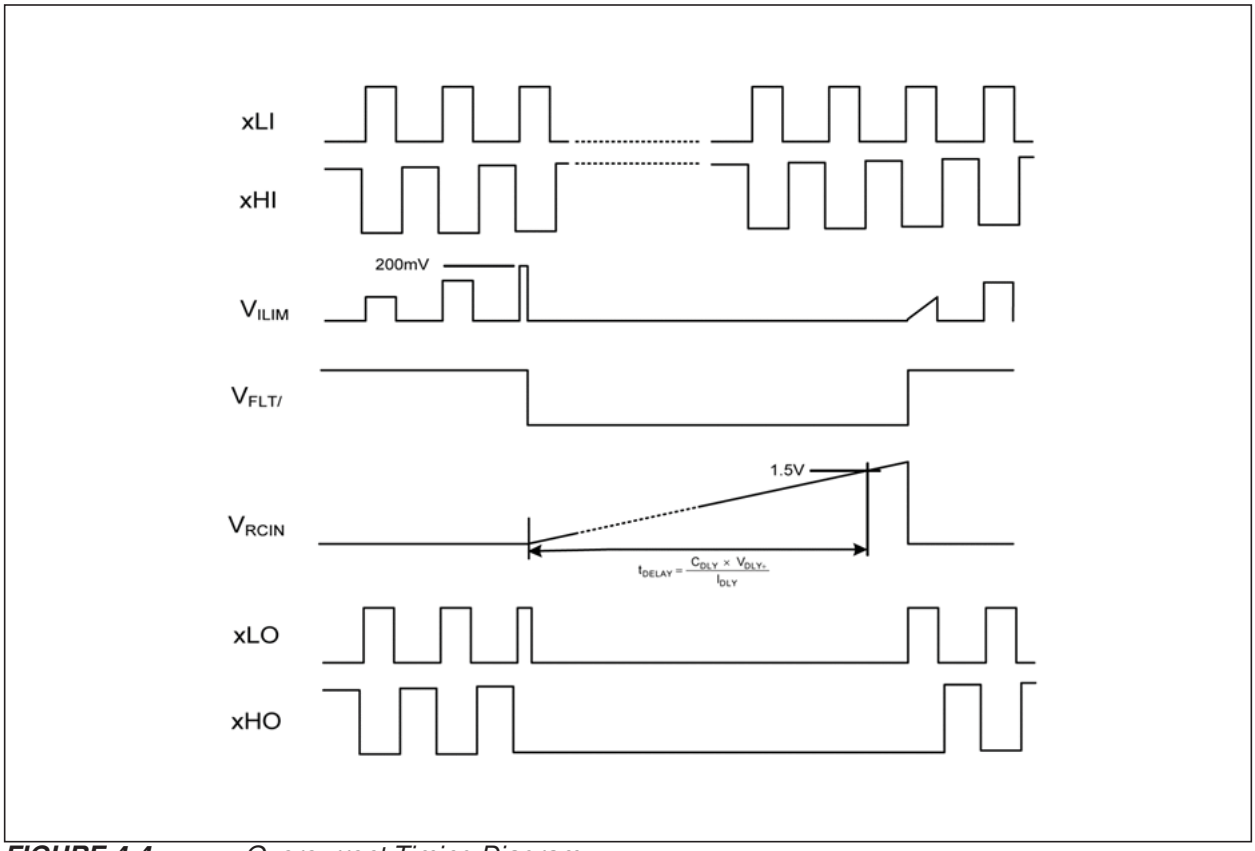


FIGURE 4-4: *Overcurrent Timing Diagram.*

5.0 FUNCTIONAL DESCRIPTION

The MIC4607 is a non-inverting, 85V three-phase MOSFET driver designed to independently drive all six N-Channel MOSFETs in a three-phase bridge. The MIC4607 offers a wide 5.5V to 16V VDD operating supply range with either six independent TTL inputs (MIC4607-1) or three PWM inputs, one for each phase (MIC4607-2). Refer to the Functional Diagram section.

The drivers contain input buffers with hysteresis, four independent UVLO circuits (three high-side and one low-side), and six output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to its HS pin. Each phase has an internal diode that is used by the bootstrap circuits to provide the drive voltages for each of the three high-side outputs. A programmable overcurrent protection circuit turns off all outputs during an overcurrent fault.

5.1 Startup and UVLO

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuits monitor the voltage between the xHB and xHS pins. Hysteresis in the UVLO circuits prevent system noise and finite circuit impedance from causing chatter during turn-on.

5.2 Enable Inputs

There is one external enable pin that controls all three phases. A logic high on the enable pin (EN) allows for startup of all phases and normal operation. Conversely, when a logic low is applied on the enable pin, all phases turn-off and the device enters a low current shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. Do not leave the EN pin floating.

5.3 Input Stage

All input pins (xLI and xHI) are referenced to the V_{SS} pin. The MIC4607 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the V_{DD} supply voltage and there is no dependence between I_{VDD} and the input signal amplitude. This feature makes the MIC4607 an excellent level translator that will drive high level gate threshold MOSFETs from a low-voltage PWM IC.

5.4 Low-Side Driver

The low-side driver is designed to drive a ground (V_{SS} pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external power device. Refer to Figure 5-1.

A high level applied to the xLI pin causes V_{DD} to be applied to the gate of the external MOSFET. A low level on the xLI pin grounds the gate of the external MOSFET.

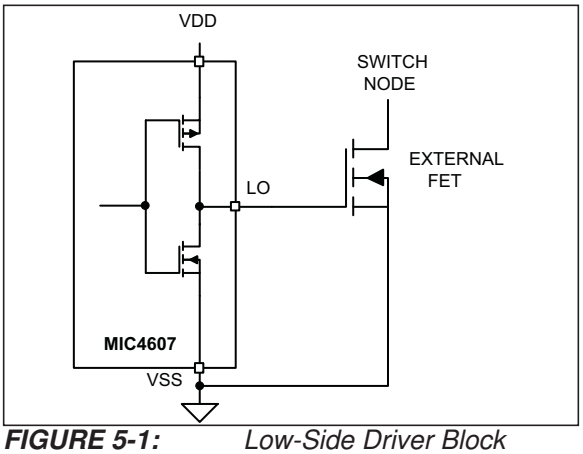


FIGURE 5-1: *Low-Side Driver Block Diagram.*

5.5 High-Side Driver and Bootstrap Circuit

Figure 5-2 illustrates a block diagram of the high-side driver and bootstrap circuit. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

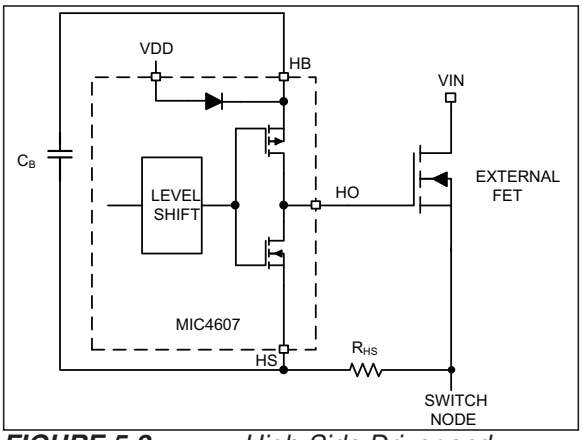


FIGURE 5-2: *High-Side Driver and Bootstrap-Circuit Block Diagram.*

A low-power, high-speed, level-shifting circuit isolates the low side (V_{SS} pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 5-3 (only Phase A illustrated), the AHS pin is at ground potential while the low-side MOSFET is on. The internal diode charges capacitor C_B to V_{DD}-V_F during this time (where V_F is

the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging. During this time, the high-side MOSFET is kept ON by the voltage across capacitor C_B.

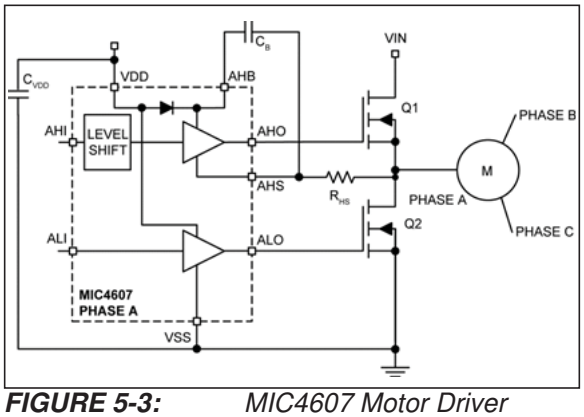


FIGURE 5-3: *MIC4607 Motor Driver Example.*

5.6 Programmable Gate Drive

The MIC4607 offers programmable gate drive, meaning the MOSFET gate drive (gate-to-source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in selecting the proper MOSFETs for a given application. Different MOSFETs require different V_{GS} characteristics for optimum R_{DSON} performance. Typically, the higher the gate voltage (up to 16V), the lower the R_{DSON} achieved. For example, as shown in Figure 5-4, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but R_{DSON} is 5.2 mΩ. If driven to 10V, R_{DSON} is 4.1 mΩ – a decrease of 20%.

In low-current applications, the losses due to R_{DSON} are minimal, but in high-current motor drive applications such as power tools, the difference in R_{DSON} can lower the efficiency, reducing run time.

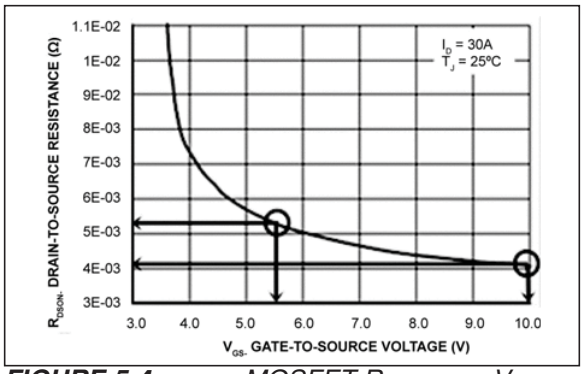


FIGURE 5-4: *MOSFET R_{DSON} vs. V_{GS}.*

5.7 Overcurrent Protection Circuitry

The MIC4607 provides overcurrent protection for the motor driver circuitry. It consists of:

- A comparator that senses the voltage across a current-sense resistor
- A latch and timer that keep all gate drivers off during a fault
- An open-drain pin that pulls low during the fault.

If an overcurrent condition is detected, the FLT/ pin is pulled low and the gate drive outputs are latched off for a time that is determined by the DLY pin circuitry. After the delay circuitry times out, a high-going edge on any of the LI pins (for the MIC4607-1 version) or a low-going edge on any of the PWM pins (for the MIC4607-2 version) is required to reset the latch, de-assert the FLT/ pin and allow the gate drive outputs to switch.

For additional information, refer to the Timing Diagrams section as well as the Functional Diagram section.

5.7.1 ILIM

The ILIM+ and ILIM- pins provide a Kelvin-sensed circuit that monitors the voltage across an external current sense resistor. This resistor is typically connected between the source pins of all three low-side MOSFETs and power ground. If the peak voltage across this resistor exceeds the VI_{LIM+} threshold, it will cause all six outputs to latch off. Both pins should be shorted to V_{SS} ground if the overcurrent features is not used.

5.7.2 DLY

A capacitor connected to the DLY pin determines the amount of time the gate drive outputs are latched off before they can be restarted.

During normal operation, the DLY pin is held low by an internal MOSFET. After an over-current condition is detected, the MOSFET turns off and the external capacitor is charged up by an internal current source. The outputs remain latched off until the DLY pin voltage reaches the V_{DLY+} threshold (typically 1.5V).

The delay time can be approximately calculated using Equation 5-1.

EQUATION 5-1:

$$t_{DLY} = \frac{C_{DLY} \times V_{DLY-}}{I_{DLY}}$$

5.7.3 FLT/

This open-drain output is pulled low while the gate drive outputs are latched off after an over-current condition. It will de-assert once the DLY pin has reached the V_{DLY+} threshold and a rising edge occurs on any LI pin (for the MIC4607-1) or a falling edge on any PWM pin (MIC4607-2).

During normal operation, the internal pull-down MOSFET is of the pin is high impedance. A pull-up resistor must be connected to this pin.

6.0 APPLICATION INFORMATION

6.1 Adaptive Dead Time

For each phase, it is important that both MOSFETs of the same phase branch are not conducting at the same time or V_{IN} will be shorted to ground and current will "shoot through" the MOSFETs. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing. The high switching current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive Dead Time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 6-1 shows an equivalent circuit of the high-side gate drive.

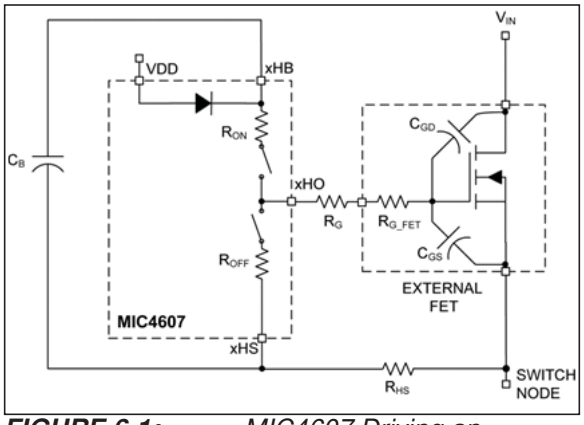


FIGURE 6-1: *MIC4607 Driving an External MOSFET.*

The internal gate resistance (R_{G_FET}) and any external damping resistor (R_G) and HS pin resistor (R_{HS}), isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

The MIC4607 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time. Figure 6-2 illustrates how the adaptive dead-time circuitry works.

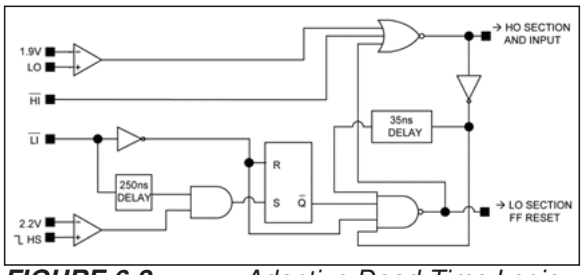


FIGURE 6-2: *Adaptive Dead-Time Logic Diagram.*

For the MIC4607-2, a high level on the xPWM pin causes $\overline{HI}$ to go low and $\overline{LI}$ to go high. This causes the xLO pin to go low. The MIC4607 monitors the xLO pin voltage and prevents the xHO pin from turning on until the voltage on the xLO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4607 drives the xHO pin high. Monitoring the xLO voltage eliminates any excessive delay due to the MOSFET driver's turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the xLO pin voltage settle out. If an external resistor is used between the xLO output and the MOSFET gate, it must be made small enough to prevent excessive voltage drop across the resistor during turn-off. Figure 6-3 illustrates using a diode (D_{LS}) and resistor (R_{LS2}) in parallel with the gate resistor to prevent a large voltage drop between the xLO pin and MOSFET gate voltages during turn-off.

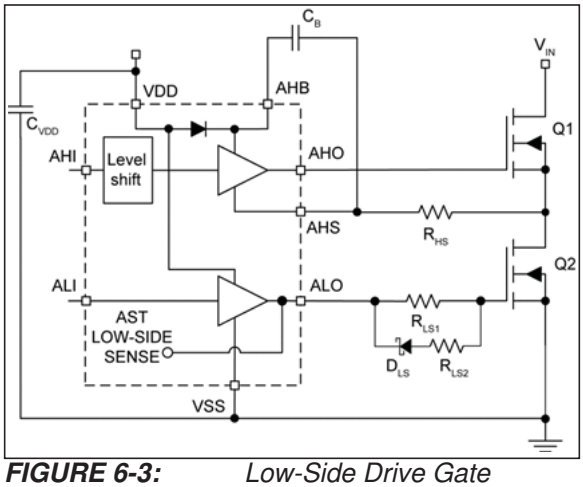


FIGURE 6-3: *Low-Side Drive Gate Resistor Configuration.*

A low on the xPWM pin causes $\overline{HI}$ to go high and $\overline{LO}$ to go low. This causes the xHO pin to go low after a short delay (t_{HOOFF}). Before the xLO pin can go high, the voltage on the switching node (xHS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the xHO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET

turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), ensuring proper operation.

The internal logic circuits also ensure a “first on” priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width can result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead-time circuit in the MIC4607 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit’s control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 6-4 shows the dead time (<20 ns) between the high- and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

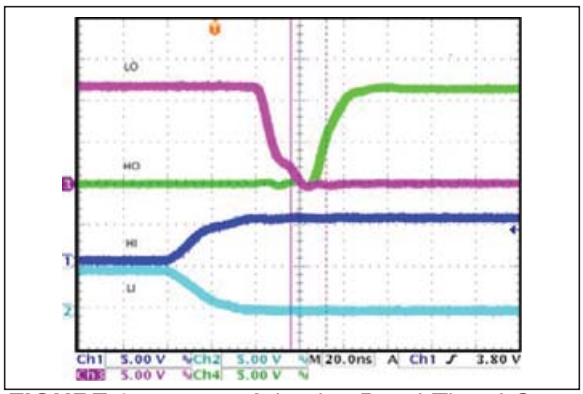


FIGURE 6-4: *Adaptive Dead-Time LO (LOW) to HO (HIGH).*

Table 6-1 contains truth tables for the MIC4607-1 (independent TTL inputs) and Table 6-2 is for the MIC4607-2 (PWM inputs) that details the “first on” priority as well as the failsafe delay (t_{SWTO}).

TABLE 6-1: MIC4607-1 TRUTH TABLE

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go HIGH until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes LOW.

TABLE 6-2: MIC4607-2 TRUTH TABLE

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	0	1	xHO will not go HIGH until xLO falls below 1.9V.

6.2 HS Node Clamp

A resistor/diode clamp between the switching node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 6-5 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and possibly a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recom-

mended. If the HS pin voltage exceeds 0.7V, a diode between the xHS pin and ground is recommended. The diode reverse voltage rating must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

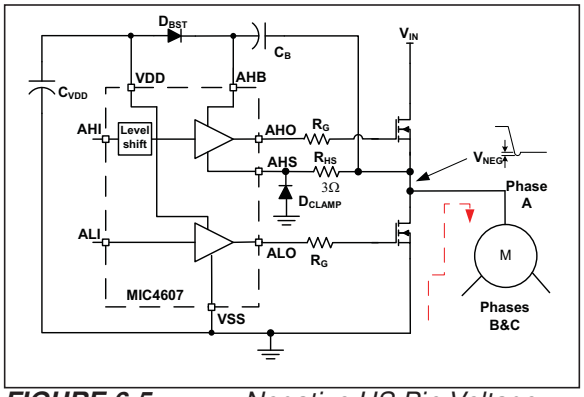


FIGURE 6-5: *Negative HS Pin Voltage.*

6.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

6.4 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by Equation 6-1.

EQUATION 6-1:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:

Q_{GATE}	Total gate charge at $V_{HB} - V_{HS}$.
f_S	Gate drive switching frequency.

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 6-2:

$$Pdiode_{FWD} = I_{F(AVE)} \times V_F$$

Where:

V_F	Diode forward voltage drop.

There are three phases in the MIC4607. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3 µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode (Figure 6-6). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated with the formula in Equation 6-3:

EQUATION 6-3:

$$Pdiode_{REV} = I_R \times V_{REV} \times (1 - D)$$

Where:

I_R	Reverse current flow at V_{REV} and T_J.
V_{REV}	Diode reverse voltage.
D	Duty cycle = $t_{ON} \times f_S$.

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.