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MICRF114

Low-Power Integrated Sub-GHz Wireless RF Transmitter

General Features

- Fully Integrated Low-Power Sub-GHz RF Transmitter
- Single-Pin Crystal Oscillator with Integrated Programmable Load Capacitor
- Wide Operating Voltage Range: 1.8V to 3.6V
- Industrial Temperature Range: -40°C to +85°C
- Low-Current Consumption: 0.2 µA in Sleep mode, 11.7 mA in +10 dBm Transmit mode
- Fast Turn-On and Turn-Off Times
- Small Footprint 6-pin SOT-23 Package

RF/Analog Features

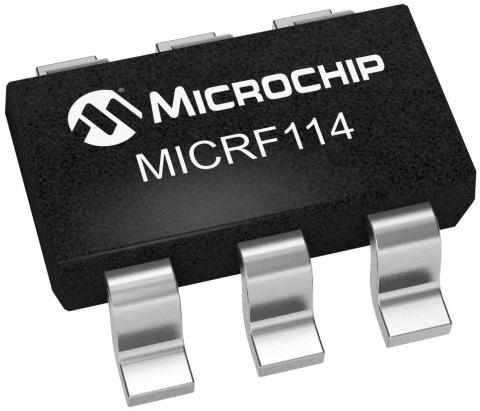
- Fully Integrated VCO and PLL Loop Filter
- Single-Ended RF Output with Easy Antenna Matching
- Wide Operating Frequency Range: 285 MHz to 445 MHz
- Transmit Power Programmable in 1 dB steps from -2 dBm to +13 dBm
- Data Rate: Up to 115.2 kbps NRZ, 57.6 kbps Manchester Encoded
- On-Off Keying (OOK) Modulation with Power Ramp-Up Control
- Complies with US (FCC) and Canada (IC) Standards

Digital Features

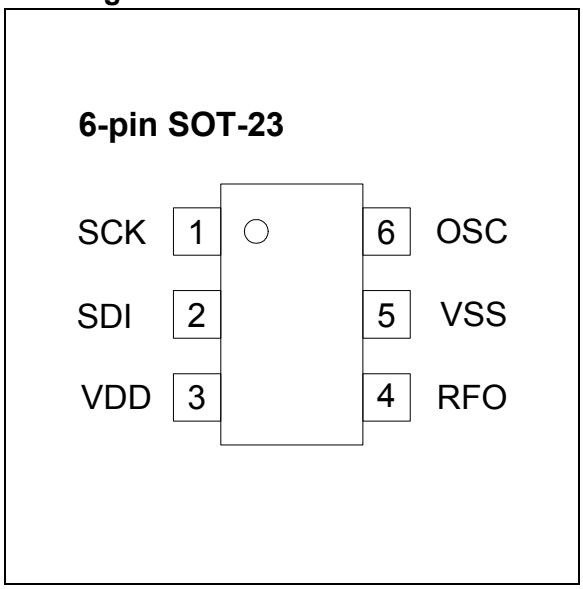
- Simple and Flexible 2-pin Proprietary Microcontroller (MCU) Interface
- Supports Proprietary Remote Control Protocols

Applications

- Remote Keyless Entry (RKE)
- Garage Door Opener (GDO)
- Alarm and Security Systems
- Command and Control
- Wireless Sensors
- Industrial Sensing and Control
- Smart Energy



Pin Diagram



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1.0 HARDWARE DESCRIPTION

1.1 Overview

The MICRF114 is a simple, low-cost OOK transmitter with programmable output power. It is primarily intended for command and control applications such as RKE and GDO. The transmitter is synthesizer based for high-frequency accuracy. It operates on a single frequency that is determined by the frequency of the crystal connected to the built-in reference oscillator. This frequency can be selected from a wide range. The more popular transmit frequencies require readily available crystal frequencies. For example, a 433.92 MHz transmit frequency requires a 13.56 MHz crystal. The RF performance of the transmitter is compliant with FCC and IC regulations and with some Japanese standards. European Telecommunications Standards Institute (ETSI) requirements can be met at low-radiated power.

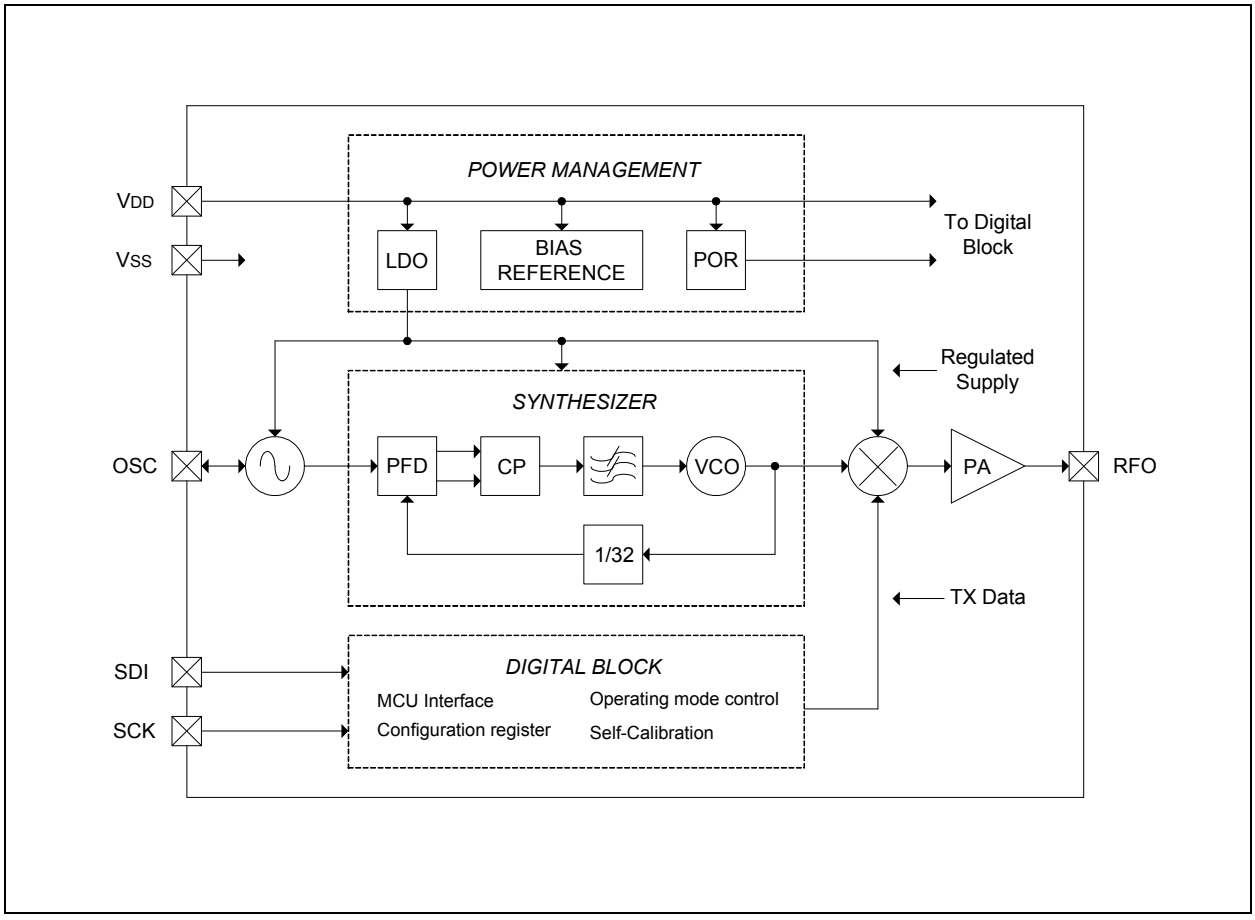
The MICRF114 is optimized for battery-powered applications. It features low-current consumption and can operate over a wide supply voltage range. Internal circuits sensitive to supply voltage variations run from the on-chip Low Dropout (LDO) regulator. To reduce pin count and system Bill of Materials (BOM), the LDO regulator does not need an external capacitor for stability, and the single-pin reference oscillator has a integrated programmable crystal load capacitor. The single-ended RF output enables easy matching to monopole antennas with a minimal number of external components.

A 2-wire proprietary MCU interface is used to program the parameters of the MICRF114 to select its operating mode and to input the transmit data packet. A built-in self-calibration circuit ensures consistent performance over the operating frequency range and against temperature variations. Initial calibration is automatically performed during Power-on Reset (POR). Recalibration can be initiated by the MCU that controls the application when required.

1.2 Block Diagram

Figure 1-1 shows the MICRF114 block diagram.

FIGURE 1-1: MICRF114 ARCHITECTURE BLOCK DIAGRAM



1.3 Pin Descriptions

Table 1-1 describes the MICRF114 pins.

TABLE 1-1: MICRF114 PIN DESCRIPTIONS

Pin	Name	Type	Description
1	SCK	Digital Input	MCU interface serial clock input
2	SDI	Digital Input	MCU interface serial configuration or TX data input
3	VDD	Power	Positive supply voltage
4	RFO	Analog Output	RF TX output
5	VSS	Power	Ground reference
6	OSC	Analog Input	Reference crystal connection

1.4 Power Management

The MICRF114 has a single power pin and a single ground pin. The sensitive analog blocks run from an internal LDO, which does not need an external capacitor. A bias and reference circuit provides reference voltage to the LDO and bias currents to all analog blocks.

The digital block runs from the unregulated supply. This enables communication with the MCU even when most of the blocks (including the LDO) are turned off to save power. Additionally, the MICRF114 retains its self-calibration result and user-programmable parameters in this low-power state. To get the highest possible efficiency, the RF Power Amplifier (PA) block runs directly from the unregulated supply.

A POR circuit keeps the MICRF114 in a Reset state until the supply voltage is sufficient for proper operation of the digital block. The POR event resets the device control state machine and the Configuration register to their default state. A Reset is also triggered by sufficiently large supply voltage glitches and brown-out.

1.5 MCU Interface

A proprietary 2-wire serial interface consisting of a clock line and a data line is utilized to control the operation of the MICRF114 and to input the transmit data packet. Special start and stop conditions on these two lines indicate the beginning and end of communication with the MCU. Except during these Start and Stop bits, the MCU must change the data only when the clock is at logic low. Control and Configuration bits are sent synchronously, and the MICRF114 samples the data on the rising edge of the clock. Transmit data is sent asynchronously with the clock held low. During transmission, the serial data line is connected directly to the RF modulator. The assembly and timing of the data packet are the responsibilities of the MCU.

1.6 Device Control

Data transmission start and stop are always initiated by the MCU. Programmable transmit parameters are stored in a single 16-bit register. The value in this register is kept as long as the supply voltage is present. The MCU can rewrite the register at the beginning of each transmission. Immediately after POR or at the beginning of a transmission, an internal state machine turns on the various blocks of the MICRF114 with the required sequence and timing and then performs an automatic calibration of the device when required. The MCU must wait for these operations to be completed before sending the transmit data packet.

An initial calibration is done after POR. The calibration result is kept as long as the supply voltage is present. Recalibration can be requested by the MCU when required.

1.7 Crystal Oscillator

The reference frequency source is a single-pin crystal oscillator. The transmit frequency is 32 times the reference. Thus, the relative accuracy of the crystal oscillator directly determines the accuracy of the transmit frequency. The most popular transmit frequencies require standard and off-the-shelf low-cost crystals. The oscillator operates at parallel resonance. The load capacitor that the crystal requires is integrated to minimize the BOM. To accommodate various crystal types and compensate for PCB parasitic capacitances, the value of this load capacitor is programmable by the MCU.

The other function of the crystal oscillator is to provide a relatively accurate clock frequency for the automatic calibration circuit. As the crystal frequency is determined by the transmit frequency and can vary over a wide range, the clock is generated by dividing the crystal frequency by a programmable number that must be properly set to achieve the expected performance.

1.8 Frequency Synthesizer

The frequency synthesizer is a fully integrated PLL with a fixed feedback division ratio. It operates on a single frequency that is determined by the reference crystal. The VCO within the PLL operates directly at the transmit frequency to save power. The VCO also has a wide tuning range to cover most of the popular frequencies below 500 MHz.

1.9 Transmit Path

The main element of the transmit path is the RF Power Amplifier (PA). Since typical applications use monopole antennas, the output is single-ended. It must be biased to V_{DD} using an inductor. This configuration enables high-voltage swing, thereby reducing the required supply current for the specified output power. The output power is programmable by the MCU in 1 dB steps. This enables the current consumption and transmit range to be optimized according to the product requirements of the customers. Additionally, compliance with the relevant regulations can be ensured with different antenna gains.

To ease design-in and keep the BOM as low as possible, the output capacitance of the PA is programmable by the MCU. As a result, the impedance matching circuit between the RF output and the antenna requires fewer elements and is easier to optimize. A modulator circuit is used to control the slope of the output power ramping on and off. This is to prevent steep supply current transients which may result in a spectrum splatter.

NOTES:

2.0 FUNCTIONAL DESCRIPTION

2.1 Initialization

After applying the supply voltage, the MICRF114 is initialized by its built-in POR circuit. The POR is level sensitive. It starts to generate a Reset pulse for the internal logic when the rising supply voltage (V_{DD}) crosses a given threshold. The threshold level is chosen so that the operation of the digital circuits is already guaranteed at the beginning of the Reset pulse.

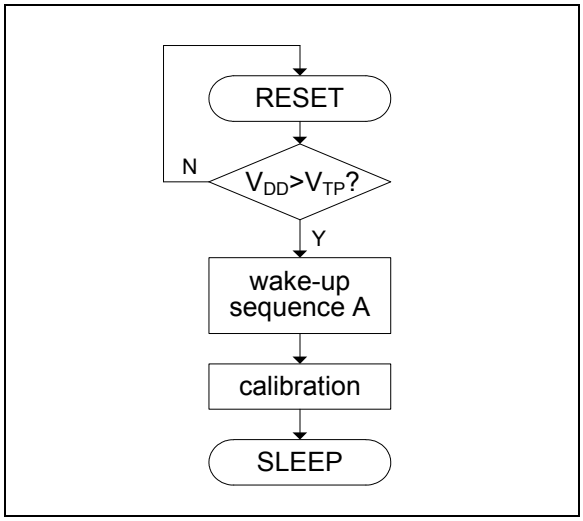
Initialization first involves resetting all internal state machines, setting the Configuration register to its default value, and executing a calibration sequence to guarantee proper operation of the frequency synthesizer. Blocks needed for calibration are turned on with the required sequence and timing. The result is stored after calibration, and all blocks are turned off to bring the MICRF114 into Sleep mode where it waits for the MCU to initiate transmission. The calibration result is kept as long as the supply voltage is present.

Figure 2-1 illustrates the simplified initialization flowchart where the Reset due to V_{DD} drops or brown-out is not shown. Additionally, it is not shown that a Reset condition in any state or during any sequence immediately brings the MICRF114 into its Reset state.

One of the advantages of the level-sensitive Reset is that the generation and length of the Reset pulse are mostly independent of the slope of the rising V_{DD}. Another advantage is that it triggers a Brown-out Reset (BOR) when V_{DD} goes below the V_{TP} threshold voltage. Refer to Figure 2-2.

Abrupt drops of the V_{DD} can disturb the operation of digital circuits even if the V_{DD} always stays above the threshold level during such a transient. The POR block also generates a Reset pulse after this kind of event if the voltage drop exceeds the V_{TG} threshold value.

FIGURE 2-1: INITIALIZATION FLOWCHART



2.2 Operating Modes

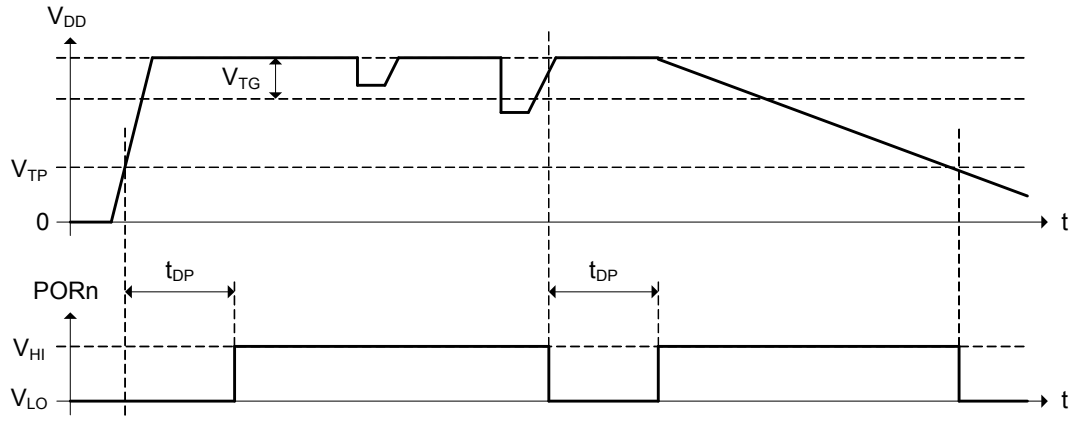
The MICRF114 has two main operating modes:

- Sleep mode
- Transmit mode

In Sleep mode, all the blocks (except the POR and the digital block) are powered down and wait to be woken up by the MCU. The current consumption is minimal because there is no activity within the digital block. After the wake-up sequence and the associated delay, MICRF114 enters Transmit mode. In Transmit mode, all blocks become active and an RF signal, modulated by the data stream sent by the MCU, is transmitted. Transmission can be terminated by the MCU without any time-out delay when required and the MICRF114 immediately goes back to Sleep mode.

Section 2.3 "Communication with the MCU" shows the main operating mode flowchart and the associated activity on the MCU interface.

FIGURE 2-2: POR OPERATION



Note: V_{HI} follows V_{DD}

2.3 Communication with the MCU

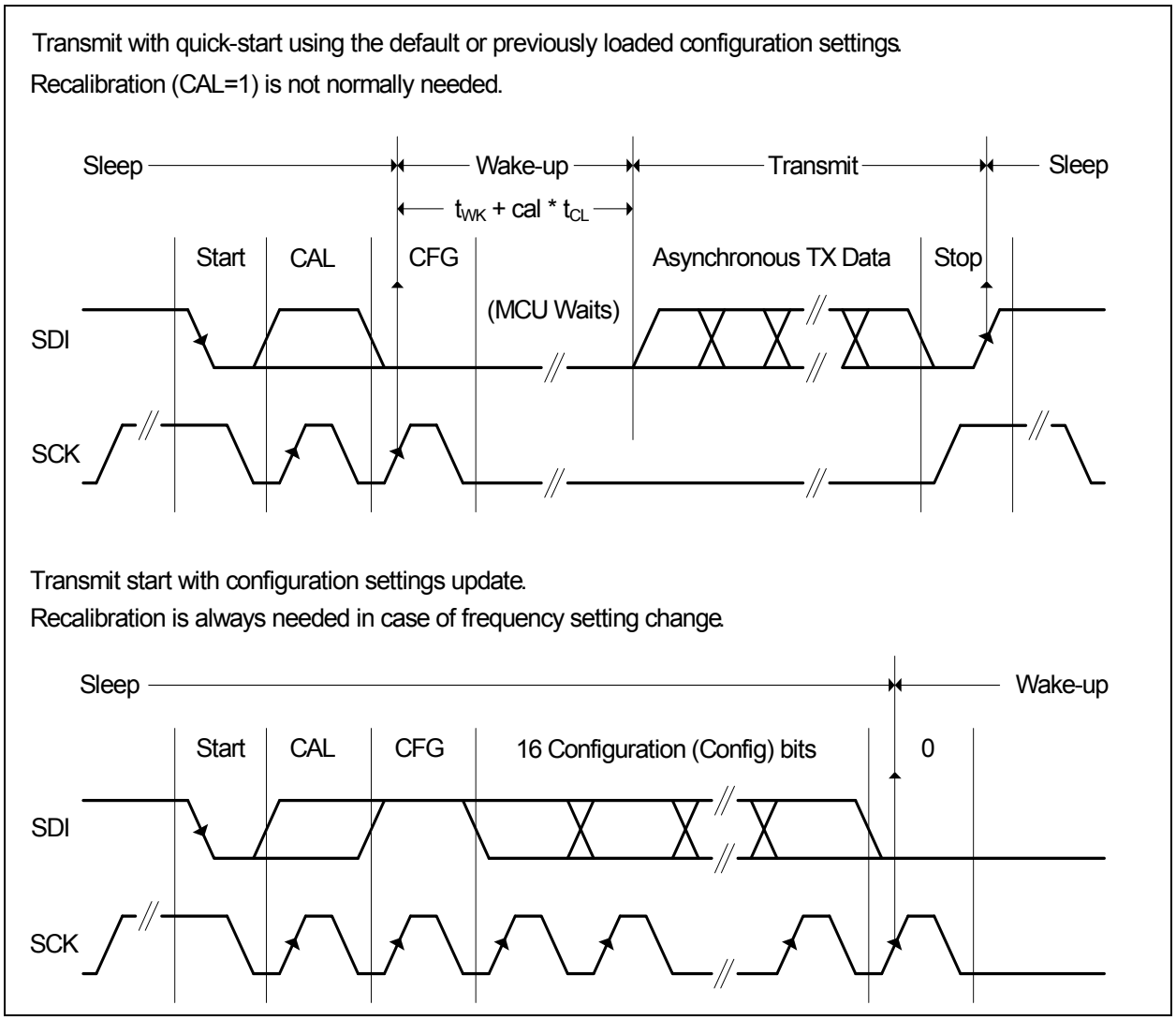
The communication between the MCU and the MICRF114 is one-directional and it is always initiated by the MCU. It uses a proprietary protocol that supports switching between the two operating modes, optional request for recalibration, reprogramming of the operating parameters (as needed), and transmit data input. The logic is active-high.

The communications protocol requires both the lines of Serial Clock (SCK) and Serial Data Input (SDI) to idle high. However, this is not the state with the lowest current consumption because the SCK input of the MICRF114 has an internal pull-down resistor to avoid unwanted clock transitions during the power-on process. In Sleep mode, the clock line can be pulled low to minimize the overall supply current.

Control and Configuration bits are sent synchronously after the Start bit. The two control bits, CAL and CFG, must always be present. If CAL is high, recalibration is performed before transmission. In this case, the wake-up time from Sleep mode to Transmit mode is longer. If CFG is high, the MCU must send 17 additional Configuration bits. The first 16 bits updates the 16-bit Transmit Parameter register within the MICRF114. The Most Significant bit (MSb) is sent first. The last bit must always be '0'. Figure 2-3 shows the two methods of starting transmission.

The wake-up sequence from Sleep mode to Transmit mode starts at the rising edge of the last clock pulse. This is the second or 19th clock, depending on the CFG bit setting.

FIGURE 2-3: COMMUNICATION PROTOCOL



After the wake-up delay, the MICRF114 starts to automatically transmit. Since the exact timing of this is unknown by the MCU, keep the transmit data input low until the maximum specified wake-up time passes. Although the MICRF114 wakes up earlier, it transmits '0', that is, no carrier. Transmit data is asynchronous and directly modulates the RF carrier. The MCU takes care of all timing and coding of the data in software. This is feasible due to the typical low-data rates and is necessary due to the great variety of proprietary protocols. The flowchart in Figure 2-4 shows the MICRF114 states during a normal operation cycle.

2.4 Parameter Selection

All transmit parameters of the MICRF114 are stored in a single 16-bit register. This is loaded with default values at POR. The MCU can modify these values before sending the transmit data. There are four distinct parameter fields in the register as shown in Table 2-1. To keep the MCU interface simple, only the complete register as a whole can be updated. Fields that need to remain unchanged must be reloaded with the same value. For example, the new register value is retained in Sleep mode until the next POR event.

FIGURE 2-4: TOP FLOWCHART

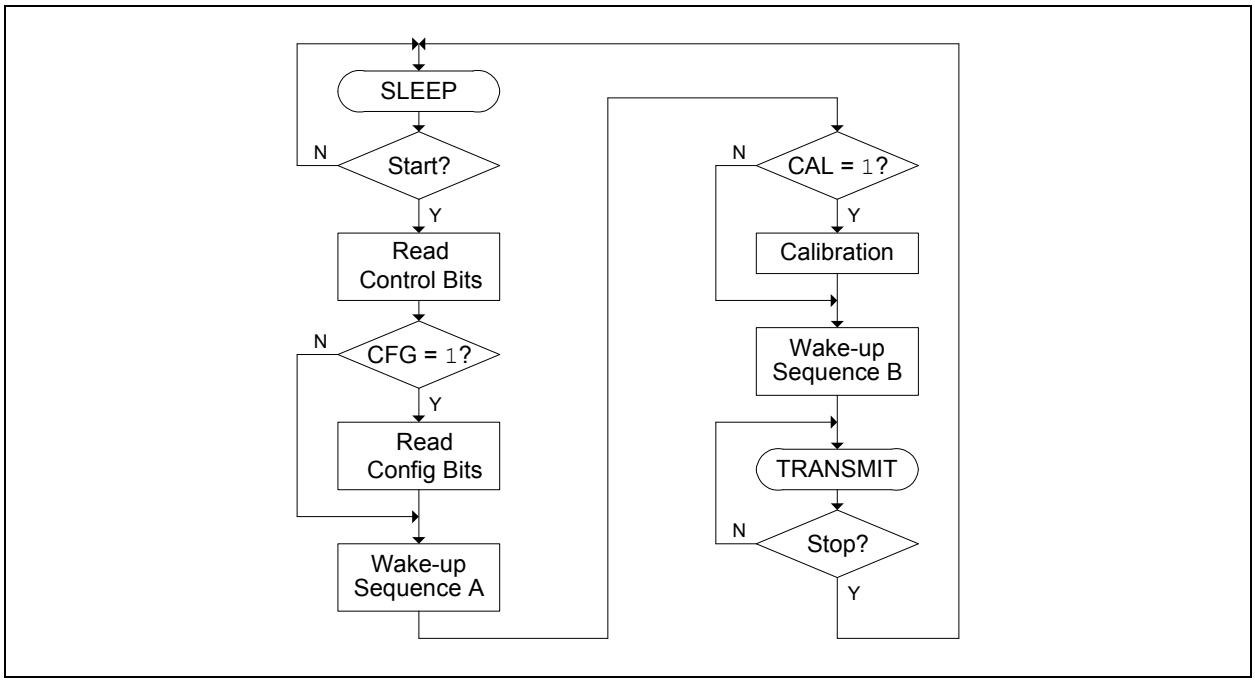


TABLE 2-1: TRANSMIT PARAMETERS OF MICRF114

Bit Range	Parameter	Field	Symbol	Default	
				Setting	Value
<15:13>	Transmit Frequency	F<2:0>	f_{TX}	0x7	425-445 MHz
<12:8>	Crystal Load Capacitor	X<4:0>	C_{XT}	0x16	18 pF
<7:4>	RF Transmit Power	P<3:0>	P_{TX}	0xC	+10 dBm
<3:0>	RF Output Tuning Capacitor	R<3:0>	C_{TX}	0x0	0 pF

Select the transmit frequency parameter to ensure that the actual operating frequency, which is determined by the selected crystal, falls into the frequency range defined by the parameter. Refer to Table 2-2.

TABLE 2-2: FREQUENCY RANGE

fTX range (MHz)		F<2:0>
Min	Max	
285	305	0
305	325	1
325	345	2
345	365	3
365	385	4
385	405	5
405	425	6
425	445	7

Equation 2-1 through Equation 2-1 show that the rest of the programmable parameters can be calculated from the Control bit fields.

EQUATION 2-1: CRYSTAL LOAD CAPACITOR

Crystal Load Capacitor:

$$C_{XT} = 7\ pF + X<4:0> * 0.5\ pF$$

EQUATION 2-2: RF TRANSMIT POWER

RF Transmit Power:

$$P_{TX} = -2\ dBm + P<3:0>\ dBm$$

EQUATION 2-3: RF OUTPUT TUNING CAPACITOR

RF Output Tuning Capacitor:

$$C_{TX} = 0\ pF + R<3:0> * 0.2\ pF$$

The operating frequency, the crystal load capacitor, and the RF output tuning capacitor settings depend on the selection of external components and, to a lesser extent, PCB layout. If these parameters are different from the default values, it must be set only once during the first transmission after a POR event.

2.5 Transmitting

The MICRF114 is normally in Sleep mode. The MCU always initiates entry into Transmit mode by sending a Start bit, the compulsory Control bits, and the optional Configuration bits to the MICRF114, which starts its wake-up sequence. After the wake-up delay, it transmits the data present on its SDI pin. The MCU holds the SDI pin low for the maximum specified wake-up time. If calibration is requested, the maximum specified calibration time must be added to the wake-up time.

Transmit parameters are not usually changed on the fly, and recalibration is not necessary. Therefore, the MCU can use the quick-start transmit sequence as described in **Section 2.3 "Communication with the MCU"**. However, except in the rare case that all default parameter settings are acceptable for the application, the first transmission after a POR event must include sending the required Configuration bits. Recalibration is always needed when the transmit frequency is in a band that is different from the default value.

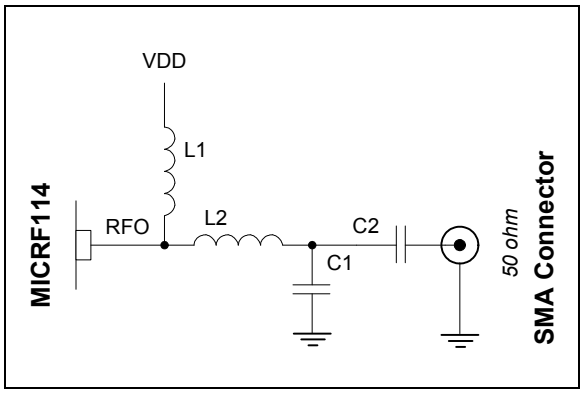
The MICRF114 stays in Transmit mode until the MCU sends a Stop bit and then reverts to Sleep mode without any time-out delay.

3.0 TYPICAL PERFORMANCE CURVES

3.1 Characterization Setup

The MICRF114 is characterized at the two most popular frequencies, 315 MHz and 433.92 MHz, over the whole operating temperature and supply voltage range. The results shown in **Section 3.2 "315 MHz Results"** and **Section 3.3 "433 MHz results"** are the average values taken from three devices, each coming from a typical wafer lot. The RF output of the MICRF114 is matched to 50 ohms to facilitate connection to a spectrum analyzer. Refer to Figure 3-1.

FIGURE 3-1: MATCHING CIRCUIT SCHEMATIC



Harmonic filtering is omitted. The measured power levels are calculated back to the RFO pin of the MICRF114, taking into account the losses of the characterization setup. Component values that are valid for the two frequencies are listed in Table 3-1.

TABLE 3-1: COMPONENT VALUES

Component	Frequency	
	315 MHz	433 MHz
L1	360 nH	330 nH
L2	39 nH	22 nH
C1	6.8 pF	5.6 pF
C2	9.1 pF	5.6 pF

Current consumption is measured with a 50% duty-cycle OOK modulation at 115.2 kbps data rate. Output power is measured in unmodulated, Continuous Wave (CW) mode. The reference spur level and the phase noise are also measured in CW mode at +10 dBm (nominal) output power setting. The phase noise is measured at 1 MHz offset from the carrier.

3.2 315 MHz Results

Figure 3-2 through Figure 3-7 show the average values measured at 315 MHz.

FIGURE 3-2: CURRENT CONSUMPTION, 0 dBm POWER SETTING

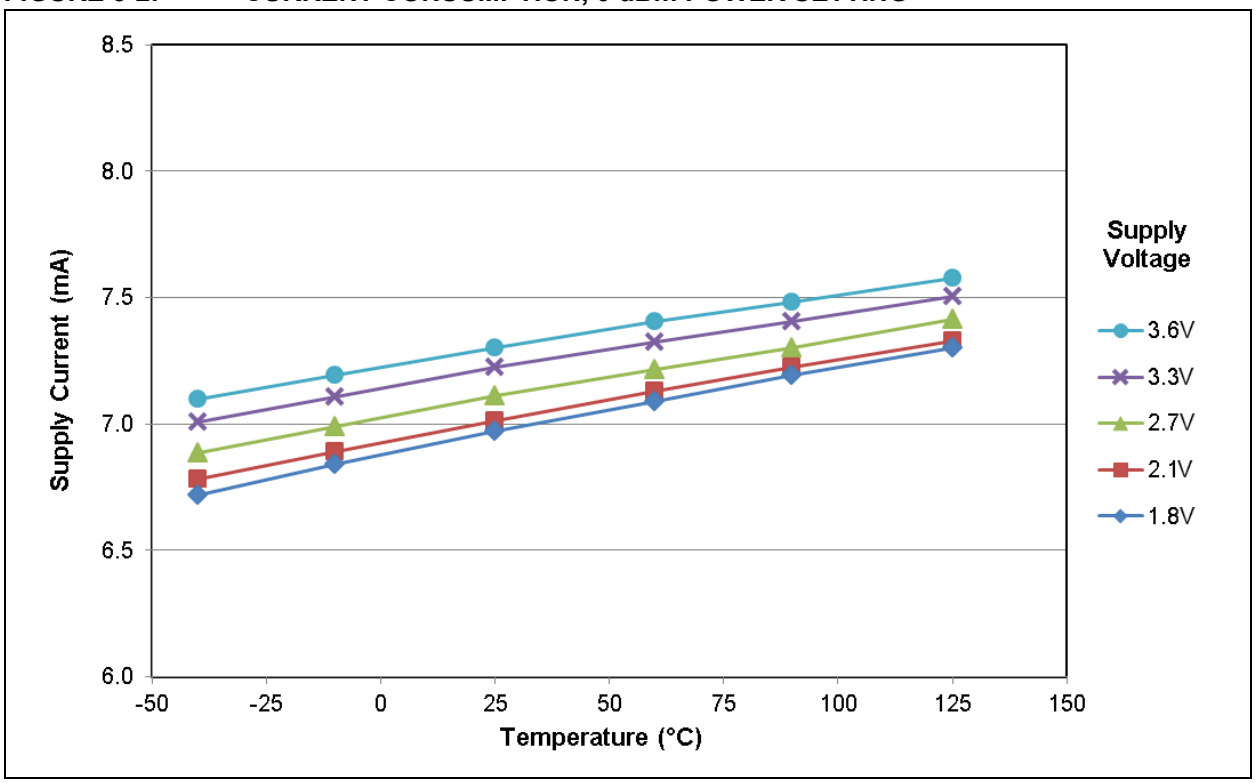


FIGURE 3-3: OUTPUT POWER, 0 dBm POWER SETTING

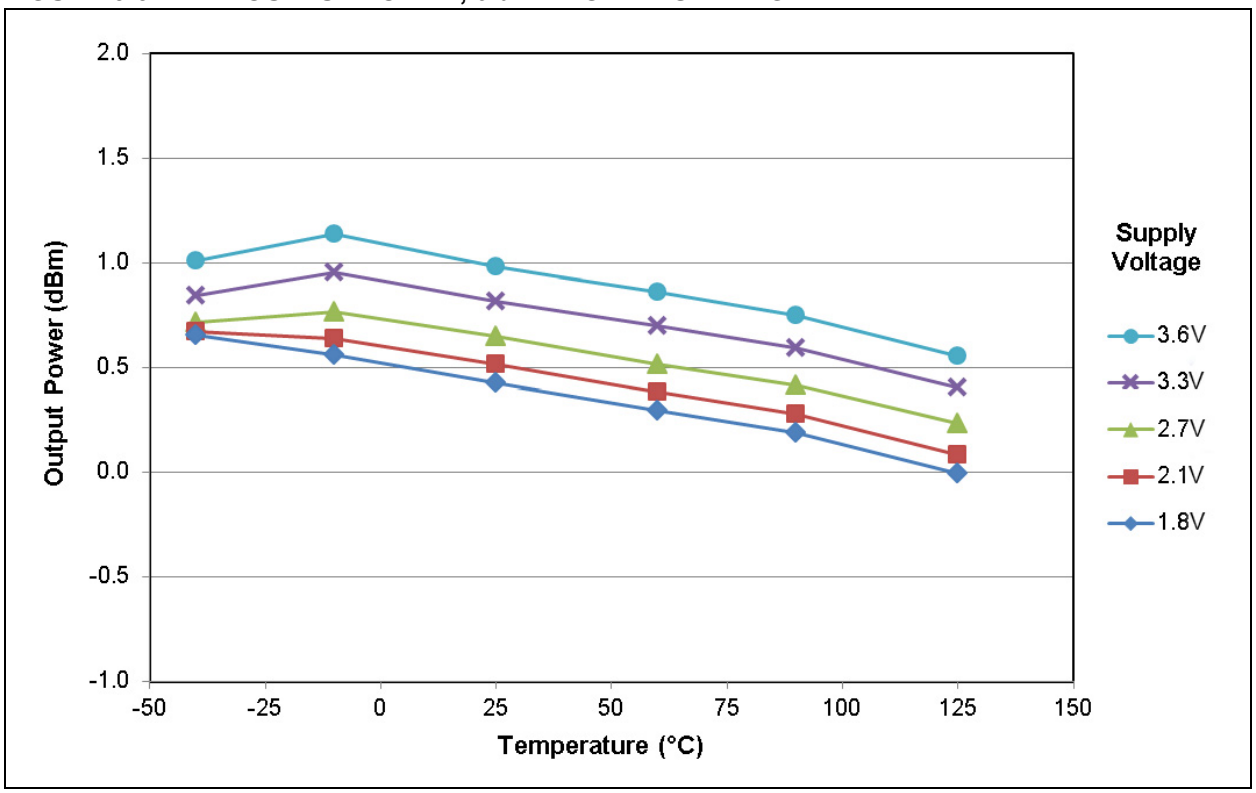


FIGURE 3-4: CURRENT CONSUMPTION, +10 dBm POWER SETTING

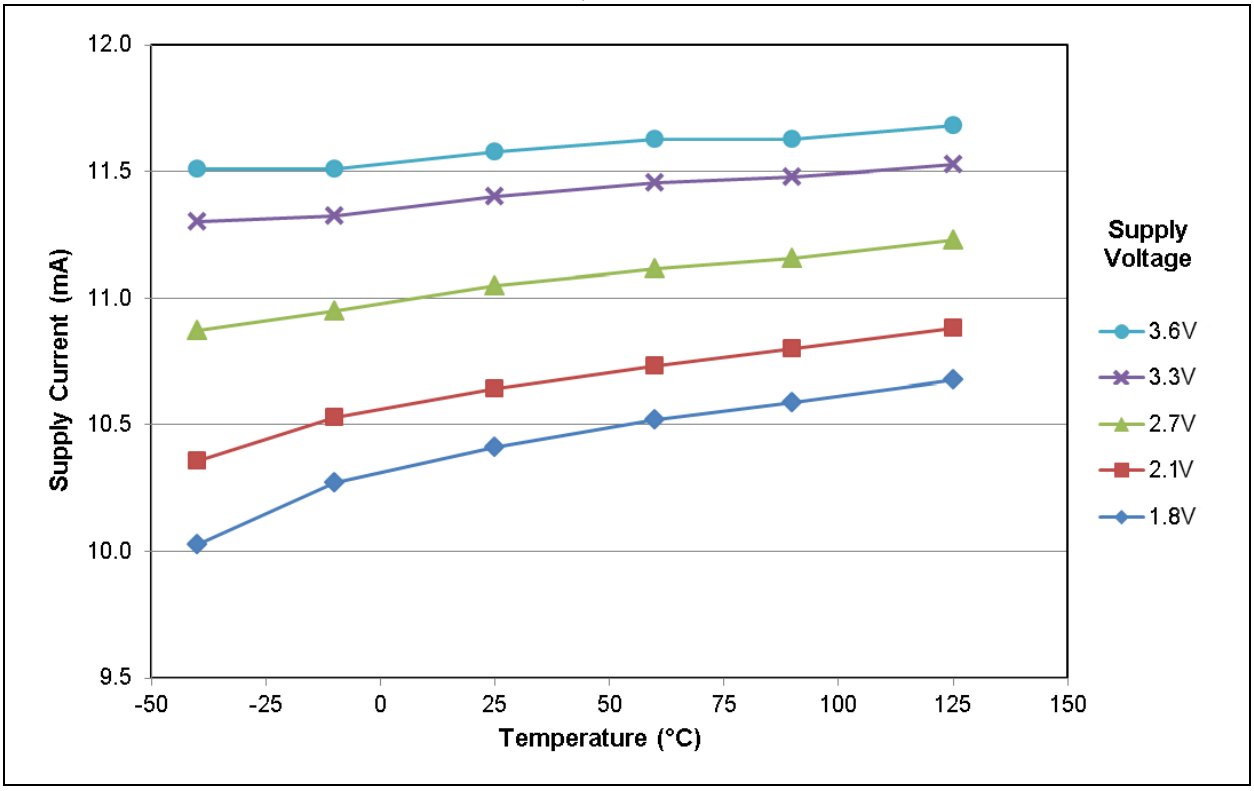


FIGURE 3-5: OUTPUT POWER, +10 dBm POWER SETTING

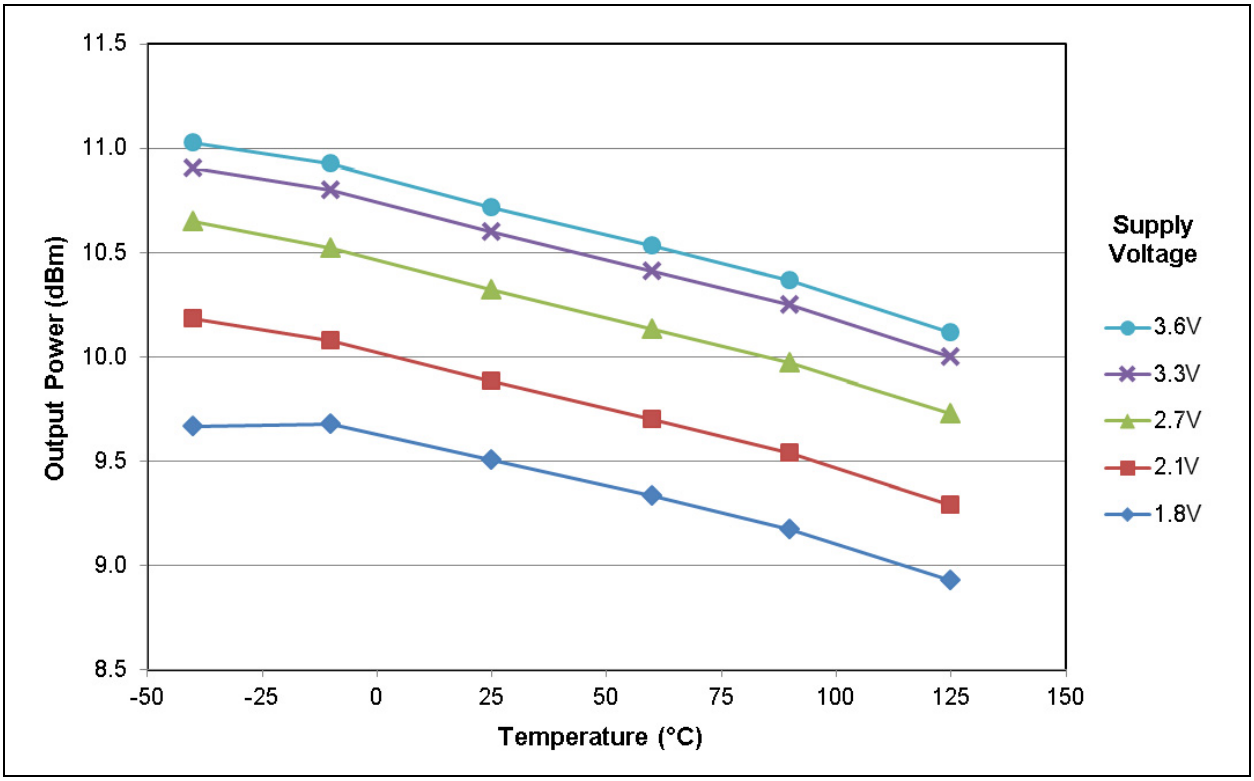


FIGURE 3-6: REFERENCE SPUR LEVEL

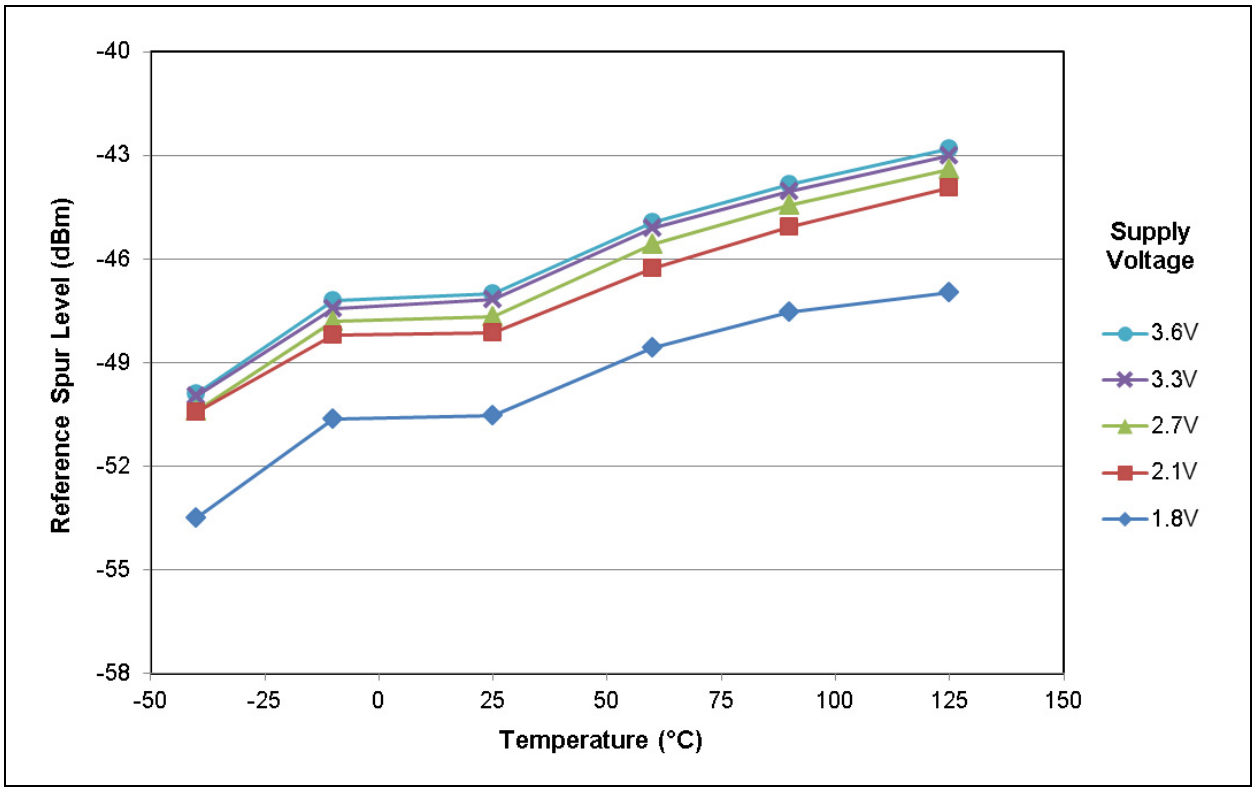
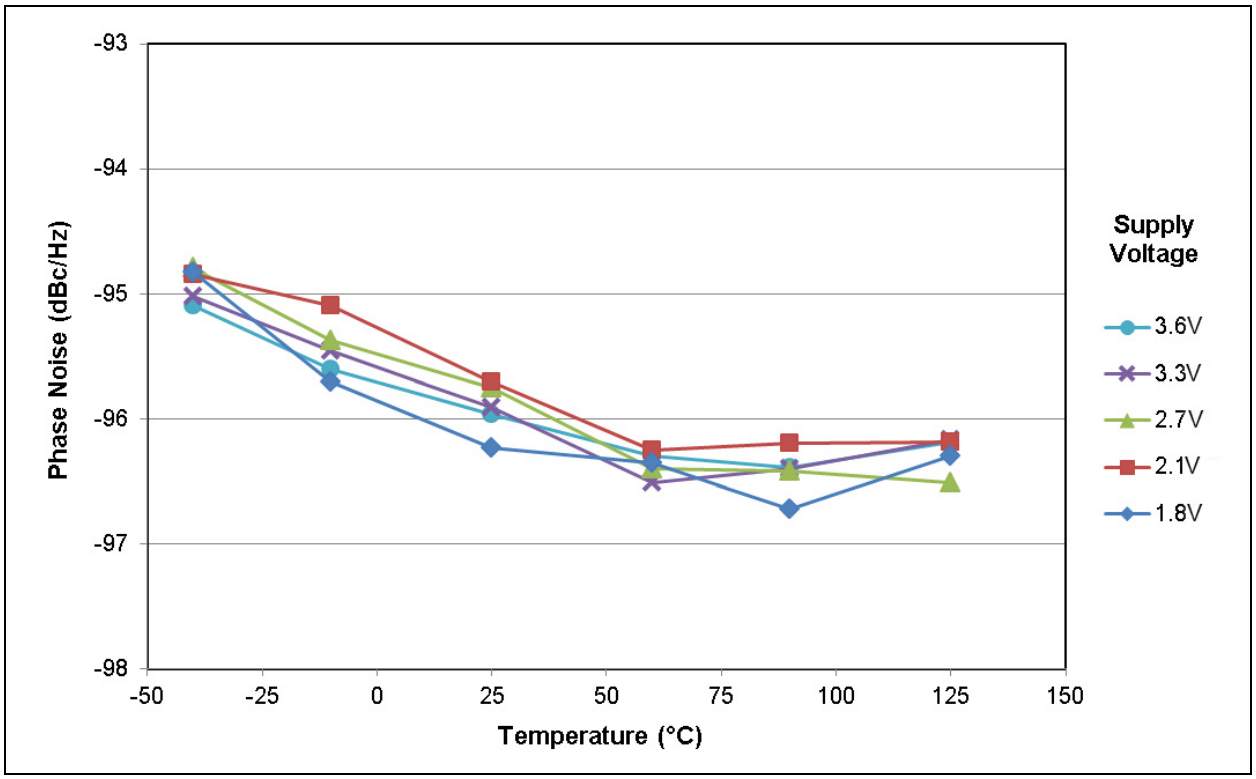


FIGURE 3-7: PHASE NOISE



3.3 433 MHz results

Figure 3-8 through Figure 3-13 show the average values measured at 433 MHz.

FIGURE 3-8: CURRENT CONSUMPTION, 0 dBm POWER SETTING

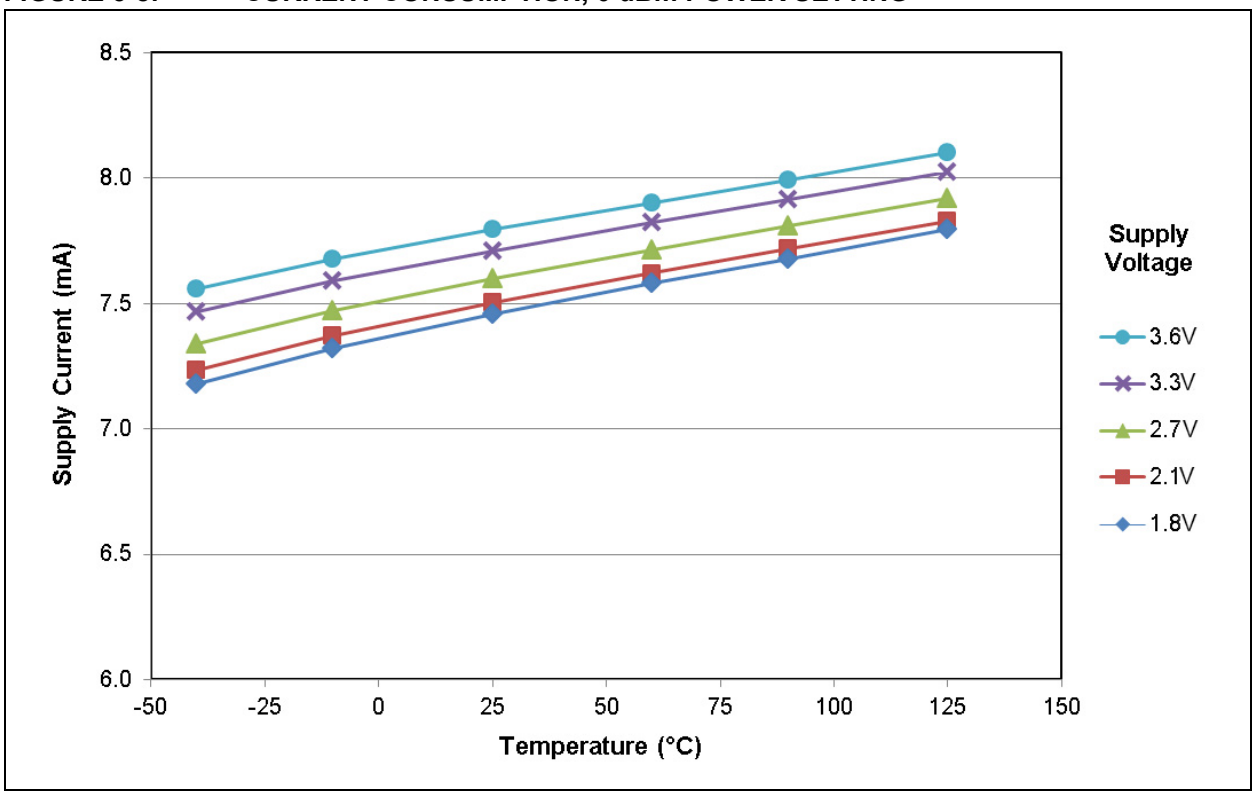


FIGURE 3-9: OUTPUT POWER, 0 dBm POWER SETTING

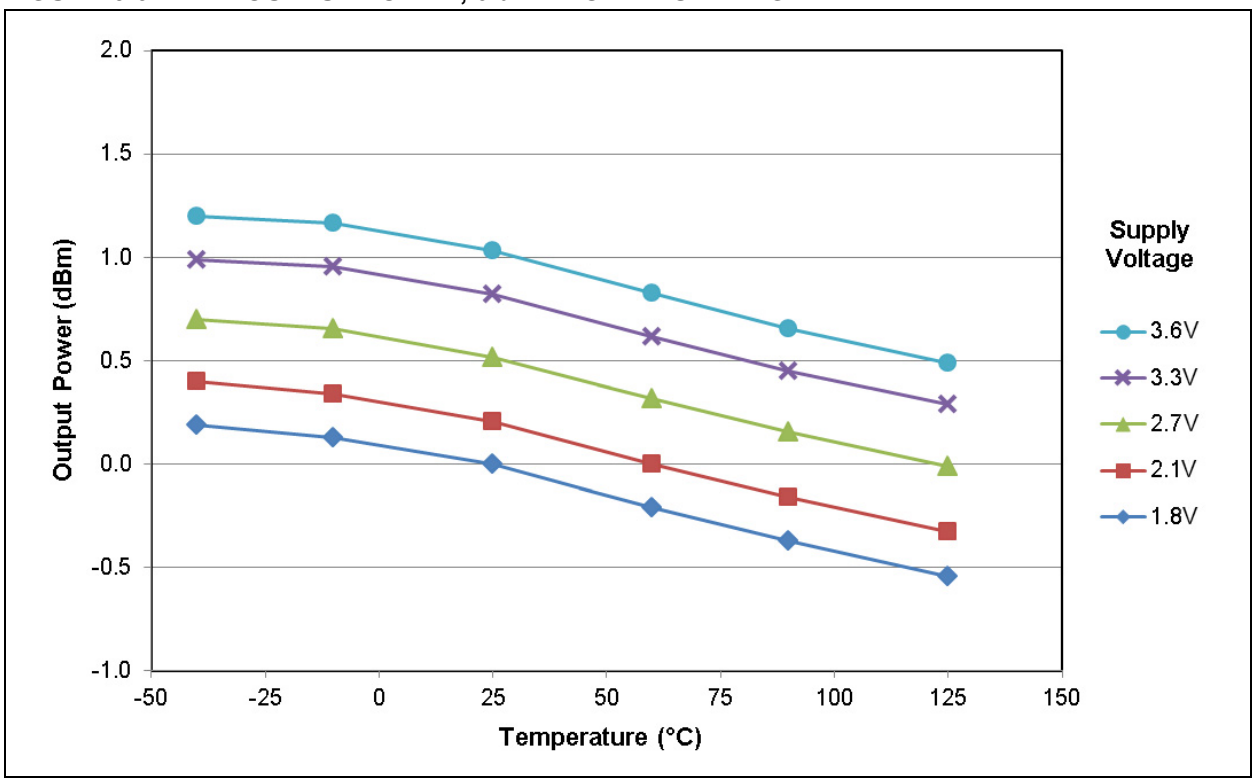


FIGURE 3-10: CURRENT CONSUMPTION, +10 dBm POWER SETTING

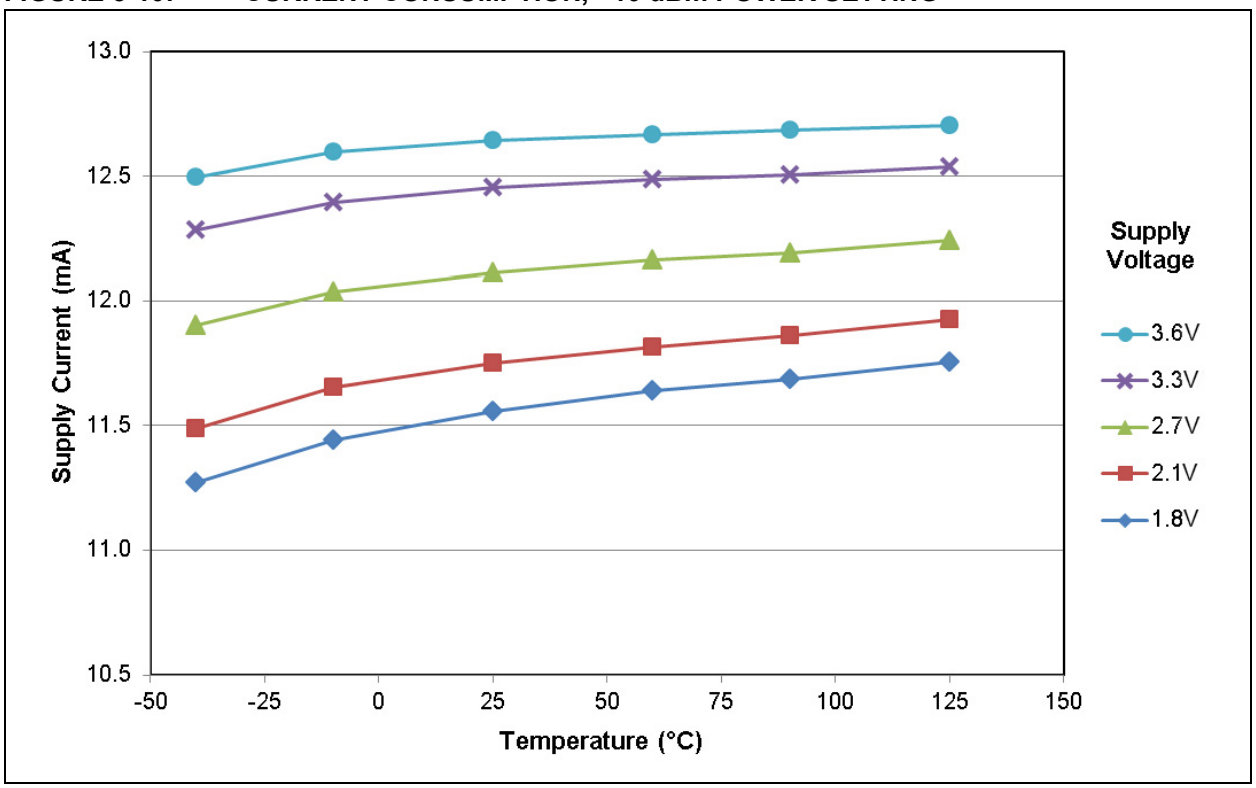


FIGURE 3-11: OUTPUT POWER, +10 dBm POWER SETTING

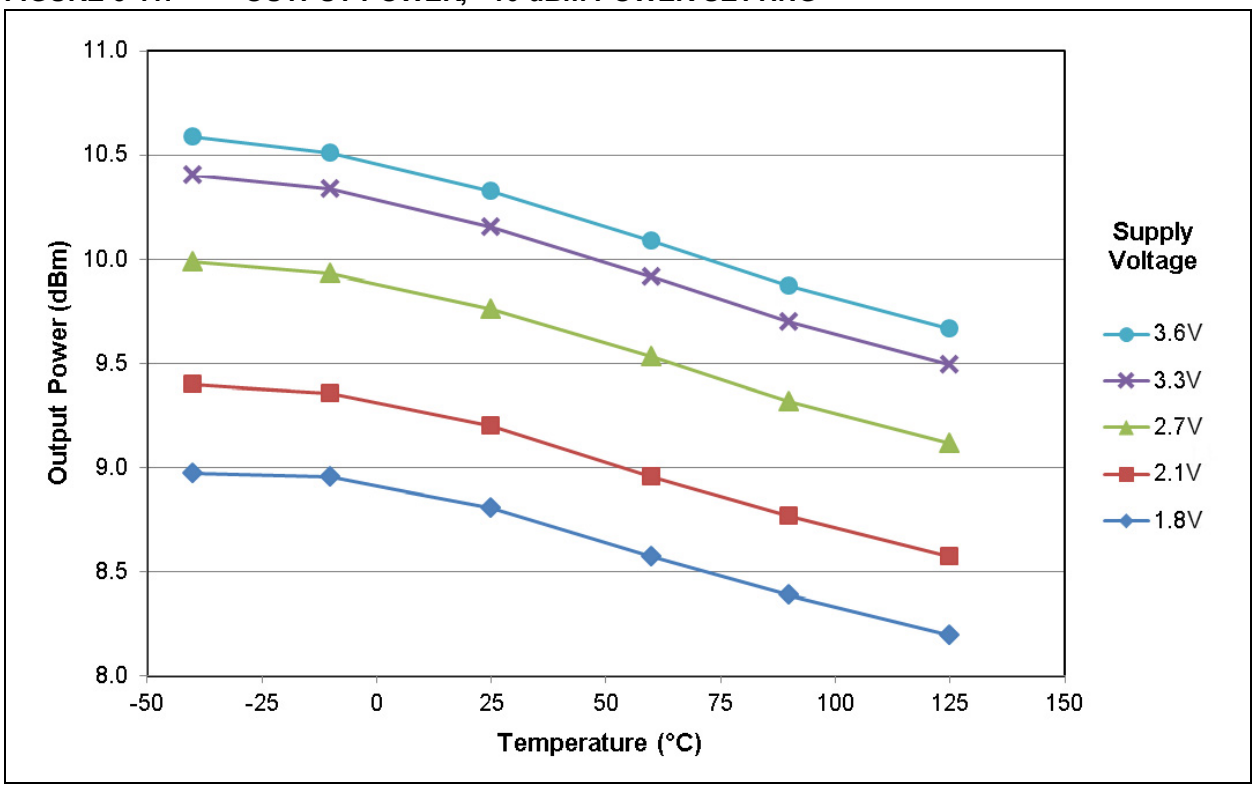


FIGURE 3-12: REFERENCE SPUR LEVEL

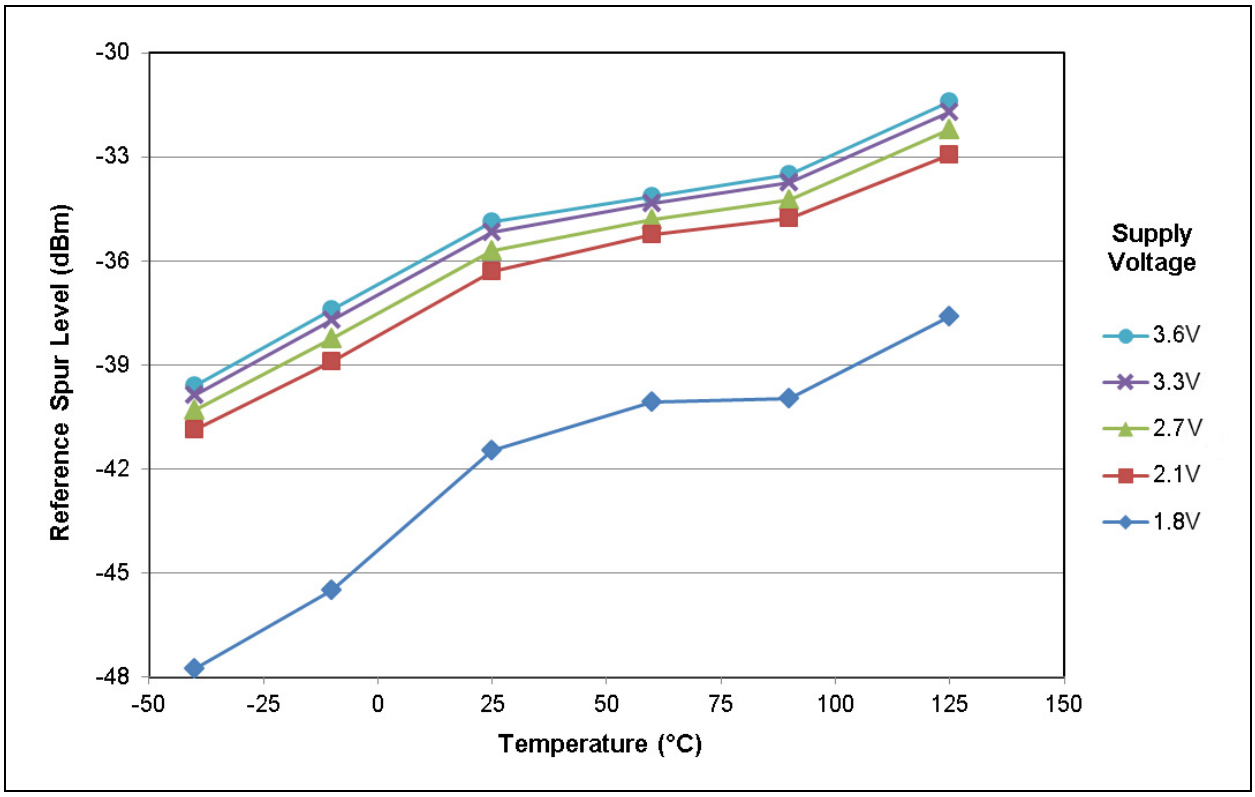
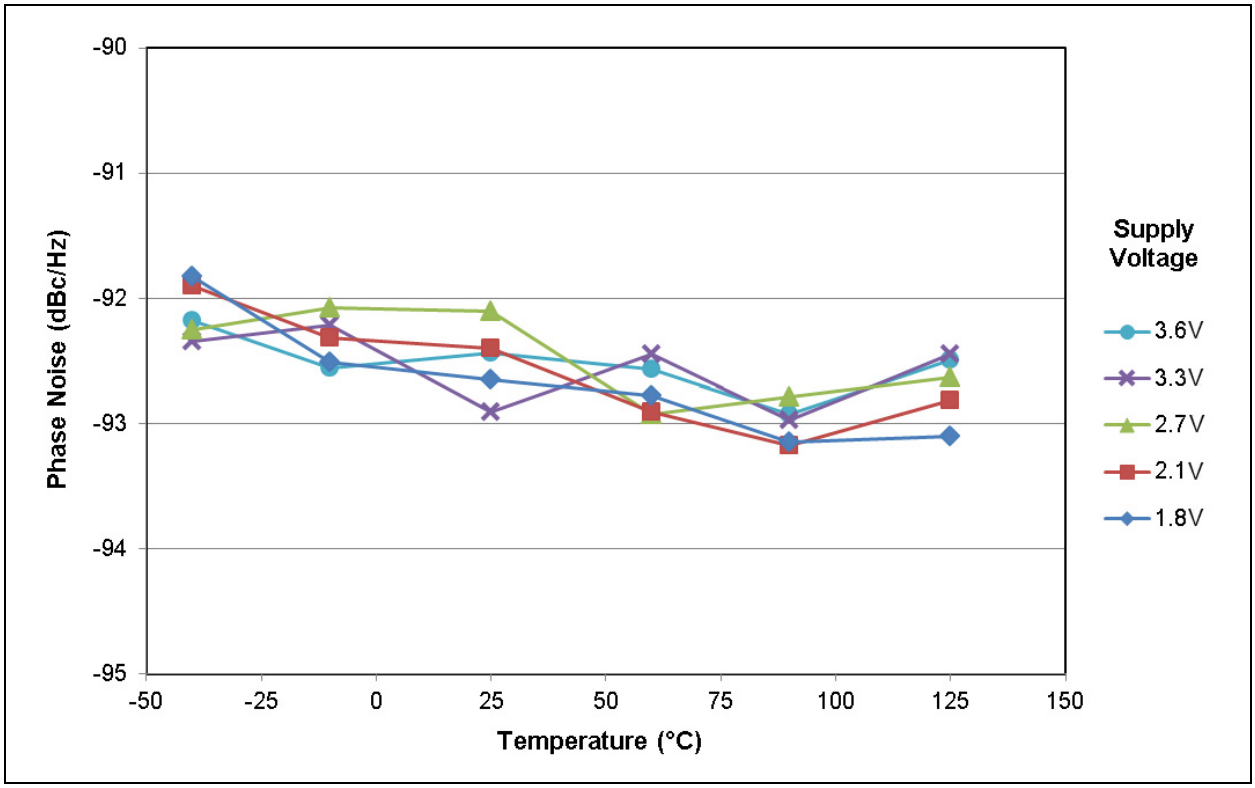


FIGURE 3-13: PHASE NOISE



NOTES:

4.0 APPLICATION CIRCUIT

4.1 50-ohm Matching Example

Figure 4-1 shows the RF section of the MICRF114 application circuit. The VSS pin potential is the ground reference for the whole circuit. The supply voltage (1.8V to 3.6V) is connected to the VDD pin. Capacitors C5 and C6 provide supply bypass (filtering). In every application, the MICRF114 has to be controlled by an MCU via the proprietary serial interface (SDI and SCK pins). The quartz crystal (X1) connected to the OSC pin determines the operating frequency which is 32 times the crystal resonance frequency.

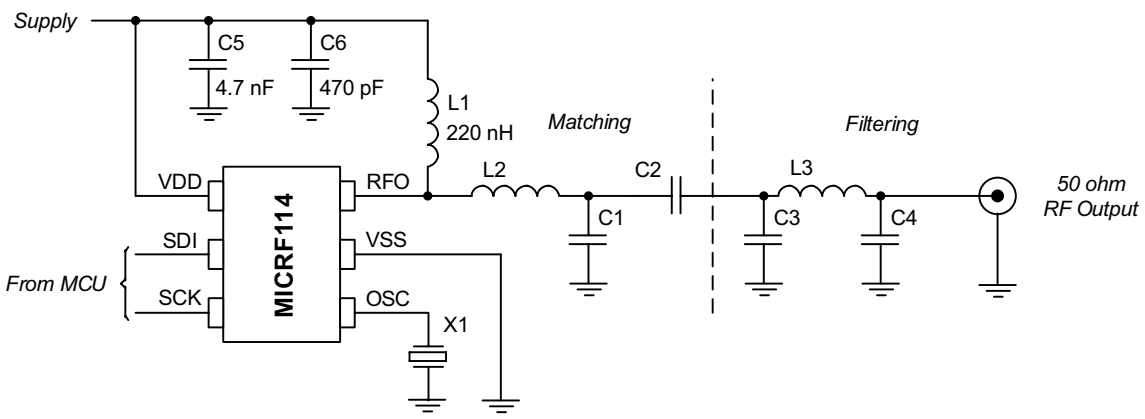
The matching network (L1, L2, C1, and C2) provides optimum power transfer from the MICRF114 to the antenna. The filter stage (L3, C3, and C4) removes the unwanted harmonics. The required harmonic suppression depends on the operating frequency, antenna characteristics, and regional regulations. This means the order of the filter (the number of components) may be different in an actual application with an integrated antenna.

Table 4-1 shows the values of the frequency-dependent components for the two most popular frequencies. Except for L1, it is recommended to use 0402 SMD components in the matching and filter network.

TABLE 4-1: COMPONENT VALUES

Component	Frequency	
	315 MHz	433 MHz
X1	9.84375 MHz	13.56 MHz
L2	39 nH	22 nH
C1	9.1 pF	6.8 pF
C2	9.1 pF	5.6 pF
C3	12 pF	8.2 pF
L3	27 nH	18 nH
C4	12 pF	8.2 pF

FIGURE 4-1: SCHEMATIC DIAGRAM



Note: This is a suggested schematic diagram only. Component values for C1 to C4 and L2 to L3 vary according to operating frequency, antenna characteristics, and regional regulations. Certain components can be removed.

4.2 Measurement Results

The important parameters for regulatory standard compliance are measured on PICtail™ boards for the two most popular operating frequencies using the frequency-dependent components listed in Table 4-1. The MICRF114 operates in CW mode. Harmonics and spurs are measured at +10 dBm output power setting. Matching network, cable, and connector losses are not compensated to ensure that the actual power readings on the spectrum analyzer are slightly less.

Measurement results are shown in Figure 4-2 through Figure 4-7. Note that the regulations limit the radiated field strength at a given distance. The maximum usable power setting at a given frequency and geographic region can be determined only if the antenna gain is known. The level of the fundamental carrier signal and all possible out-of-band signals – harmonics, spurs, and integrated phase noise – must be taken into account. The filter network can be simplified at low-radiated power.

FIGURE 4-2: HARMONIC LEVELS AT 315 MHZ

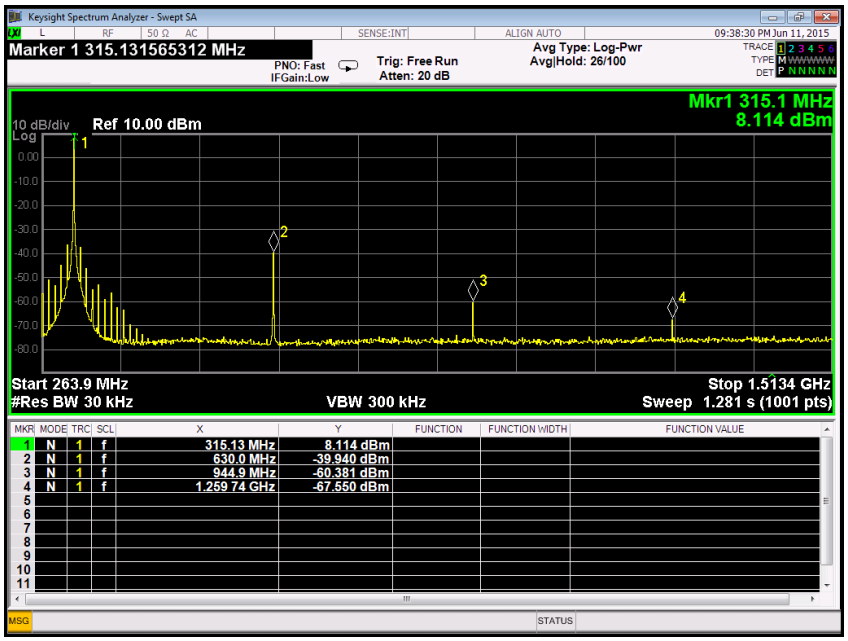


FIGURE 4-3: SPURIOUS LEVELS AT 315 MHZ

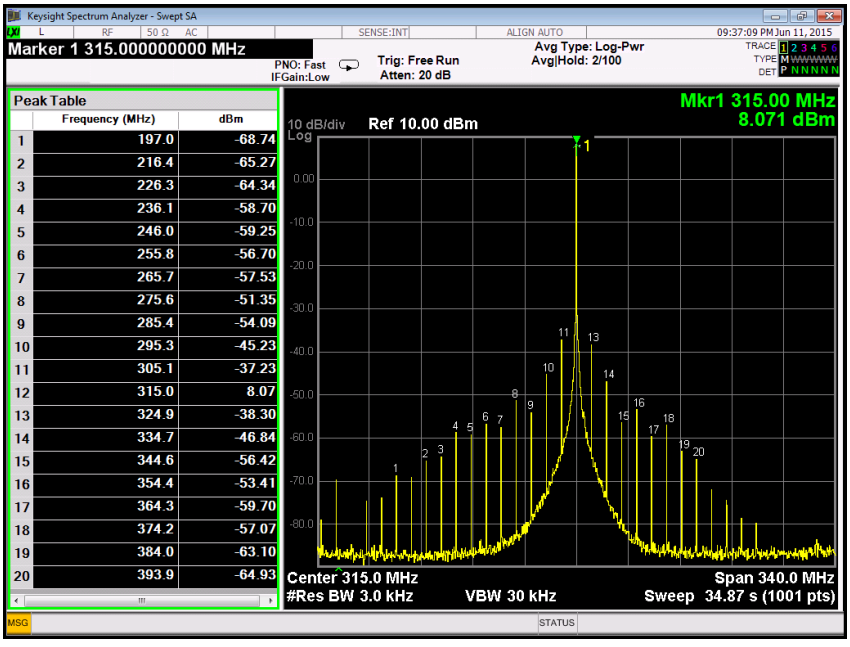


FIGURE 4-4: PHASE NOISE AT 315 MHZ

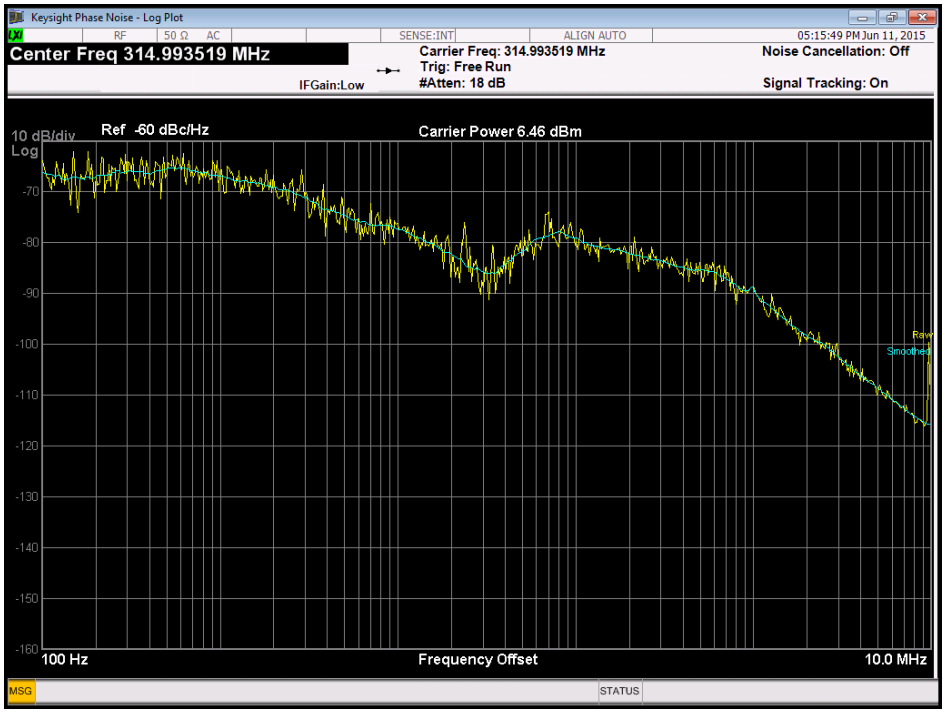


FIGURE 4-5: HARMONIC LEVELS AT 433 MHZ

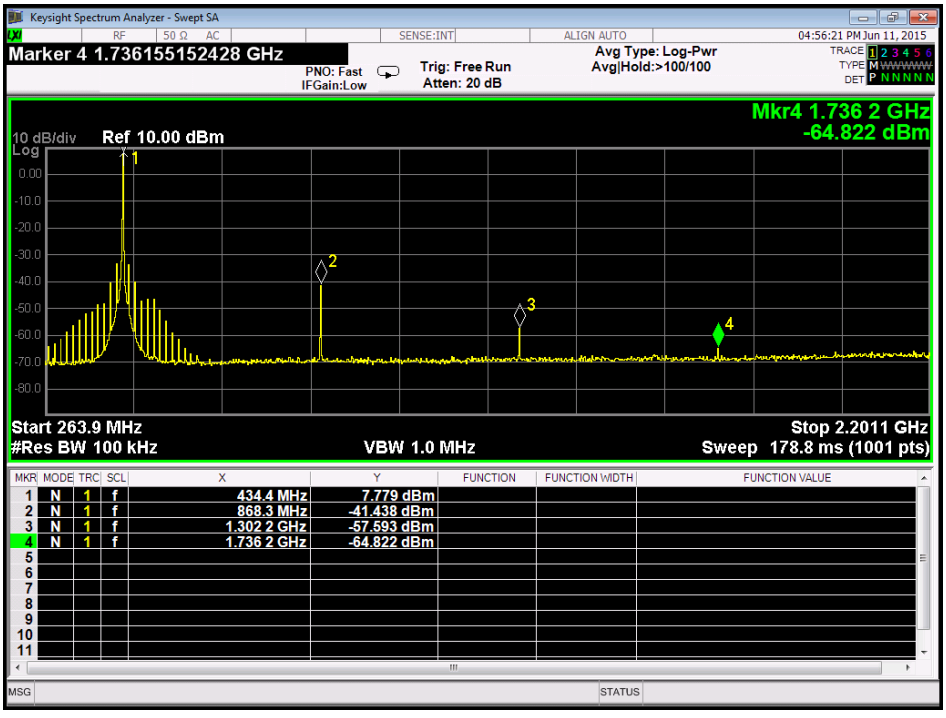


FIGURE 4-6: SPURIOUS LEVELS AT 433 MHZ

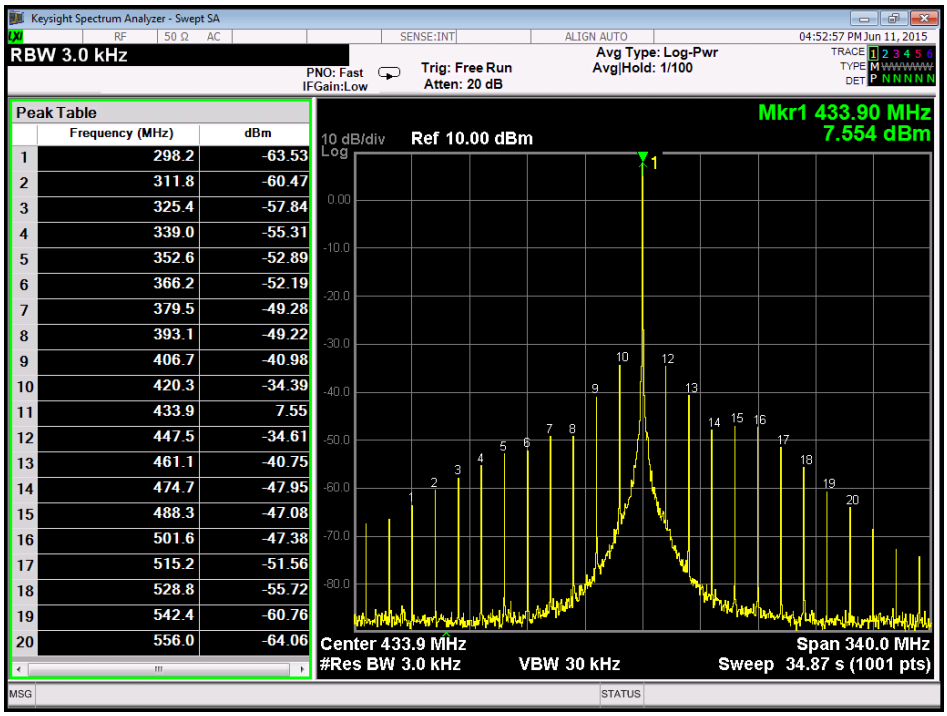
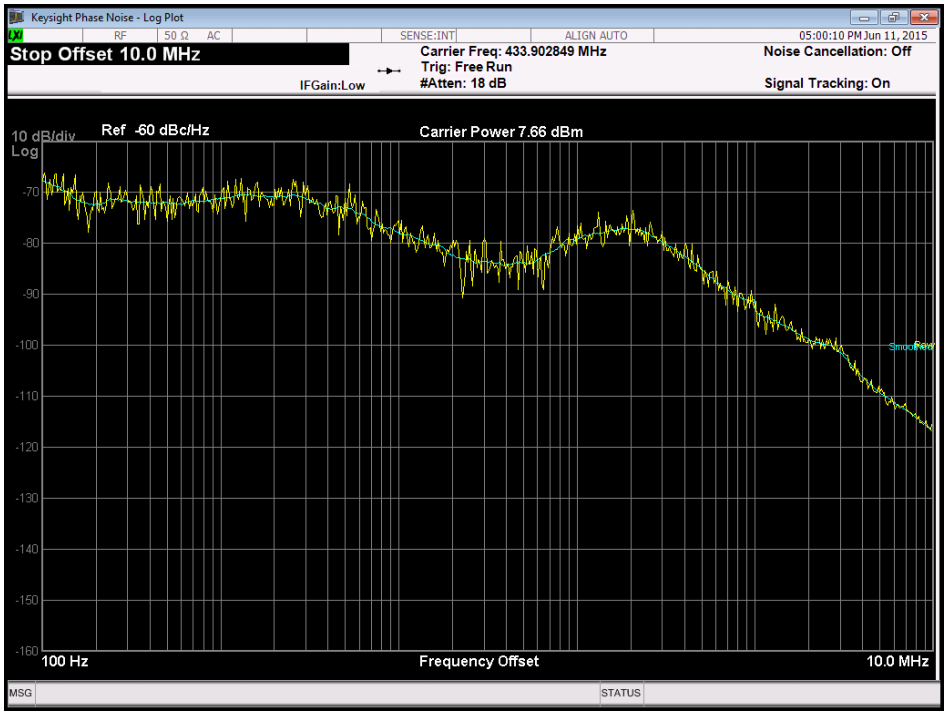


FIGURE 4-7: PHASE NOISE AT 433 MHZ



5.0 ELECTRICAL CHARACTERISTICS

In Table 5-1 and Table 5-2, all voltages are referenced to the potential on the VSS pin.

TABLE 5-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
V_{DD}	Supply Voltage	-0.3	—	4.0	V	On VDD pin
V_{IN}	Voltage on any pin	-0.3	—	V_{DD}+0.3	V	Except VDD and RFO pins
V_{RF}	Voltage on RFO pin	-0.3	—	9	V	RF peak values
V_{ESD}	Electrostatic Discharge	—	—	2000	V	Any pin combinations, HBM
I_{IN}	Current into any pin	-25	—	25	mA	—
T_{ST}	Storage Temperature	-55	—	+125	°C	—
T_{LD}	Lead Temperature	—	—	+260	°C	Soldering, for max 10s

TABLE 5-2: RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
V_{DD}	Supply Voltage	1.8	2.7	3.6	V	On VDD pin
V_{IN}	Voltage on any pin	0.0	—	V_{DD}	V	Except VDD and RFO pins
V_{RF}	Voltage on RFO pin	0.2	—	7.2	V	RF peak values
T_{OP}	Operating Temperature	-40	+27	+85	°C	Ambient

Typical parameter values in Table 5-3 through Table 5-6 are valid at typical V_{DD} and T_{OP} except where indicated otherwise.

TABLE 5-3: DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
I_{DD}	Supply Current	—	0.2	—	µA	Sleep mode
		—	11.7	—	mA	Transmit mode(1)
V_{TP}	POR Level Threshold	—	1.2	—	V	V_{DD} < V_{TP} needed for POR
V_{TG}	POR Glitch Threshold	—	0.8	—	V	Larger glitch generates POR
V_{IL}	Digital in Low Level	—	—	0.35 x V_{DD}	V	—
V_{IH}	Digital in High Level	0.65 x V_{DD}	—	—	V	—
R_{PD}	Input Pull Down	—	134	—	kΩ	On SCK pin

Note 1: OOK transmission with +10 dBm power and 50% duty cycle.

TABLE 5-4: AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
f_{TX}	Transmit Frequency	285	—	445	MHz	32 times the crystal frequency
C_{TX}	Output Capacitance	0	—	3	pF	Selectable with 0.2 pF steps
P_{TX}	Output Power	—	+13	—	dBm	Maximum setting(1)
		-2	—	+13	dBm	Typical control range
		—	1	—	dB	Power control step
P_{SP}	Spurious Emission	—	—	-45	dBc	Excluding harmonics
L_{OUT}	Phase Noise	—	—	-76	dBc/Hz	100 kHz from carrier
		—	—	-92	dBc/Hz	1 MHz from carrier
Z_{OUT}	RF Output Impedance(2)	—	7.5-j50.9	—	Ω	At 315 MHz
		—	6.0-j32.2	—	Ω	At 433 MHz
DR	Modulation Data Rate	0	—	115.2	kbps	NRZ
		0	—	57.6	kbps	Manchester encoded
h_{MOD}	Modulation Depth	—	60	—	dB	—
SR_{VDD}	V_{DD} Slew Rate	0.1	—	—	V/ms	For proper POR operation
C_{XT}	Crystal Load Capacitor	7	—	22.5	pF	Selectable with 0.5 pF steps
R_{XT}	Crystal Loss Resistance	—	—	80	Ω	—

Note 1: Valid with optimum matching circuit at T_{OP} = 27°C and V_{DD} = 2.7V to 3.3V

2: The RF output impedance varies with the operating frequency, the output power setting P_{TX} (which is not necessarily equal to the actual output power) and the output tuning capacitance setting C_{TX}. The values given: P_{TX} = +10 dBm and C_{TX} = 0 pF.

TABLE 5-5: TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
t_{DP}	POR Delay Time	—	—	20	ms	—
t_{WK}	Wake-up Time	—	—	3	ms	Without calibration
t_{CL}	Calibration Time	—	—	2	ms	—

TABLE 5-6: MCU INTERFACE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Notes
t_{CHI}	Clock High Time	30	—	—	ns	$V_{SCK} > V_{IH}$ (1)
t_{CLO}	Clock Low Time	30	—	—	ns	$V_{SCK} < V_{IL}$ (1)
t_{CS}	Clock Setup Time	15	—	—	ns	Before and after start or stop edge
t_{CH}	Clock Hold Time	15	—	—	ns	
t_{DHI}	Data High Time	100	—	—	ns	Between stop and start edges
t_{DS}	Data Setup Time	15	—	—	ns	—
t_{DH}	Data Hold Time	15	—	—	ns	—
t_{FI}	Input Signal Fall Time	—	—	500	ns	Between V_{IL} and V_{IH}
t_{RI}	Input Signal Rise Time	—	—	500	ns	

Note 1: For the definition of V_{IL} and V_{IH} see Table 5-3.

FIGURE 5-1: MCU INTERFACE TIMING