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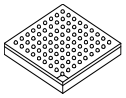
NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMX8MDQLQCEC
Rev. 0.1, 05/2018

MIMX8MQ7DVAJZAA **MIMX8MQ6DVAJZAA**
MIMX8MD7DVAJZAA **MIMX8MD6DVAJZAA**
MIMX8MQ5DVAJZAA

i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products



Package Information
Plastic Package
FBGA 17 x 17 mm, 0.65 mm pitch

Ordering Information
See Table 2 on page 6

1 i.MX 8M Dual / 8M QuadLite / 8M Quad introduction

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors represent NXP's latest market of connected streaming audio/video devices, scanning/imaging devices, and various devices requiring high-performance, low-power processors.

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors feature advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M4 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors. The i.MX 8M Quad and i.MX 8M Dual processors have hardware acceleration for video playback up to 4K, and can drive the video outputs up to 60 fps. Although the i.MX 8M QuadLite processor does not have hardware acceleration for video decode, it allows for video playback with software decoders if needed.

Table 1. Features

Subsystem	Feature
Arm Cortex-A53 MPCore platform	Quad symmetric Cortex-A53 processors: • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Support L1 cache RAMs protection with parity/ECC
	Support of 64-bit Armv8-A architecture: • 1 MB unified L2 cache • Support L2 cache RAMs protection with ECC • Frequency of 1.5 GHz
Arm Cortex-M4 core platform	16 KB L1 Instruction Cache
	16 KB L1 Data Cache
	256 KB tightly coupled memory (TCM)
Connectivity	Two PCI Express Gen2 interfaces
	Two USB 3.0/2.0 controllers with integrated PHY interfaces
	Two Ultra Secure Digital Host Controller (uSDHC) interfaces
	One Gigabit Ethernet controller with support for EEE, Ethernet AVB, and IEEE 1588
	Four Universal Asynchronous Receiver/Transmitter (UART) modules
	Four I^2C modules
	Three SPI modules
External memory interface	32/16-bit DRAM interface: LPDDR4-3200, DDR4-2400, DDR3L-1600
	8-bit NAND-Flash
	eMMC 5.0 Flash
	SPI NOR Flash
	QuadSPI Flash with support for XIP
GPIO and pin multiplexing	GPIO modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
On-chip memory	Boot ROM (128 KB)
	On-chip RAM (128 KB + 32 KB)
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management

Table 1. Features (continued)

Subsystem	Feature
Multimedia	Video Processing Unit: • 4Kp60 HEVC/H.265 main, and main 10 decoder • 4Kp60 VP9 decoder • 4Kp30 AVC/H.264 decoder • 1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 decoder
	Graphic Processing Unit: • 4 shader • 267 million triangles/sec • 1.6 Giga pixel/sec • 32 GFLOPs 32-bit or 64 GFLOPs 16-bit • Support OpenGL ES 1.1, 2.0, 3.0, 3.1, Open CL 1.2, and Vulkan
	HDMI Display Interface: • HDMI 2.0a supporting one display: resolution up to 4096 x 2160 at 60 Hz, support HDCP 2.2 and HDCP 1.4[1] • 20+ Audio interfaces 32-bit @ 384 kHz fs, with Time Division Multiplexing (TDM) support • S/PDIF input and output • Audio Return Channel (ARC) on HDMI • Upscale HD graphics to 4K for display • Downscale 4K video to HD for display • Display Port • Embedded Display Port
	MIPI-DSI Display Interface: • MIPI-DSI 4 channels supporting one display, resolution up to 1920 x 1080 at 60 Hz • LCDIF display controller • Output can be LCDIF output or DC display controller output
	Audio: • S/PDIF input and output • Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces, including one SAI with 16 Tx and 16 Rx channels, one SAI with 8 Tx and 8 Rx channels, and three SAI with 2 Tx and 2 Rx channels • One SAI for 8 Tx channels for HDMI output audio • One S/PDIF input for HDMI ARC input
	Camera inputs: • Two MIPI-CSI2 camera inputs (4-lane each)
Security	Resource Domain Controller (RDC) supports four domains and up to eight regions
	Arm TrustZone (TZ) architecture
	On-chip RAM (OCRAM) secure region protection using OCRAM controller
	High Assurance Boot (HAB)
	Cryptographic acceleration and assurance (CAAM) module
	Secure non-volatile storage (SNVS): Secure real-time clock (RTC)
	Secure JTAG controller (SJC)

Table 1. Features (continued)

Subsystem	Feature
System debug	Arm CoreSight debug and trace architecture
	TPIU to support off-chip real-time trace
	ETF with 4 KB internal storage to provide trace buffering
	Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
	Cross Triggering Interface (CTI)
	Support for 5-pin (JTAG) debug interface

[1] Please contact the NXP sales and marketing team for order details on HDCP enable parts.

NOTE

The actual feature set depends on the part numbers as described in Table 2. Functions such as display and camera interfaces, and connectivity interfaces, may not be enabled for specific part numbers.

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Dual / 8M QuadLite / 8M Quad processor system.

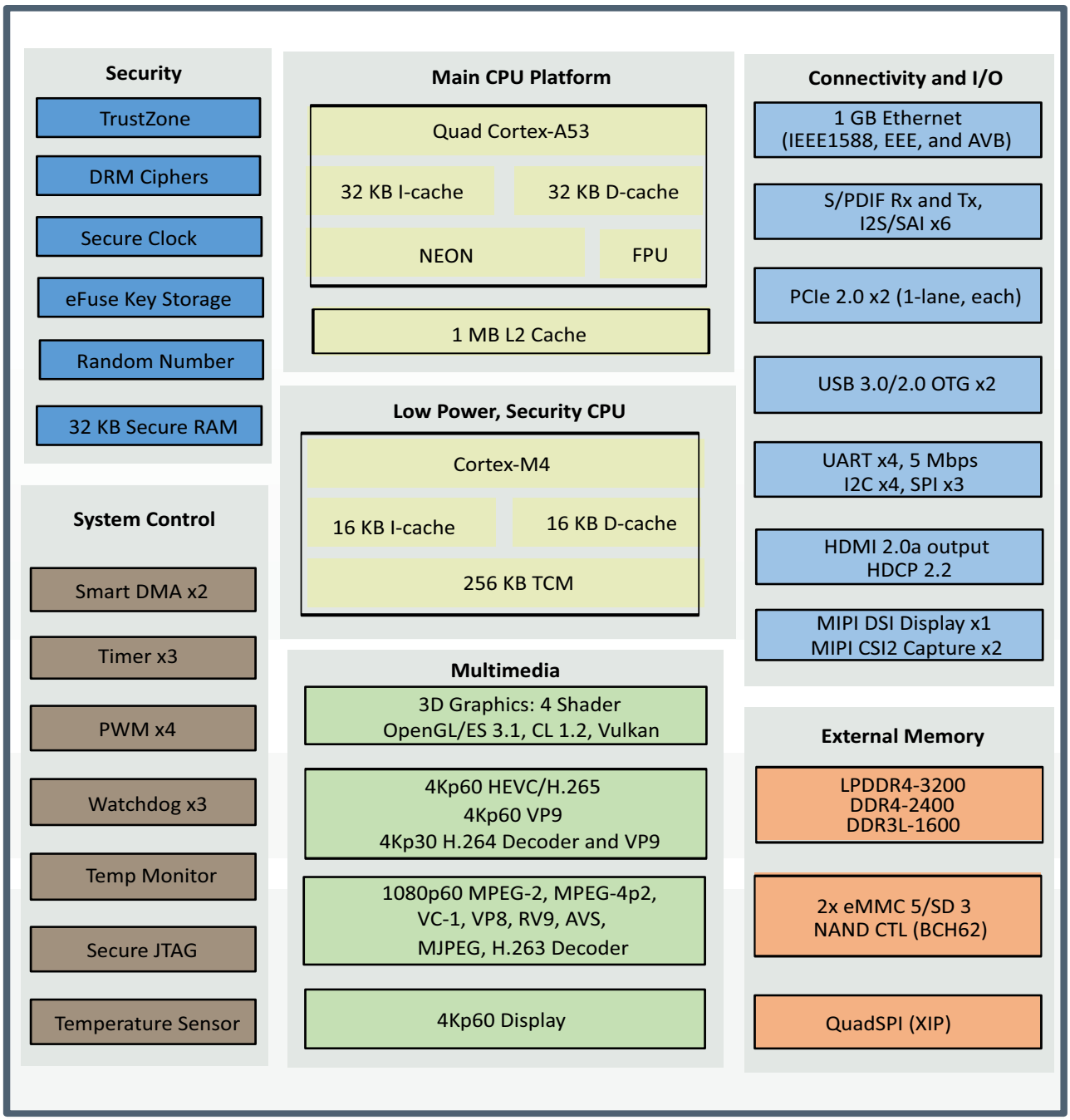


Figure 1. i.MX 8M Dual / 8M QuadLite / 8M Quad system block diagram

1.2 Ordering information

Table 2 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

Table 2. Orderable part numbers

Part number[1]	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature T_j (°C)	Package
MIMX8MQ7DVAJZAA	8M Quad	1.5 GHz	Consumer	0 to +95	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ6DVAJZAA	8M Quad	1.5 GHz	Consumer	0 to +95	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD7DVAJZAA	8M Dual	1.5 GHz	Consumer	0 to +95	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD6DVAJZAA	8M Dual	1.5 GHz	Consumer	0 to +95	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ5DVAJZAA	8M Quad Lite	1.5 GHz	Consumer	0 to +95	17 x 17 mm, 0.65 mm pitch, FBGA

1 Part number requires a Dolby Vision™ license from Dolby.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.

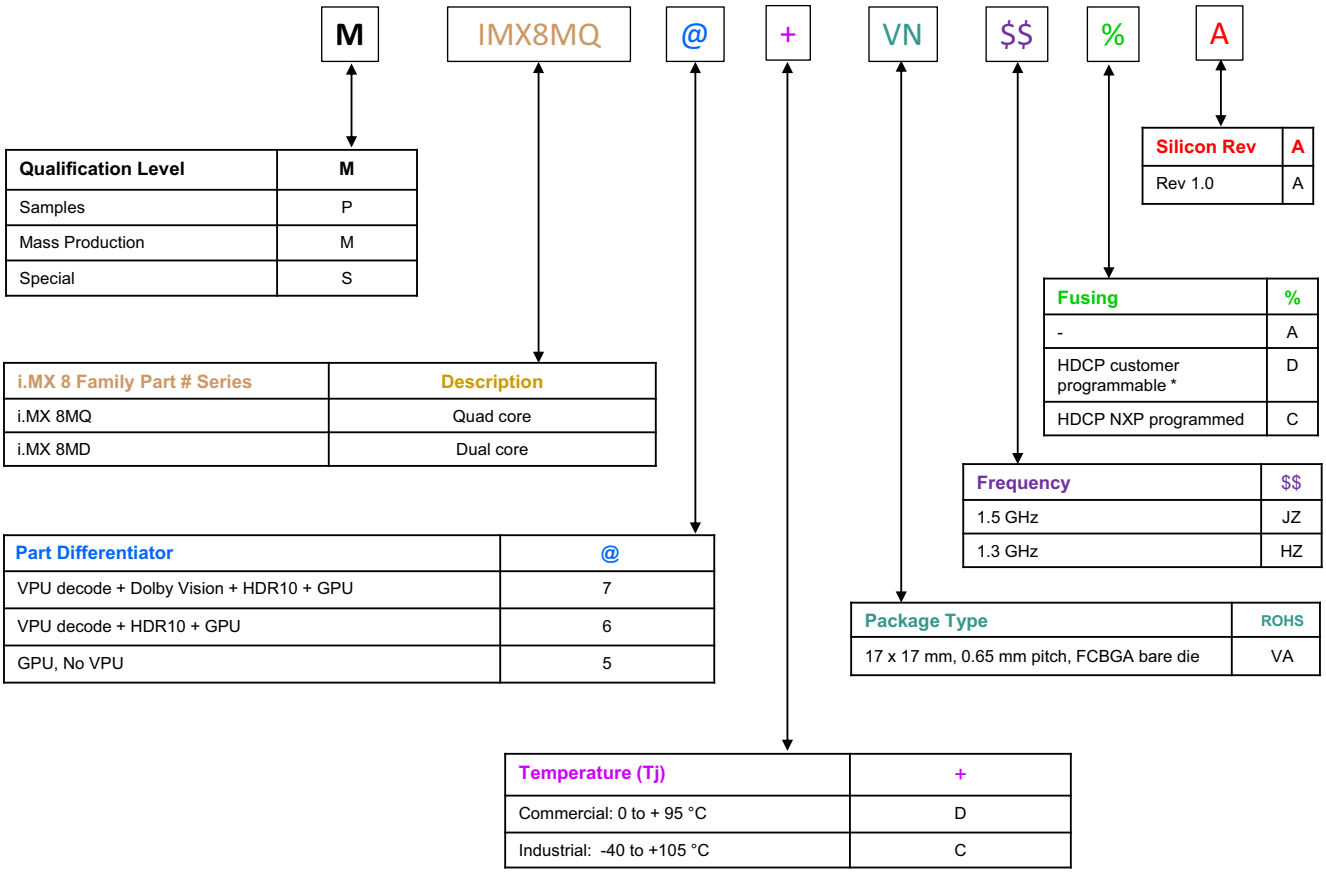


Figure 2. Part number nomenclature—i.MX 8M Dual / 8M QuadLite / 8M Quad processors

*Please contact the NXP sales and marketing team for order details on HDCP enable parts.

2 Modules list

The i.MX 8M Dual / 8M QuadLite / 8M Quad of processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M4 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M4 core is used as a customer microcontroller.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Dual / 8M QuadLite / 8M Quad processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Dual / 8M QuadLite / 8M Quad platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DC	Display Controller	Dual display controller
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 32/16-bit LPDDR4-3200, DDR4-2400, and DDR3L-1600 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
EIM	NOR-Flash / PSRAM interface	The EIM NOR-FLASH / PSRAM provides: • Support for 16-bit (in Muxed I/O mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support for 16-bit (in muxed and non muxed I/O modes) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1	Ethernet Controller	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for details.
GIC	Generic Interrupt Controller	The GIC handles all interrupts from the various subsystems and is ready for virtualization.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit-3D	The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays.
HDMI Tx	HDMI Tx interface	The HDMI module provides an HDMI standard interface port to an HDMI 2.0a-compliant display.
I2C1 I2C2 I2C3 I2C4	I^2C Interface	I^2C provides serial interface for external devices.
IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
MIPI CSI2 (four-lane)	MIPI Camera Serial Interface	This module provides two four-lane MIPI camera serial interfaces, each of them can operate up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (four-lane)	MIPI Display Serial Interface	This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps.
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility.
OCRAM	On-Chip Memory controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. In i.MX 8M Dual / 8M QuadLite / 8M Quad processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
PCIe1 PCIe2	2x PCI Express 2.0	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power Management Unit	Integrated power management unit. Used to provide power to various SoC domains.
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
QSPI	Quad SPI	The Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3 SAI4 SAI5 SAI6	Synchronous Audio Interface	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
SDMA	Smart Direct Memory Access	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	Secure JTAG Controller	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Dual / 8M QuadLite / 8M Quad of processors use JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The SJC of the i.MX 8M Dual / 8M QuadLite / 8M Quad incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, and Master Key Control.
SPDIF1 SPDIF2	Sony Philips Digital Interconnect Format	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
TEMPSENSOR	Temperature Sensor	Temperature sensor
TZASC	Trust-Zone Address Space Controller	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4	UART Interface	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	The i.MX 8M Dual / 8M QuadLite / 8M Quad SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.0. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode. One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface.
USB 3.0/2.0	2x USB 3.0/2.0 controllers and PHYs	Two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains: • USB 3.0 core, which can operate in both 3.0 and 2.0 mode
VPU	Video Processing Unit	A high performing video processing unit (VPU), which covers many SD-level and HD-level video decoders. See the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for a complete list of the VPU's decoding and encoding capabilities.
WDOG1 WDOG2 WDOG3	Watchdog	The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator interface	The XTALOSC module enables connectivity to an external crystal oscillator device.

2.1 Recommended connections for unused interfaces

The recommended connections for unused analog interfaces can be found in the Section, "Unused Input/Output Terminations," in the hardware development guide for the device.

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Dual / 8M QuadLite / 8M Quad processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. i.MX 8M Dual / 8M QuadLite / 8M Quad chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 13
FPBGA package thermal resistance	on page 14
Operating ranges	on page 15
External clock sources	on page 17
Maximum supply currents	on page 18
Power modes	on page 19
USB PHY Suspend current consumption	on page 22

3.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 5 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 5. Absolute maximum ratings

Parameter description	Symbol	Min	Max	Unit	Notes
Core supply voltages	VDD_ARM VDD_SOC	0	1.1	V	1.1 V is for VDD_ARM overdrive
Power supply for GPU	VDD_GPU	0	1.1	V	1.1 V is for overdrive
Power supply for VPU	VDD_VPU	0	1.1	V	Nominal mode
		0	1.1	V	Overdrive mode

Table 5. Absolute maximum ratings (continued)

Parameter description	Symbol	Min	Max	Unit	Notes
GPIO supply voltage	NVCC_JTAG, NVCCGPIO1, NVCC_ENT, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SA1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, NVCC_I2C, NVCC_UART	0	3.6	V	1.8 V mode/3.3 V mode
SNVS IO supply voltage	NVCC_SNVS	0	3.6	V	3.3 V mode only
VDD_SNVS supply voltage	VDD_SNVS	0	0.99	V	—
USB high supply voltage	USB1_VDD33, USB1_VPH, USB2_VDD33, USB2_VPH	0	3.63	V	—
USB_VBUS input detected	USB1_VBUS, USB2_VBUS	0	5.25	V	—
Input voltage on USB*_DP, USB*_DN pins	USB1_DP/USB1_DN USB2_DP/USB2_DN	0	USB1_VDD33 USB2_VDD33	V	—
Input/output voltage range	V_{in}/V_{out}	0	OVDD[1]+0.3	V	—
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V	—
Storage temperature range	$T_{STORAGE}$	–40	150	°C	—

1 OVDD is the I/O supply voltage.

3.1.2 Thermal resistance

3.1.2.1 FPBGA package thermal resistance

Table 6 displays the thermal resistance data.

Table 6. Thermal resistance data

Rating	Test conditions	Symbol	17 x 17 pkg value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	Bare die: 16.4	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	Bare die: 13.9	°C/W °C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	Bare die: 4.6	°C/W
Junction to Case[1,5]	—	$R_{\theta JC}$	Bare die: 0.1	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

3.1.3 Operating ranges

Table 7 provides the operating ranges of the i.MX 8M Dual / 8M QuadLite / 8M Quad processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM).

Table 7. Operating ranges

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power supply for Quad-A53	VDD_ARM	0.81	0.9	1.05	V	Nominal mode—the maximum Arm core frequency supported in this mode is 1000 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum Arm core frequency supported in this mode is defined in Table 2.
Power supply for SoC logic	VDD_SOC	0.81	0.9	0.99	V	—
Power supply for GPU	VDD_GPU	0.81	0.9	1.05	V	Nominal mode—the maximum GPU frequency supported in this mode is 800 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum GPU frequency supported in this mode is 1 GHz.
Power supply for VPU	VDD_VPU	0.81	0.9	1.05	V	Nominal mode—the maximum VPU frequency supported in this mode is 550/500/588 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum VPU G2/G1/AXI Bus frequency supported in this mode is 660/600/800 MHz.
Core voltage	VDD_DRAM	0.81	0.9	1.05	V	Nominal mode—the maximum DRAM working frequency supported in this mode is 933 MHz.
		0.99	1.0	1.05	V	Overdrive mode—the maximum DRAM working frequency supported in this mode is 1600 MHz
Power Supply Analog Domain	VDDA_1P8	1.62	1.8	1.98	V	Power for internal analog blocks—must match the range of voltages that the rechargeable backup battery supports.
PLL 1.8 V supply voltage	VDDA_DRAM	1.71	1.8	1.89	V	—
Backup battery supply range	VDD_SNVS	0.81	0.9	0.99	V	—

Table 7. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
Supply for 25 MHz crystal	VDD_1P8_XTAL_25M	1.6	1.8	1.98	V	—
Supply for 27 MHz crystal	VDD_1P8_XTAL_27M	1.6	1.8	1.98	V	—
Temperature sensor	VDD_1P8_TSENSOR	1.6	1.8	1.98	V	—
USB supply voltages	USB1_VDD33/ USB1_VPH	3.069	3.3	3.63	V	This rail is for USB
	USB2_VDD33/ USB2_VPH	3.069	3.3	3.63	V	This rail is for USB
	USB1/2_DVDD	0.837	0.900	0.990	V	0.9 V supply for USB high speed operation
	USB1/2_VP	0.837	0.900	0.990	V	0.9 V supply for USB super speed operation
	USB1/2_VPTX	0.837	0.900	0.990	V	0.9 V supply for PHY transmit
DDR I/O supply voltage	NVCC_DRAM	1.06	1.10	1.17	V	LPDDR4
		1.14	1.2	1.26	V	DDR4
		1.28	1.35	1.42	V	DDR3L
	DRAM_VREF	0.49 x NVCC_DRAM	0.5 x NVCC_DRAM	0.51 x NVCC_DRAM	V	Set to one-half NVCC_DRAM
GPIO supply voltages	NVCC_JTAG, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SAI1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, NVCC_I2C, NVCC_UART	1.65, 3.0	1.8, 3.3	1.95, 3.6	V	—
	NVCC_ENET	1.65, 2.25 3.0	1.8, 2.5 3.3	1.95, 2.75 3.6	V	—
	NVCC_GPIO1	1.65 3.0	1.8, 3.3	1.95, 3.6	V	Power for GPIO1_IO00 ~ GPIO1_IO15
	NVCC_SNVS	3.0	3.3	3.6	V	Power for 3.3 V only
HDMI supply voltage	HDMI_AVDDCLK	0.850	0.900	0.990	V	0.9 V supply for HDMI high speed clock
	HDMI_AVDDIO	1.700	1.800	1.900	V	1.8 V supply for HDMI bias and PLL
	HDMI_AVDDCORE	0.850	0.900	0.990	V	0.9 V supply for HDMI analog

Table 7. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
MIPI supply voltage	MIPI_VDDA	0.81	0.9/1.0	1.1	V	Analog core power supply
	MIPI_VDDHA	1.62	1.8	1.98	V	Analog IO power supply
	MIPI_VDD	0.81	0.9/1.0	1.1	V	Digital core power supply
	MIPI_VDDPLL	0.81	0.9/1.0	1.1	V	Analog supply for MIPI PLL
Voltage rails supplied from 1.8 V PHY	PCIE_VPH	1.674 3.069	1.8 3.3	1.98 3.63	V	Supplied from PMIC
	PCIE_VP, PCIE_VPTX	0.837	0.9	0.99	V	Supplied from PMIC
Temperature sensor accuracy	T_{delta}	—	±3	—	°C	Typical accuracy over the range –40°C to 125°C
Fuse power	EFUSE_VQPS	1.71	1.8	1.98	V	Power supply for internal use
Junction temperature, consumer	T_J	0	—	+95	°C	See Table 2 for complete list of junction temperature capabilities.

1 Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This result in an optimized power/speed ratio.

3.1.4 External clock sources

A 25 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for CPU, BUS, and high-speed interfaces. For fractional PLLs, the 25 MHz clock from the oscillator can be directly used as the PLL reference clock.

A 27 MHz oscillator is used as the reference clock for HDMI PHY. Also it can be used as the alternative source for the fractional PLLs.

A 32 kHz clock input pin is used as the RTC clock source. It is expected to be supplied by an external 32.768 kHz oscillator. When an external RTC clock input is not present, the 32 kHz clock for internal logic is generated by the 25 MHz oscillator. The frequency of the internal 32 kHz clock will be 31.25 kHz.

Two pairs of differential clock inputs, named as CLK1P and CLK1N, can be used as the reference clock for the PLL. This is mainly used for a high-speed clock input during testing.

Four clock inputs to the CCM from normal GPIO pads via IOMUX can be used as the clock sources in the CCM.

Table 8 shows the interface frequency requirements.

Table 8. External input clock frequency

Parameter description	Symbol	Min	Typ	Max	Unit
RTC[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI_25M/XTALO_25M[2]	f_{xtal}	20	25	40	MHz
XTALI_27M/XTALO_27M[2]	f_{xtal}	20	27	40	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent.

3 Recommended nominal frequency 32.768 kHz.

The typical values shown in Table 8 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC operation, two clock sources are available.The decision of choosing a clock source should be made based on real-time clock use and precision timeout.

3.1.5 Maximum supply currents

Table 9 represents the maximum momentary current transients on power lines and should be used for power supply selection. Maximum currents are higher by far than the average power consumption of typical use cases.

Table 9. Maximum supply currents[1]

Power rail	Max current	Unit
VDD_ARM	384 to 2410[1]	mA
VDD_SOC	1400 to 1870[1]	mA
VDD_GPU	0 to 2040[1]	mA
VDD_VPU	0 to 610[1]	mA
VDD_DRAM	600 to 870[1]	mA
VDDA_0P9	50	mA
VDDA_1P8	20	mA
VDDA_DRAM	30	mA
VDD_SNVS	5	mA
NVCC_SNVS	5	mA
NVCC_<XXX>	I_{max} = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.	
NVCC_DRAM	375 to 750[1]	mA
DRAM_VFEF	10	mA
USB1_DVDD	9.2	mA
USB2_DVDD	9.2	mA
USB1_VP	35.7	mA
USB2_VP	35.7	mA
USB1_VPTX	21.2	mA

Table 9. Maximum supply currents[1] (continued)

Power rail	Max current	Unit
USB2_VPTX	21.2	mA
USB1_VDD33	24.5	mA
USB2_VDD33	24.5	mA
USB1_VPH	20.3	mA
USB2_VPH	20.3	mA
PCIE_VP (PCIE1)	38.1	mA
PCIE_VP (PCIE2)	38.1	mA
PCIE_VPH (PCIE1)	43	mA
PCIE_VPH (PCIE2)	43	mA
PCIE_VPTX (PCIE1)	14.3	mA
PCIE_VPTX (PCIE2)	14.3	mA
HDMI_AVDDCLK	95.89	mA
HDMI_AVDDCORE		
HDMI_AVDDIO	6.551	mA
MIPI_VDDA (DSI)	17.1	mA
MIPI_VDDHA (DSI)	4.2	mA
MIPI_VDD (DSI)	14.4	mA
MIPI_VDDPLL (DSI)	3.8	mA
MIPI_VDDA (CSI1/2)	18.79	mA
MIPI_VDDHA (CSI1/2)	2.97	mA
EFUSE_VQPS	96.35	mA

1 Use case dependent

3.1.6 Power modes

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors support the following power modes:

- RUN Mode: All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- IDLE Mode: When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M4 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.
- Deep Sleep Mode (DSM): The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.

- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 10. Chip power in different LP mode

Mode	Supply	Max.[1]	Unit
SNVS	VDD_SNVS (1.0 V)	1.39	mA
	NVCC_SNVS (3.6 V)	4.25	
	Total[2]	17	mW
Deep Sleep Mode (DSM)	VDD_SOC (1.0 V)	148.50	mA
	VDDA_1P8 (2.0 V)	12.82	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	0.50	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.80	
	NVCC_DRAM (1.17 V)	4.51	
	Total[2]	197	mW
IDLE	VDD_ARM (1.0 V)	152.10	mA
	VDD_SOC (1.0 V)	132.90	
	VDD_DRAM (1.0 V)	44.10	
	VDDA_1P8 (2.0 V)	13.53	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	1.32	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.34	
	NVCC_DRAM (1.17 V)	13.12	
	Total[2]	389	mW
RUN	Total	1 to 4	mW

1 All the power numbers defined in the table are based on typical silicon at 25°C. Use case dependent

2 Sum of the listed supply rails.

Table 11 summarizes the external power supply states in all the power modes.

Table 11. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON

Table 11. The power supply states (continued)

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_GPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_VPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_DRAM	OFF	OFF	OFF	ON	ON
VDDA_0P9	OFF	OFF	ON	ON	ON
VDDA_1P8	OFF	OFF	ON	ON	ON
VDDA_DRAM	OFF	OFF	ON	ON	ON
VDD_SNVS	OFF	ON	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

3.1.7 USB PHY Suspend current consumption

3.1.7.1 Low power Suspend Mode

The VBUS Valid comparators and their associated bandgap circuits are enabled by default. Table 12 shows the USB interface current consumption in Suspend mode with default settings.

Table 12. USB PHY current consumption in Suspend mode[1]

	USB1_VDD33	USB2_VDD33
Current	154 µA	154 µA

1 Low Power Suspend is enabled by setting USBx_PORTSC1 [PHCD]=1 [Clock Disable (PLPSCD)].

3.1.7.2 Power-Down modes

Table 13 shows the USB interface current consumption with only the OTG block powered down.

Table 13. USB PHY current consumption in Sleep mode[1]

	USB1_VDD33	USB2_VD33
Current	520 µA	520 µA

1 VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 14 shows the USB interface current consumption in Power-Down mode.

Table 14. USB PHY current consumption in Power-Down mode[1]

	USB1_VDD33	USB2_VDD33
Current	146 µA	146 µA

1 The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

3.1.8 PCIe PHY 2.1 DC electrical characteristics

Table 15. PCIe recommended operating conditions

Parameter	Description		Min	Max	Unit
PCIE_VP	Low Power Supply Voltage for PHY Core	—	0.837	0.99	V
PCIE_VPTX	PHY transmit supply	—	0.837	0.99	
PCIE_VPH	High Power Supply Voltage for PHY Core	1.8	1.674	1.98	
		3.3	3.069	3.63	

Table 15. PCIe recommended operating conditions (continued)

Parameter	Description	Min	Max	Unit
T_A	Commercial Temperature Range	0	70	°C
T_J	Simulation Junction Temperature Range	-40	125	°C

Note: V_{DD} should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core (1.0 V nominal value or 1.1 V overdrive DC value).
The power supply voltage variation for the PHY core should have less than ±5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

Table 16. PCIe DC electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
PCIE1_VP, PCIE2_VP	Power Supply Voltage		0.9 - 7%	0.9	0.9 + 10%	V
PD	Power Consumption	Normal	—	40	—	mW
		Partial Mode	—	27	—	mW
		Slumber Mode	—	7	—	mW
		Full Powerdown	—	0.2	—	mW

Table 17. PCIe PHY high-speed characteristics

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
Unit Interval	UI	2.5 Gbps	—	400	—	ps
		5.0 Gbps	—	200	—	
TX Serial output rise time (20% to 80%)	T_{TXRISE}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial output fall time (80% to 20%)	T_{TXFALL}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial data output voltage (Differential, pk–pk)	ΔV_{TX}	2.5 Gbps	800	—	1100	mVp–p
		5.0 Gbps	600	—	900	
PCIe Tx deterministic jitter < 1.5 MHz	TRJ	2.5 Gbps	3	—	—	ps, rms
		5.0 Gbps	3	—	—	
PCIe Tx deterministic jitter > 1.5 MHz	TDJ	2.5 Gbps	—	—	20	ps, pk–pk
		5.0 Gbps	—	—	10	

Table 17. PCIe PHY high-speed characteristics (continued)

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
RX Serial data input voltage (Differential pk–pk)	ΔV_{RX}	2.5 Gbps	120	—	1200	mVp–p
		5.0 Gbps	120	—	1200	

Table 18. PCIe PHY reference clock timing requirements (vp is PIE_VP, 0.9 V power supply)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
FREF_OFFSET	Reference clock frequency offset	-300	—	30	ppm	—
DJREF_CLK	Reference clock cycle to cycle jitter	—	—	35	ps	DJ across all frequencies
DCREF_CLK	Duty cycle	40	—	60	%	—
VCMREF_CLK	Common mode input level	0	—	vp	V	Differential inputs
VDREF_CLK	Differential input swing	-0.3	—	—	V_{PP}	Differential inputs
VOLREF_CLK	Single-ended input logic low	-0.3	—	-0.3	V	If single-ended input is used.
VOHREF_CLK	Single-ended input logic high	vp - 0.3	—	vp + 0.3	V	If single-ended input is used.
SWREF_CLK	Input edge rate	—	—	—	V/ns	—
REF_CLK_SKEW	Reference clock skew (±)	—	—	200	ps	—

PCIe PHY interface is compliant with PCIe Express GEN2.

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

3.2.1 Power-up sequence

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors have the following power-up sequence requirements:

- Turn on NVCC_SNVS
- Turn on VDD_SNVS
- RTC_RESET_B release
- Turn on VDD_SOC and VDDA_0P9

- Turn on VDD_ARM, VDD_GPU, VDD_VPU, and VDD_DRAM (no sequence between these four rails)
- Turn on VDDA_1P8_XXX, VDDA_DRAM (no sequence between these rails)
- Turn on NVCC_XXX and NVCC_DRAM (no sequence between these rails)
- POR_B release (it should be asserted during the entire power up sequence)

If the GPU/VPU is not used during the ROM boot sequence, VDD_GPU/VDD_VPU can stay off to reduce the power during boot, and then turned on by software afterwards.

During the chip power up, the power of the PCIe PHY, USB PHY, HDMI PHY, and MIPI PHY could stay off. After chip power up, the power of these PHys should be turned on. If any of the PHY power are turned on during the power up sequence, the POR_B can be released after the PHY power is stable.

3.2.2 Power-down sequence

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors have the following power-down sequence requirements:

- Turn off NVCC_SNVS and VDD_SNVS last
- Turn off VDD_SOC after the other power rails or at the same time as other rails
- No sequence for other power rails during power down

3.2.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about the I/O power supply of each pin, see “Power Rail” columns in the pin list tables of Section 5, “Package information and contact assignments.”

Table 19 lists the modules in each power domain.

Table 19. The modules in the power domains

Power Domain	Modules in the domain
VDD_ARM	Arm A53
VDD_GPU	GC7000L GPU
VDD_VPU	G1 and G2 VPU
VDD_DRAM	DRAM controller and PHY
VDD_SNVS	SNVS_LP
VDD_SOC	All the other modules