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NXP Semiconductors

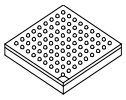
Data Sheet: Technical Data

Document Number: IMXRT1050CEC
Rev. 1, 03/2018

MIMXRT1051DVL6A
MIMXRT1051DVL6B

MIMXRT1052DVL6A
MIMXRT1052DVL6B

i.MX RT1050 Crossover Processors for Consumer Products



Package Information
Plastic Package
196-pin MAPBGA, 10 x 10 mm, 0.65 mm pitch

Ordering Information
See Table 1 on page 5

1 i.MX RT1050 introduction

The i.MX RT1050 is a new processor family featuring NXP's advanced implementation of the Arm Cortex®-M7 core, which operates at speeds up to 600 MHz to provide high CPU performance and best real-time response.

The i.MX RT1050 processor has 512 KB on-chip RAM, which can be flexibly configured as TCM or general-purpose on-chip RAM. The i.MX RT1050 integrates advanced power management module with DCDC and LDO that reduces complexity of external power supply and simplifies power sequencing. The i.MX RT1050 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX RT1050 also has rich audio and video features, including LCD display, basic 2D graphics, camera interface, SPDIF, and I2S audio interface.

The i.MX RT1050 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1050 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
  - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 600 MHz
- Cortex M7 CoreSight™ components integration for debug
- Frequency of the core, as per Table 9, "Operating ranges," on page 19.

The SoC-level memory system consists of the following additional components:

  - Boot ROM (96 KB)
  - On-chip RAM (512 KB)
    - Configurable RAM size up to 512 KB shared with M7 TCM
- External memory interfaces:
  - 8/16-bit SDRAM, up to SDRAM-166
  - 8/16-bit SLC NAND FLASH, with ECC handled in software
  - SD/eMMC
  - SPI NOR FLASH
  - Parallel NOR FLASH with XIP support
  - Single/Dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
  - Two General Programmable Timers (GPT)
    - 4-channel generic 32-bit resolution timer
    - Each support standard capture and compare operation
  - Four Periodical Interrupt Timer (PIT)
    - Generic 16-bit resolution timer
    - Periodical interrupt generation
  - Four Quad Timers (QTimer)

  - 4-channel generic 16-bit resolution timer for each
  - Each support standard capture and compare operation
  - Quadrature decoder integrated
- Four FlexPWMs
  - Up to 8 individual PWM channels for each
  - 16-bit resolution PWM suitable for Motor Control applications
- Four Quadrature Encoder/Decoders

Each i.MX RT1050 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
  - Parallel RGB LCD interface
    - Support 8/16/24 bit interface
    - Support up to 1366 x 768 WXGA resolution
    - Support Index color with 256 entry x 24 bit color LUT
    - Smart LCD display with 8/16-bit MPU/8080 interface
- Audio:
  - S/PDIF input and output
  - Three synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
  - MQS interface for medium quality audio via GPIO pads
- Generic 2D graphics engine:
  - BitBlit
  - Flexible image composition options—alpha, chroma key
  - Image rotation (90˚, 180˚, 270˚)
  - Porter-Daff operation
  - Image size
  - Color space conversion
  - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
  - Standard 2D-DMA operation
- Camera sensors:
  - Support 24-bit, 16-bit, and 8-bit CSI input
- Connectivity:
  - Two USB 2.0 OTG controllers with integrated PHY interfaces
  - Two Ultra Secure Digital Host Controller (uSDHC) interfaces
    - MMC 4.5 compliance with HS200 support up to 200 MB/sec
    - SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec
    - Support for SDXC (extended capacity)

  - One 10/100 M Ethernet controller with support for IEEE1588
  - Eight universal asynchronous receiver/transmitter (UARTs) modules
  - Four I2C modules
  - Four SPI modules
  - Two FlexCAN modules
- GPIO and Pin Multiplexing:
  - General-purpose input/output (GPIO) modules with interrupt capability
  - Input/output multiplexing controller (IOMUXC) to provide centralized pad control
  - Two FlexIOs

The i.MX RT1050 processors integrate advanced power management unit and controllers:

- Full PMIC integration. On-chip DCDC and LDO
- Temperature sensor with programmable trip points
- GPC hardware power management controller

The i.MX RT1050 processors support the following system debug:

- Arm CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Support for 5-pin (JTAG) and SWD debug interfaces selected by eFuse

Security functions are enabled and accelerated by the following hardware:

- High Assurance Boot (HAB)
- Data Co-Processor (DCP):
  - AES-128, ECB, and CBC mode
  - SHA-1 and SHA-256
  - CRC-32
- Bus Encryption Engine (BEE)
  - AES-128, ECB, and CTR mode
  - On-the-fly QSPI Flash decryption
- True random number generation (TRNG)
- Secure Non-Volatile Storage (SNVS)
  - Secure real-time clock (RTC)
  - Zero Master Key (ZMK)
- Secure JTAG Controller (SJC)

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

1.2 Ordering information

Table 1 provides examples of orderable part numbers covered by this Data Sheet.

Table 1. Ordering information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MIMXRT1051DVL6A MIMXRT1051DVL6B	Features supports: • 600 MHz, commercial grade for general purpose • No LCD/CSI/PXP • CAN x2 • Ethernet • eMMC 4.5/SD 3.0 x2 • USB OTG x2 • UART x8 • SAI x3 • Timer x4 • PWM x4 • I^2C x4 • SPI x4	10 x 10 mm, 0.65 pitch, 196 MAPBGA	0 to +95
MIMXRT1052DVL6A MIMXRT1052DVL6B	Features supports: • 600 MHz, commercial grade for general purpose • With LCD/CSI/PXP • CAN x2 • Ethernet • eMMC 4.5/SD 3.0 x2 • USB OTG x2 • UART x8 • SAI x3 • Timer x4 • PWM x4 • I^2C x4 • SPI x4	10 x 10 mm, 0.65 pitch, 196 MAPBGA	0 to +95

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX RT1050 Crossover Processors for Consumer Products data sheet (IMXRT1050CEC) covers parts listed with a “D (Consumer temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/imxrtseries or contact an NXP representative for details.

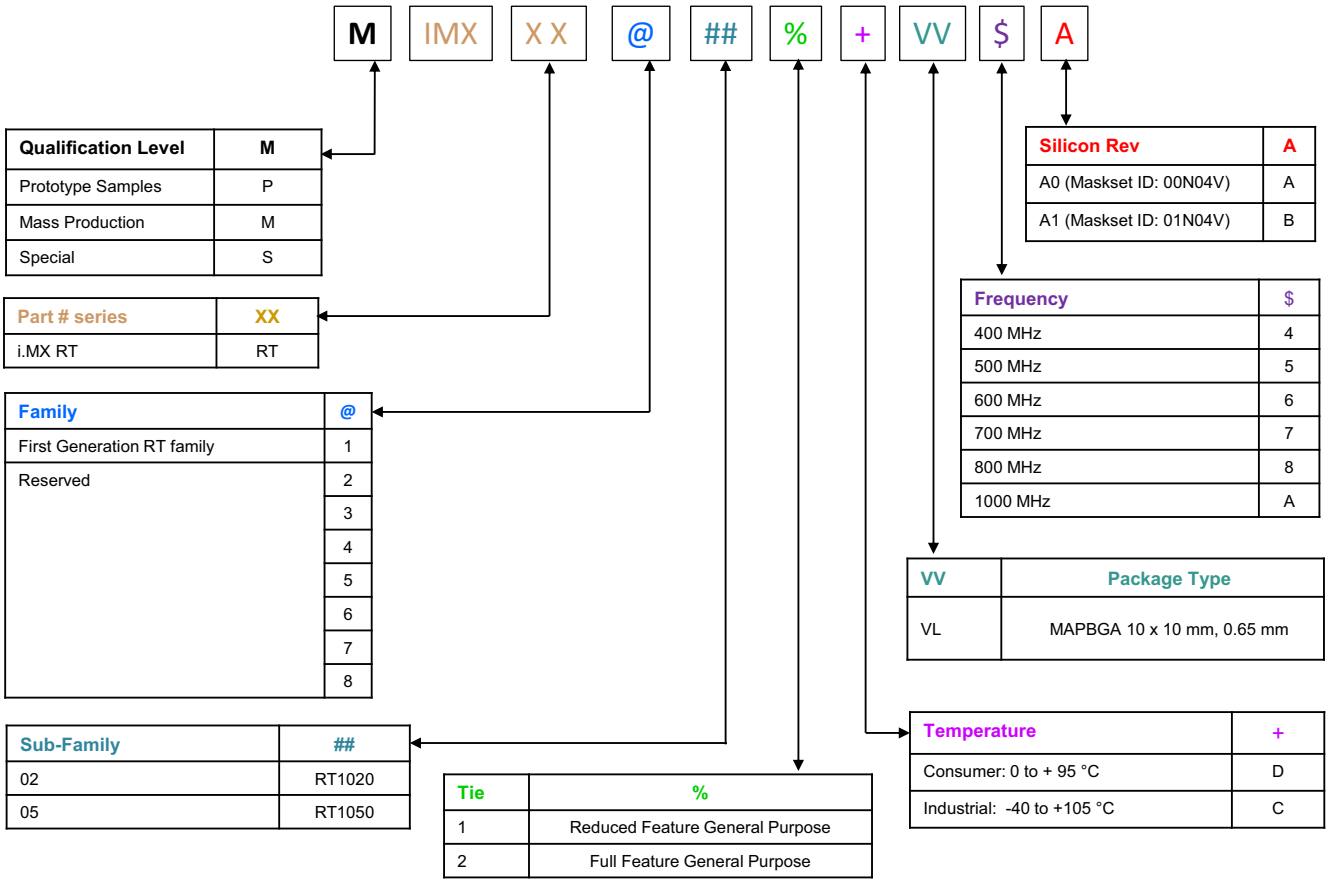


Figure 1. Part number nomenclature—i.MX RT1050

2 Architectural overview

The following subsections provide an architectural overview of the i.MX RT1050 processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX RT1050 processor system[1].

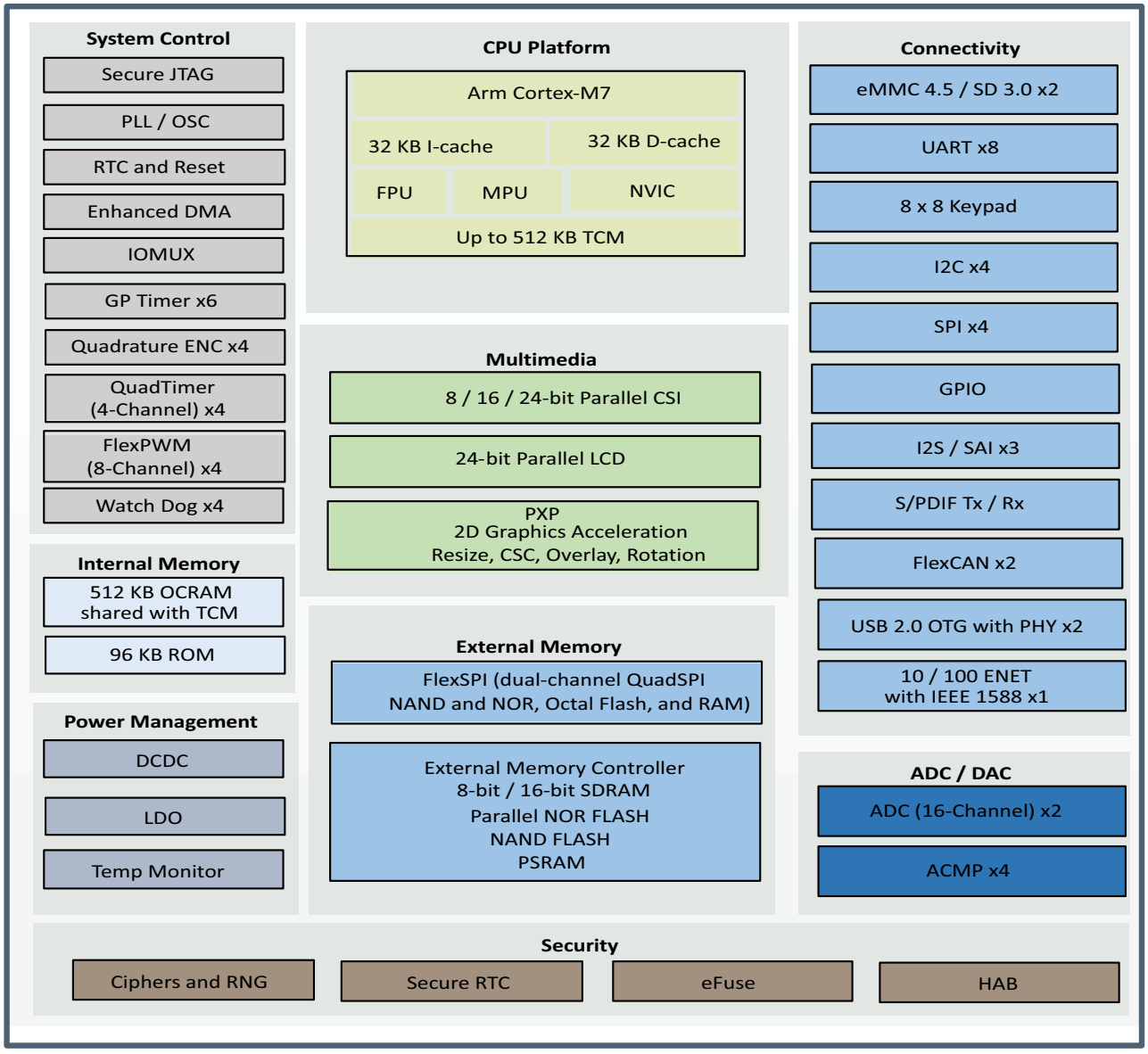


Figure 2. i.MX RT1050 system block diagram

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 1 for details.

3 Modules list

The i.MX RT1050 processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX RT1050 modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ACMP1 ACMP2 ACMP3 ACMP4	Analog Comparator	Analog	The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).
ADC1 ADC2	Analog to Digital Converter	Analog	The ADC is a 12-bit general purpose analog to digital converter.
AOI	And-Or-Inverter	Cross Trigger	The AOI provides a universal boolean function generator using a four team sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).
Arm	Arm Platform	Arm	The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules.
BEE	Bus Encryption Engine	Security	On-The-Fly FlexSPI Flash Decryption
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX RT1050 platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DCDC	DCDC Converter	Analog	The DCDC module is used for generating power supply for core logic. Main features are: • Adjustable high efficiency regulator • Supports 3.0 V input voltage for A0 and 3.3 V input voltage for A1 • Supports nominal run and low power standby modes • Supports at 0.9 ~ 1.3 V output in run mode • Supports at 0.9 ~ 1.0 V output in standby mode • Over current and over voltage detection
eDMA	enhanced Direct Memory Access	System Control Peripherals	There is an enhanced DMA (eDMA) engine and two DMA_MUX. • The eDMA is a 32 channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor. • The DMA_MUX is capable of multiplexing up to 128 DMA request sources to the 32 DMA channels of eDMA.
ENC	Quadrature Encoder/Decoder	Timer Peripherals	The enhanced quadrature encoder/decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EWM	External Watchdog Monitor	Timer Peripherals	The EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
FlexIO1 FlexIO2	Flexible Input/output	Connectivity and Communications	The FlexIO is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active.
FlexPWM1 FlexPWM2 FlexPWM3 FlexPWM4	Pulse Width Modulation	Timer Peripherals	The pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms.
FlexRAM	RAM	Memories	The i.MX RT1050 has 512 KB of on-chip RAM which could be flexible allocated to I-TCM, D-TCM, and on-chip RAM (OCRAM) in a 32 KB granularity. The FlexRAM is the manager of the 512 KB on-chip RAM array. Major functions of this blocks are: interfacing to I-TCM and D-TCM of Arm core and OCRAM controller; dynamic RAM arrays allocation for I-TCM, D-TCM, and OCRAM.
FlexSPI	Quad Serial Peripheral Interface	Connectivity and Communications	FlexSPI acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT1 GPT2	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
KPP	Keypad Port	Human Machine Interfaces	The KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: • Multiple-key detection • Long key-press detection • Standby key-press detection • Supports a 2-point and 3-point contact key matrix

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Multimedia Peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capabilities. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
LPI2C1 LPI2C2 LPI2C3 LPI2C4	Low Power Inter-integrated Circuit	Connectivity and Communications	The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master. The I2C provides a method of communication between a number of external devices. More detailed information, see Section 4.9.2, “LPI2C module timing parameters.
LPSPI1 LPSPI2 LPSPI3 LPSPI4	Low Power Serial Peripheral Interface	Connectivity and Communications	The LPSPI is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. • It can continue operating while the chip is in stop modes, if an appropriate clock is available • Designed for low CPU overhead, with DMA off loading of FIFO register access
LPUART1 LPUART2 LPUART3 LPUART4 LPUART5 LPUART6 LPUART7 LPUART8	UART Interface	Connectivity Peripherals	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PXP	Pixel Processing Pipeline	Multimedia Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications.
QuadTimer1 QuadTimer2 QuadTimer3 QuadTimer4	QuadTimer	Timer Peripherals	The quad-timer provides four time channels with a variety of controls affecting both individual and multi-channel features.Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ROMCP	ROM Controller with Patch	Memories and Memory Controllers	The ROMCP acts as an interface between the Arm advanced high-performance bus and the ROM. The on-chip ROM is only used by the Cortex-M7 core during boot up. Size of the ROM is 96 KB.
RTC OSC	Real Time Clock Oscillator	Clock Sources and Control	The RTC OSC provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.678 kHz reference clock for the RTC.
RTWDOG	Watch Dog	Timer Peripherals	The RTWDG module is a high reliability independent timer that is available for system to use. It provides a safety feature to ensure software is executing as planned and the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU. Windowed refresh mode is supported as well.
SAI1 SAI2 SAI3	Synchronous Audio Interface	Multimedia Peripherals	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SA-TRNG	Standalone True Random Number Generator	Security	The SA-TRNG is hardware accelerator that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions.
SEMC	Smart External Memory Controller	Memory and Memory Controller	The SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The interface supported includes SDRAM, NOR Flash, SRAM, and NAND Flash, as well as 8080 display interface.
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX RT1050 processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port is accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX RT1050 SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 2. i.MX RT1050 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
Temp Monitor	Temperature Monitor	Analog	The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.
TSC	Touch Screen	Human Machine Interfaces	With touch controller to support 4-wire and 5-wire resistive touch panel.
USBO2	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX RT1050 specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
WDOG1 WDOG2	Watch Dog	Timer Peripherals	The watchdog (WDOG) Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XBAR	Cross BAR	Cross Trigger	Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX RT1050 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output (LVDS I/O) is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX RT1050 Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
DCDC_PSWITCH	PAD is in DCDC_IN domain and connected the ground to bypass DCDC. To enable DCDC function, assert to DCDC_IN with at least 1ms delay for DCDC_IN rising edge.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.

Table 3. Special signal considerations (continued)

Signal Name	Remarks
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX RT1050 reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.
WAKEUP	A GPIO powered by SNVS domain power supply which can be configured as wakeup source in SNVS mode.

Table 4. JTAG Controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended connections for unused analog interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Not connected
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Not connected
ADC	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT1050 processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX RT1050 chip-Level conditions

For these characteristics	Topic appears
Absolute maximum ratings	on page 17
10 x 10 MM (VM) thermal resistance	on page 18
Operating ranges	on page 19
External clock sources	on page 20
Maximum supply currents	on page 21
Low power mode supply currents	on page 22
USB PHY current consumption	on page 22

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 shows the absolute maximum operating ratings.

Table 7. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
Core supplies input voltage	VDD_SOC_IN	-0.3	1.3	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
Power for DCDC	DCDC_IN	-0.3	3.6	V
Supply input voltage to Secure Non-Volatile Storage and Real Time Clock	VDD_SNVS_IN	-0.3	3.6	V
USB VBUS supply	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Supply for 12-bit ADC	VDDA_ADC	3	3.6	V

Table 7. Absolute maximum ratings (continued)

IO supply for GPIO in SDIO1 bank (3.3 V mode)	NVCC_SD0	3	3.6	V
IO supply for GPIO in SDIO1 bank (1.8 V mode)		1.65	1.95	V
IO supply for GPIO in SDIO2 bank (3.3 V mode)	NVCC_SD1	3	3.6	V
IO supply for GPIO in SDIO2 bank (1.8 V mode)		1.65	1.95	V
IO supply for GPIO in EMC bank (3.3 V mode)	NVCC_EMC	3	3.6	V
IO supply for GPIO in EMC bank (1.8 V mode)		1.65	1.95	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 1000 500	V
Input/Output Voltage range	$V_{in/Vout}$	-0.5	OVDD + 0.3[1]	V
Storage Temperature range	$T_{STORAGE}$	-40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 10 x 10 MM (VM) thermal resistance

Table 8 displays the 10 x 10 MM (VM) package thermal resistance data.

Table 8. 10 x 10 MM (VM) thermal resistance data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	72.1	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	43.9	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	57.5	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	39.0	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	26.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.1	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	$R_{\theta JB\_CSB}$	22.3	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

[7] Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating ranges

Table 9 provides the operating ranges of the i.MX RT1050 processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

Table 9. Operating ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode	VDD_SOC_IN	Overdrive	1.25	—	1.3	V	—
	VDD_SOC_IN	M7 core at 528 MHz	1.15	—	1.3	V	—
		M7 core at 132 MHz	1.15	—	1.3		
		M7 core at 24 MHz	0.925	—	1.3		
IDLE Mode	VDD_SOC_IN	M7 core operation at 528 MHz or below	1.15	—	1.3	V	—
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.925	—	1.3	V	Refer to Table 12 Low power mode current and power consumption
SNVS Mode	VDD_SOC_IN	—	0		1.3	V	—
Power for DCDC	DCDC_IN	—	2.8	3.0	3.6	V	—
VDD_HIGH internal Regulator	VDD_HIGH_IN[2]	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[3]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—
GPIO supplies	NVCC_GPIO	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
	NVCC_SD1						
	NVCC_SD2						
	NVCC_EMC						

Table 9. Operating ranges (continued)

A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered even if the ADC is not used. VDDA_ADC_3P3 cannot be powered when the other SoC supplies (except VDD_SNVS_IN) are off.
Temperature Operating Ranges							
Junction temperature	Tj	Standard Commercial	0	—	95	°C	See the application note, i.MX RT1050 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

2 Applying the maximum voltage results in shorten lifetime. 3.6 V usage limited to < 1% of the use profile. Reset of profile limited to below 3.49 V.

3 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX RT1050 Hardware Development Guide* (IMXRT1050HDG).

4.1.4 External clock sources

Each i.MX RT1050 processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 10 shows the interface frequency requirements.

Table 10. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP SDK to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 μA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

See the i.MX RT1050 Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximum supply currents

Power Rail	Conditions	Max Current	Unit
DCDC_IN	Max power for FF chip at 95 °C	100	mA
VDD_HIGH_IN	Include internal loading in analog	50	mA
VDD_SNVS_IN	—	250	μA
USB_OTG1_VBUS USB_OTG2_VBUS	25 mA for each active USB interface	50	mA
VDDA_ADC_3P3	3.3 V power supply for 12-bit ADC, 600 μA typical, 750 μA max, for each ADC. 100 Ohm max loading for touch panel, cause 33 mA current.	40	mA
NVCC_GPIO NVCC_SD0 NVCC_SD1 NVCC_EMC	Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.		

4.1.6 Low power mode supply currents

Table 12 shows the current core consumption (not including I/O) of i.MX RT1050 processors in selected low power modes.

Table 12. Low power mode current and power consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE	• LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	4.0	mA
		VDD_HIGH_IN (3.3 V)	4.7	
		VDD_SNVS_IN (3.3 V)	0.036	
		Total	27.63	mW
LOW POWER IDLE	• LDO_2P5 and LDO_1P1 are set to Weak mode • WFI, half FlexRAM power down in power gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	2.2	mA
		VDD_HIGH_IN (3.3 V)	0.3	
		VDD_SNVS_IN (3.3 V)	0.042	
		Total	7.73	mW
SUSPEND (DSM)	• LDO_2P5 and LDO_1P1 are shut off • CPU in Power Gate mode • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • Peripheral clock gated, but remain powered	DCDC_IN (3.0 V for A0 and 3.3 V for A1)	0.2[2]	mA
		VDD_HIGH_IN (3.3 V)	0.037	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.788	mW
SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive	DCDC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.3 V)	0.02	
		Total	0.066	mW

1 Typical process material in fab

2 Average current

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY current consumption in power down mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	< 0.5 μA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 System power and clocks

This section provide the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable.
- POR_B should be held low during the entire power up sequence.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS, USB_OTG2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

4.2.1.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see "Power Rail" columns in pin list tables of Section 6, "Package information and contact assignments."

4.2.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1050 Reference Manual* (IMXRT1050_RM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.2.2.1 Digital regulators (LDO_SNVS)

There are one digital LDO regulator ("Digital", because of the logic loads that they drive, not because of their construction). The advantages of the regulator is to reduce the input supply variation because of its input supply ripple rejection and its on-die trimming. This translates into more stable voltage for the on-chip logics.

The regulator has two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the target voltage.

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

4.2.2.2 Regulators for analog modules

4.2.2.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V

to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050_RM).

4.2.2.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB PHY, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).

4.2.2.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX RT1050 Crossover Processors* (IMXRT1050HDG).

For additional information, see the *i.MX RT1050 Reference Manual* (IMXRT1050RM).