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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





**ARM Cortex™ -M0**  
**32-BIT MICROCONTROLLER**

**NuMicro Mini51™ DE Series**  
**Datasheet**

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## 1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with ARM® Cortex™-M0 core for industrial control and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz and operate at 2.5V ~ 5.5V, -40°C ~ 105°C, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro Mini51™ series offers 4K/8K/16K-bytes embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I<sup>2</sup>C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NuMicro Mini51™ series in order to reduce component count, board space and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.



## 2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.5 V to 5.5 V
- Memory
  - 4 KB/ 8 KB/ 16 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - ◆ Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for Power-down wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25°C, 5V)
    - ◆ Dynamically calibrating the HIRC OSC to 22.1184 MHz  $\pm 1\%$  from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up
- I/O Port
  - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - ◆ Input-only with high impedance
    - ◆ Push-pull output
    - ◆ Open-drain output
    - ◆ Quasi-bidirectional
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable default I/O mode of all pins after POR
- Timer

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode
- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTS<sub>n</sub> and RTS<sub>n</sub>)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer
- I<sup>2</sup>C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40°C~105°C
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP



### 3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 4.1-1 List of Abbreviations



## 4 PARTS INFORMATION LIST AND PIN CONFIGURATION

### 4.1 NuMicro Mini51™ Series Selection Code

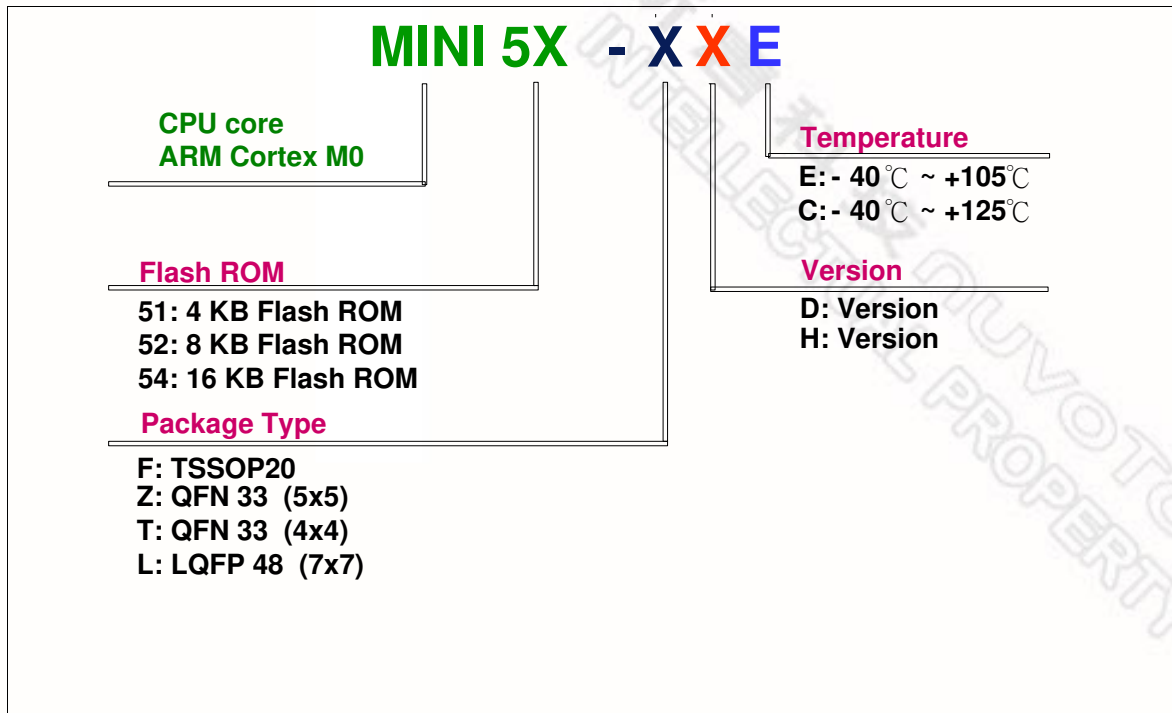


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

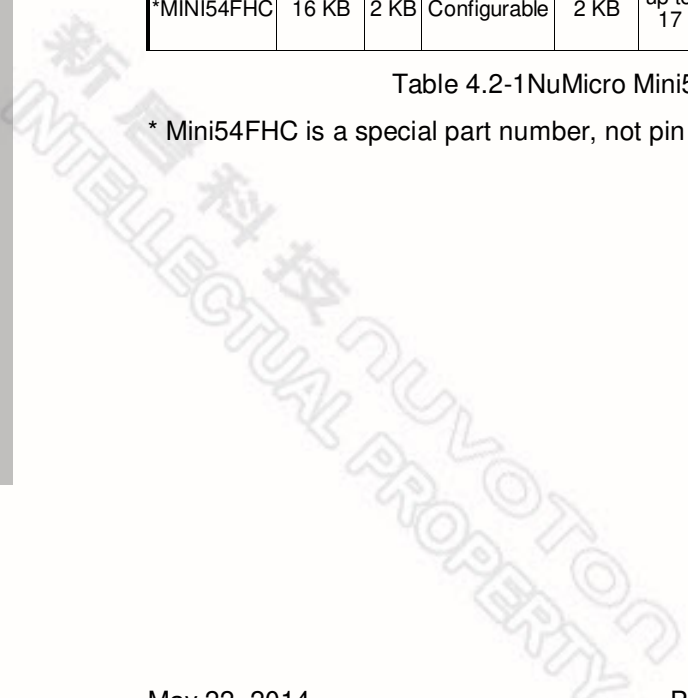


4.2 NuMicro Mini51™ Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP IAP	IRC 22.1184 MHz	Package
							UART	SPI	I <sup>2</sup> C						
MINI51FDE	4 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI51LDE	4 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI51TDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI52FDE	8 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI52LDE	8 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI52TDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI54FDE	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI54LDE	16 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI54TDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
*MINI54FHC	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	6	3x10-bit	v	v	TSSOP20

Table 4.2-1 NuMicro Mini51™ Series Product Selection Guide

\* Mini54FHC is a special part number, not pin to pin compatible to others Mini51 series part number.





### 4.3 PIN CONFIGURATION

#### 4.3.1 LQFP 48-pin

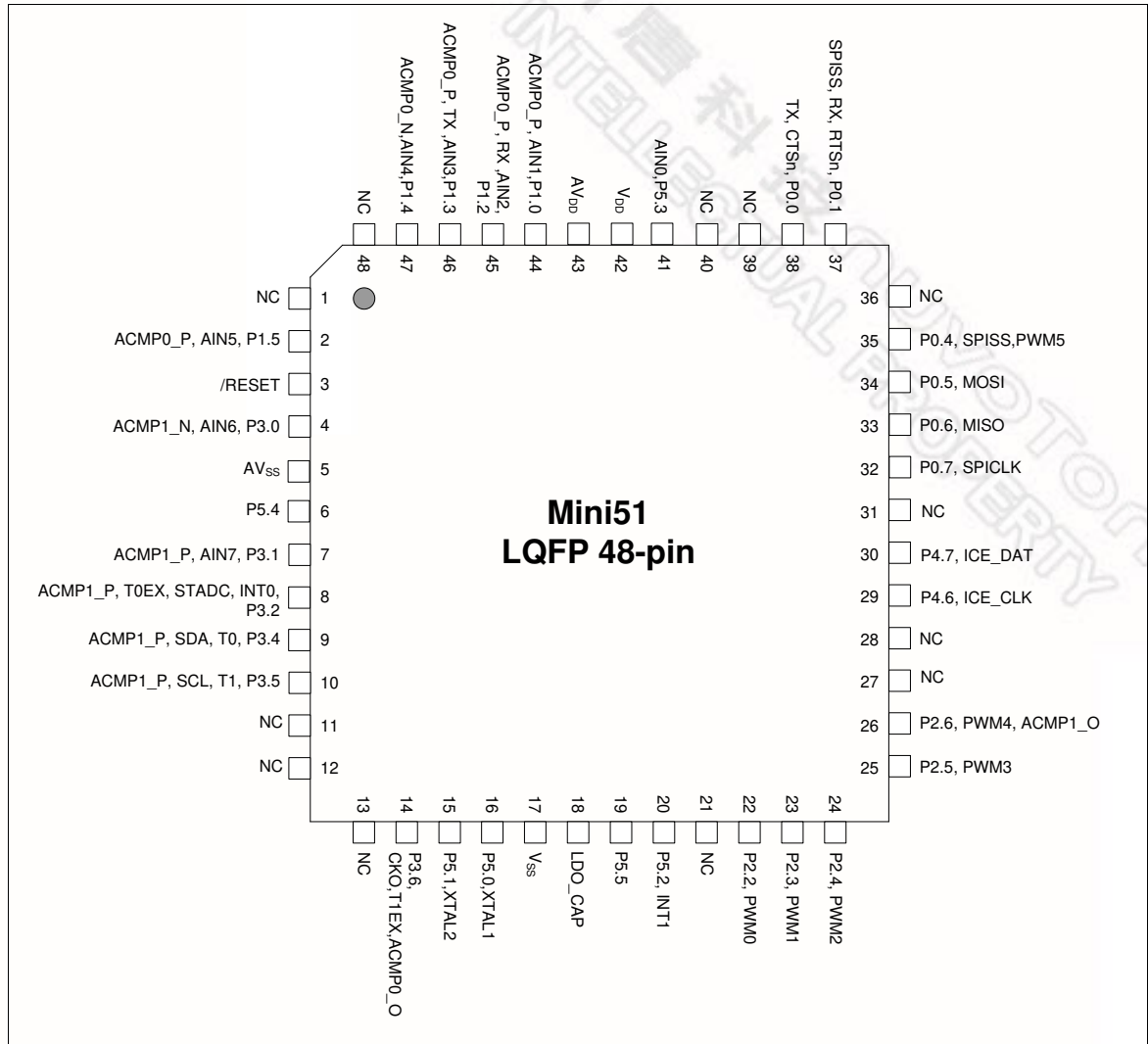


Figure 4.3-1 NuMicro Mini51™ Series LQFP 48-pin Diagram



4.3.2 QFN 33-pin

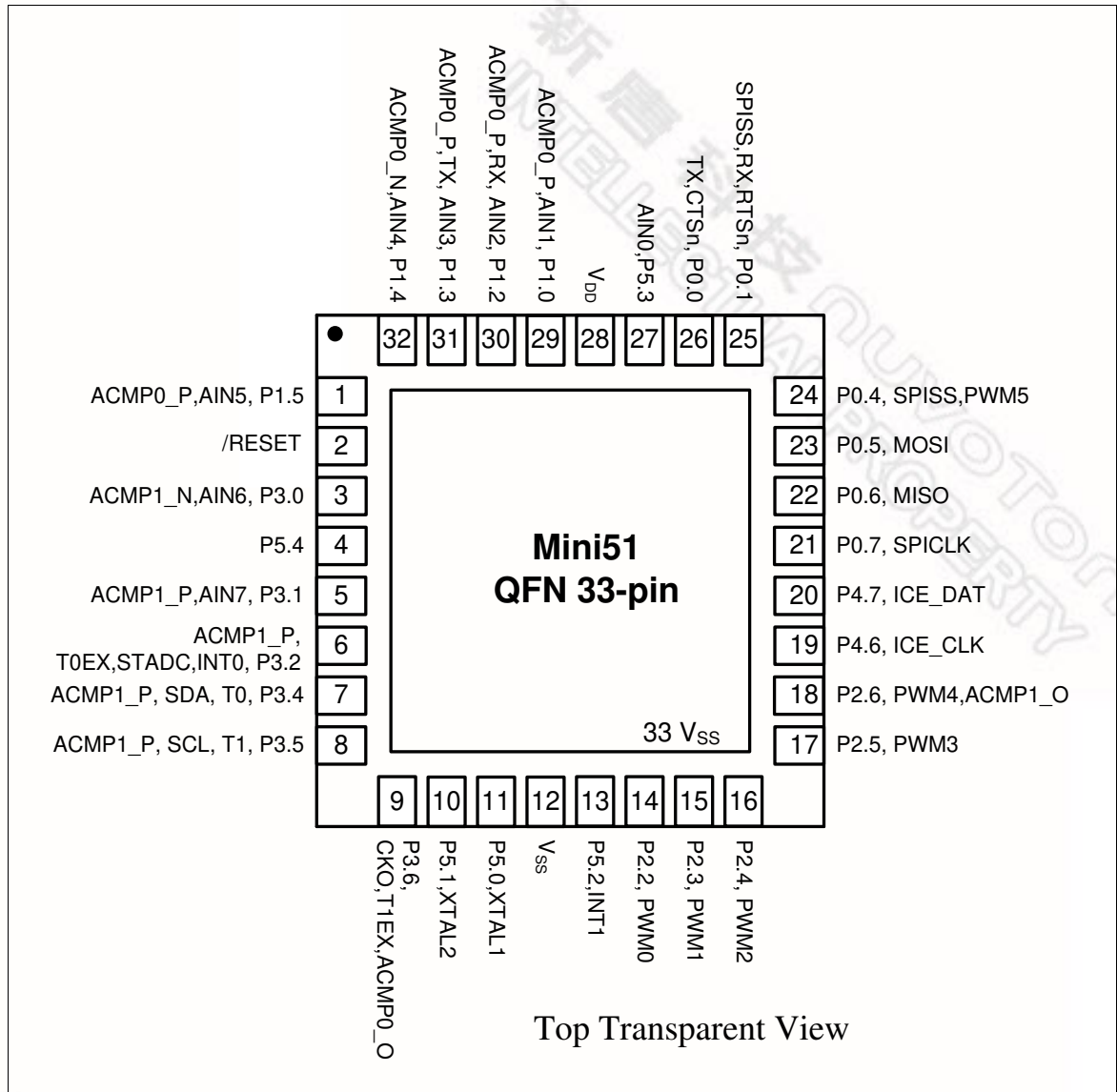


Figure 4.3-2 NuMicro Mini51™ Series QFN 33-pin Diagram



4.3.3 TSSOP 20-pin

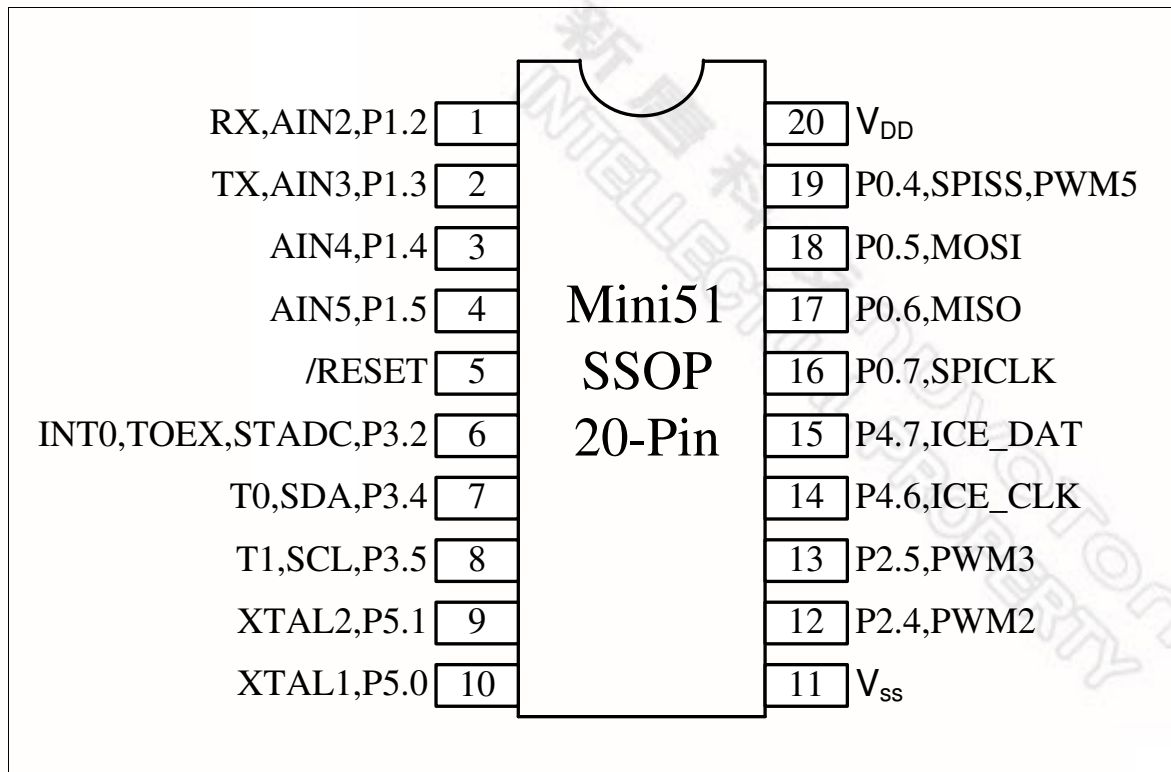


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

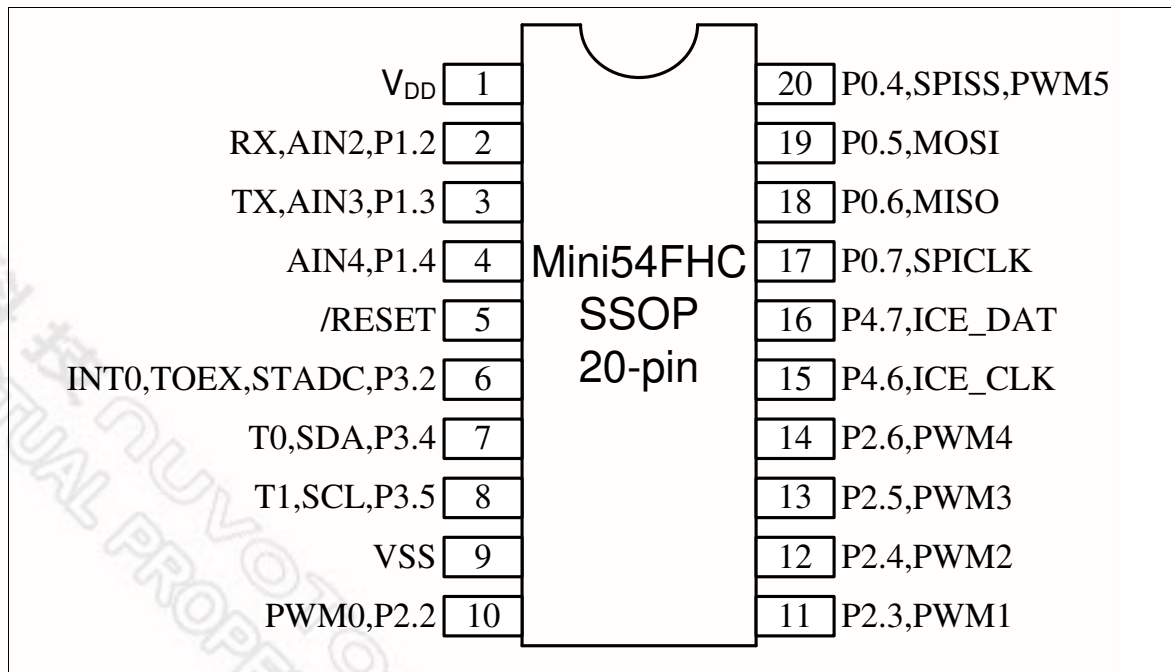


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram



#### 4.4 Pin Description

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
1	---	---	---	NC	---	Not connected
2	1	4	---	P1.5	I/O	General purpose digital I/O pin
				AIN5	AI	ADC analog input pin
				ACMP0_P	AI	Analog comparator positive input pin
3	2	5	5	/RESET	I(ST)	The Schmitt trigger input pin for hardware device reset. A "Low" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	---	P3.0	I/O	General purpose digital I/O pin
				AIN6	AI	ADC analog input pin
				ACMP1_N	AI	Analog comparator negative input pin
5	---	---	---	AV <sub>SS</sub>	AP	Ground pin for analog circuit
6	4	---	---	P5.4	I/O	General purpose digital I/O pin
7	5	---	---	P3.1	I/O	General purpose digital I/O pin
				AIN7	AI	ADC analog input pin
				ACMP1_P	AI	Analog comparator positive input pin
8	6	6	6	P3.2	I/O	General purpose digital I/O pin
				INT0	I	External interrupt 0 input pin
				STADC	I	ADC external trigger input pin
				T0EX	I	Timer 0 external capture/reset trigger input pin
				ACMP1_P	AI	Analog comparator positive input pin
9	7	7	7	P3.4	I/O	General purpose digital I/O pin
				T0	I/O	Timer 0 external event counter input pin
				SDA	I/O	I <sup>2</sup> C data I/O pin
				ACMP1_P	AI	Analog comparator positive input pin
10	8	8	8	P3.5	I/O	General purpose digital I/O pin
				T1	I/O	Timer 1 external event counter input pin
				SCL	I/O	I <sup>2</sup> C clock I/O pin
				ACMP1_P	AI	Analog comparator positive input pin
11	---	---	---	NC	---	Not connected.
12	---	---	---	NC	---	Not connected.
13	---	---	---	NC	---	Not connected.



Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
14	9	---	---	P3.6	I/O	General purpose digital I/O pin.
				ACMP0_O	O	Analog comparator output pin.
				CKO	O	Frequency divider output pin.
				T1EX	I	Timer 1 external capture/reset trigger input pin.
15	10	9	---	P5.1	I/O	General purpose digital I/O pin.
				XTAL2	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	10	---	P5.0	I/O	General purpose digital I/O pin.
				XTAL1	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	11	9	V <sub>SS</sub>	P	Ground pin for digital circuit.
	33					
18	---	---	---	LDO_CAP	P	LDO output pin.
19	---	---	---	P5.5	I/O	General purpose digital I/O pin. User program must enable pull-up resistor in the QFN-33 package.
20	13	---	---	P5.2	I/O	General purpose digital I/O pin.
				INT1	I	External interrupt 1 input pin.
21	---	---	---	NC	---	Not connected.
22	14	---	10	P2.2	I/O	General purpose digital I/O pin.
				PWM0	O	PWM0 output of PWM unit.
23	15	---	11	P2.3	I/O	General purpose digital I/O pin.
				PWM1	O	PWM1 output of PWM unit.
24	16	12	12	P2.4	I/O	General purpose input/output digital pin.
				PWM2	O	PWM2 output of PWM unit.
25	17	13	13	P2.5	I/O	General purpose digital I/O pin.
				PWM3	O	PWM3 output of PWM unit.
26	18	---	14	P2.6	I/O	General purpose digital I/O pin.
				PWM4	O	PWM4 output of PWM unit.
				ACMP1_O	O	Analog comparator output pin.
27	---	---	---	NC	---	Not connected.
28	---	---	---	NC	---	Not connected.
29	19	14	15	P4.6	I/O	General purpose digital I/O pin.





Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				ICE_CLK	I	Serial wired debugger clock pin.
30	20	15	16	P4.7	I/O	General purpose digital I/O pin.
				ICE_DAT	I/O	Serial wired debugger data pin.
31	---	---	---	NC	---	Not connected.
32	21	16	17	P0.7	I/O	General purpose digital I/O pin.
				SPICLK	I/O	SPI serial clock pin.
33	22	17	18	P0.6	I/O	General purpose digital I/O pin.
				MISO	I/O	SPI MISO (master in/slave out) pin.
34	23	18	19	P0.5	I/O	General purpose digital I/O pin.
				MOSI	O	SPI MOSI (master out/slave in) pin.
35	24	19	20	P0.4	I/O	General purpose digital I/O pin.
				SPISS	I/O	SPI slave select pin.
				PWM5	O	PWM5 output of PWM unit.
36	---	---	---	NC	---	Not connected.
37	25	---	---	P0.1	I/O	General purpose digital I/O pin.
				RTSn	O	UART RTS pin.
				RX	I	UART data receiver input pin.
				SPISS	I/O	SPI slave select pin.
38	26	---	---	P0.0	I/O	General purpose digital I/O pin.
				CTSn	I	UART CTS pin.
				TX	O	UART transmitter output pin.
39	---	---	---	NC	---	Not connected.
40	---	---	---	NC	---	Not connected.
41	27	---	---	P5.3	I/O	General purpose digital I/O pin.
				AIN0	AI	ADC analog input pin.
42	28	20	1	V <sub>DD</sub>	P	Power supply for digital circuit.
43				AV <sub>DD</sub>	P	Power supply for analog circuit.
44	29	---	---	P1.0	I/O	General purpose digital I/O pin.
				AIN1	AI	ADC analog input pin.
				ACMP0_P	AI	Analog comparator positive input pin.
45	30	1	2	P1.2	I/O	General purpose digital I/O pin.
				AIN2	AI	ADC analog input pin.



Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				RX	I	UART data receiver input pin.
				ACMP0_P	AI	Analog comparator positive input pin.
46	31	2	3	P1.3	I/O	General purpose digital I/O pin.
				AIN3	AI	ADC analog input pin.
				TX	O	UART transmitter output pin.
				ACMP0_P	AI	Analog comparator positive input pin.
47	32	3	4	P1.4	I/O	General purpose digital I/O pin.
				AIN4	I/O	PWM5: PWM output/Capture input.
				ACMP0_N	AI	Analog comparator negative input pin.
48	---	--	--	NC	---	Not connected.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.



## 5 BLOCK DIAGRAM

### 5.1 NuMicro Mini51™ Block Diagram

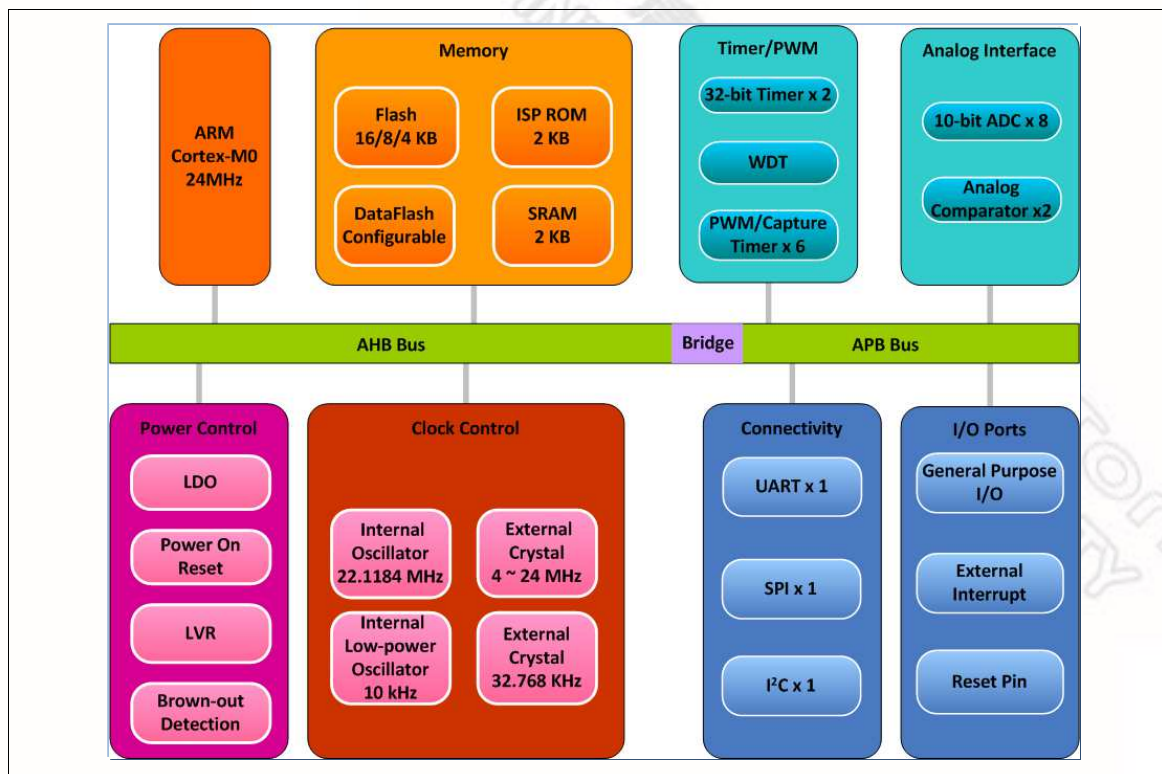


Figure 5.1-1 NuMicro Mini51™ Series Block Diagram



## 6 FUNCTIONAL DESCRIPTION

### 6.1 Memory Organization

#### 6.1.1 Overview

The NuMicro Mini51™ series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NuMicro Mini51™ series only supports little-endian data format.

#### 6.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Addressing Space	Token	Modules
<b>Flash and SRAM Memory Space</b>		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
<b>AHB Modules Space (0x5000_0000 – 0x501F_FFFF)</b>		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0~P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
<b>APB Modules Space (0x4000_0000 – 0x401F_FFFF)</b>		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I <sup>2</sup> C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with Master/slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
<b>System Control Space (0xE000_E000 – 0xE000_EFFF)</b>		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6.1-1 Address Space Assignments for On-Chip Modules



## 6.2 Nested Vectored Interrupt Controller (NVIC)

### 6.2.1 Overview

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features.

### 6.2.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

### 6.2.3 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro Mini51™ series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as 0 and the lowest priority is denoted as 3. The default priority of all the user-configurable interrupts is 0. Note that the priority 0 is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCAll	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-1 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	-	-	System exceptions	-
16	0	<b>BOD_OUT</b>	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	<b>WDT_INT</b>	WDT	Watchdog Timer interrupt	Yes
18	2	<b>EINT0</b>	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	<b>EINT1</b>	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	<b>GP0/1_INT</b>	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	<b>GP2/3/4_INT</b>	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	<b>PWM_INT</b>	PWM	PWM interrupt	No
23	7	<b>BRAKE_INT</b>	PWM	PWM interrupt	No
24	8	<b>TMR0_INT</b>	TMR0	Timer 0 interrupt	Yes
25	9	<b>TMR1_INT</b>	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	-	-	-	-
28	12	<b>UART_INT</b>	UART	UART interrupt	Yes