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ARM Cortex™-M0
32-BIT MICROCONTROLLER

NuMicro™ Family
Mini51 Series DataSheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with an ARM® Cortex™-M0 core for industrial controls and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz, and thus can afford to support a variety of industrial controls and applications requiring high CPU performance. The NuMicro Mini51™ series provides 4K/8K/16K-byte embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte embedded SRAM.

A number of system-level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and low voltage detector, have been incorporated in the NuMicro Mini51™ series to reduce component count, board space, and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, allowing user to update program memory without removing a chip from an actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for 32 interrupt inputs, each with 4-level priority
  - Supports Serial Wire Debug (SWD) with 2 watchpoints/4 breakpoints
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 4KB/8KB/16KB flash memory for program memory (APROM)
  - Configurable flash memory for data memory (Data Flash)
  - 2KB flash memory for loader (LDROM)
  - 2KB SRAM for internal scratch-pad RAM (SRAM)
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz crystal oscillator (HXT)
  - 32.768K crystal oscillator (LXT) for idle wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.0 MHz ±1% from -40^0C to 85^0C by external 32.768K crystal oscillator (LXT)
  - 10 KHz internal low-power oscillator (LIRC) for watchdog and idle wake-up
- I/O Port
  - Up to 30 GPIO (General Purpose I/O) pins for LQFP-48 package
  - Software-configured I/O type
    - Quasi-bidirectional input/output
    - Push-pull output
    - Open-drain output
    - Input-only (high impendence)
  - Optional Schmitt trigger input
- Timer
  - Two 24-bit Timers with 8-bit prescaler
    - Supports Event Counter mode
    - Supports Toggle Output mode

- Supports external trigger in Pulse Width Measurement mode
  - Supports external trigger in Pulse Width Capture mode

- Watchdog Timer
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable when time-out happens
- PWM
  - Up to three built-in 16-bit PWM generators with six PWM outputs or three complementary paired PWM outputs
  - Supports edge alignment or center alignment
  - Supports fault detection
  - Individual clock source, clock divider, 8-bit prescalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI device
  - Masters up to 12 MHz, and Slaves up to 4 MHz
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Byte Suspend mode in 32-bit transmission
- I^2C
  - Supports Master/Slave mode
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus

- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allowing for versatile rate control
- Supports multiple address recognition (4 slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 150K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started by software or external pin
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- BOD (Brown-Out Detection) Reset
  - Three programmable threshold levels: 3.8V/2.7V/2.0V (default as 2.0V)
  - Optional BOD interrupt or reset
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - LQFP 48-pin (7x7), QFN 33-pin (5x5), QFN 33-pin (4x4)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro Mini51™ Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI51LAN	4 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI51TAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI52LAN	8 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI52TAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI54LAN	16 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI54TAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)

Figure 3.1-1 NuMicro Mini51™ Series Product Selection Guide

3.2 PIN CONFIGURATION

3.2.1 LQFP 48-pin

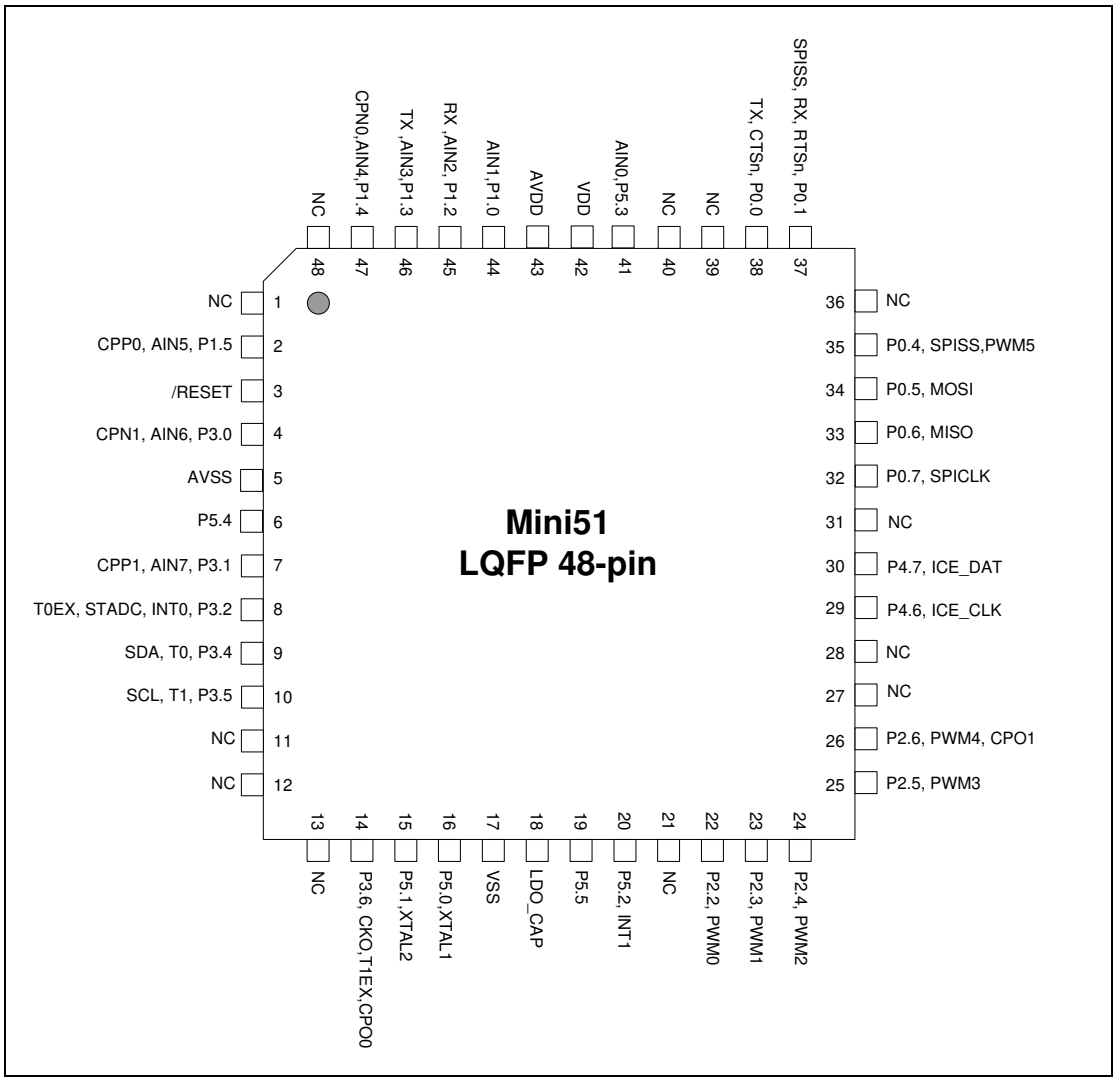

Figure 3.2-1 NuMicro Mini51™ Series LQFP 48-pin Assignment

3.2.2 QFN 33-pin

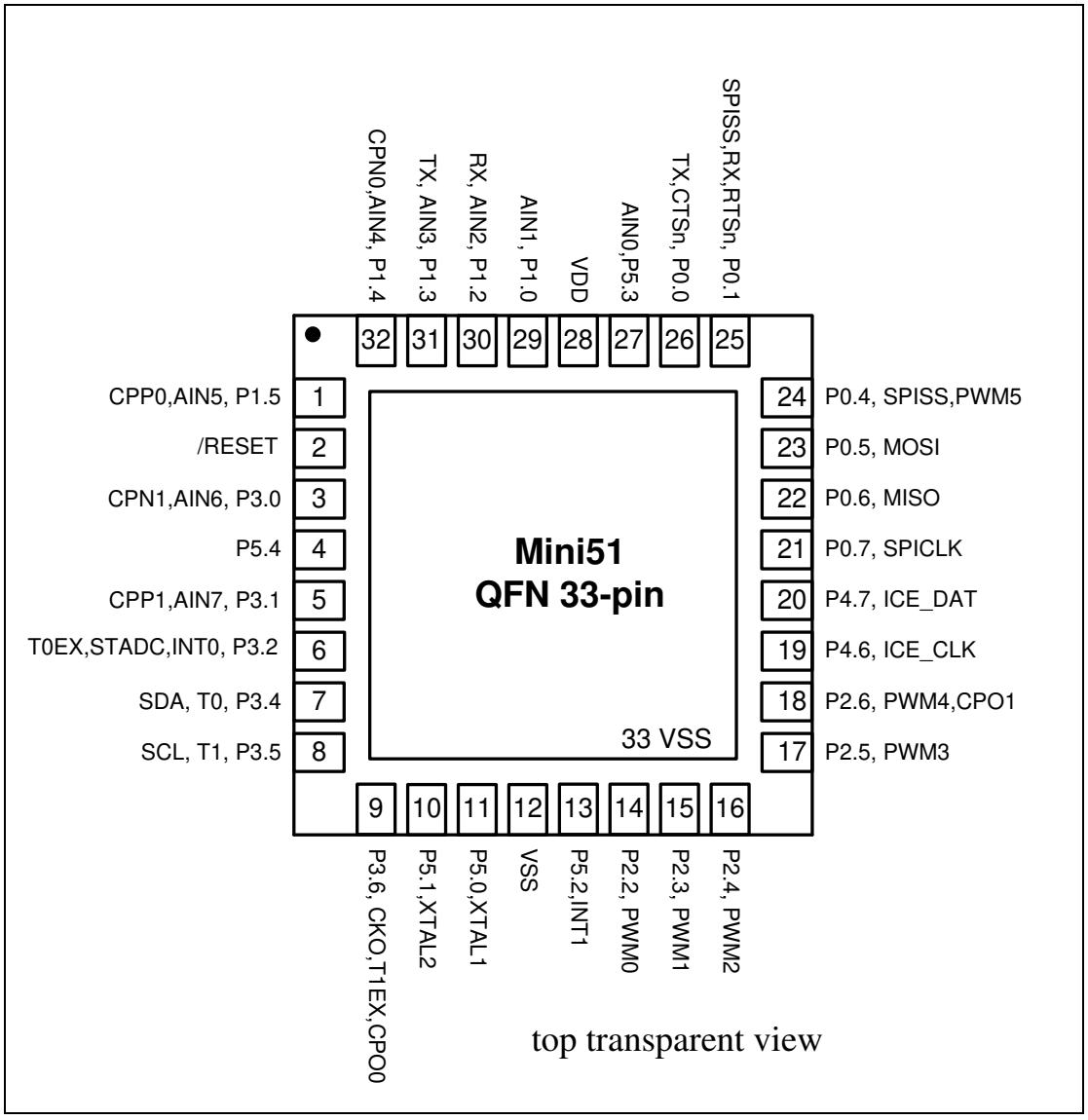

Figure 3.2-2 NuMicro Mini51™ Series QFN 33-pin Assignment

3.3 Pin Description

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
1		NC		Not connected
2	1	P1.5	**I/O**	Digital GPIO pin
		AIN5	**AI**	ADC analog input pin
		CPP0	**AI**	Analog comparator Positive input pin
3	2	/RESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	P3.0	**I/O**	Digital GPIO pin
		AIN6	**AI**	ADC analog input pin
		CPN1	**AI**	Analog comparator negative input pin
5		AVSS	**AP**	Ground pin for analog circuit
6	4	P5.4	**I/O**	Digital GPIO pin
7	5	P3.1	**I/O**	Digital GPIO pin
		AIN7	**AI**	ADC analog input pin
		CPP1	**AI**	Analog comparator positive input pin
8	6	P3.2	**I/O**	Digital GPIO pin
		INT0	**I**	External interrupt 0 input pin
		STADC	**I**	ADC external trigger input pin
		T0EX	**I**	Timer 0 external capture/reset trigger input pin
9	7	P3.4	**I/O**	Digital GPIO pin
		T0	**I/O**	Timer 0 external event counter input pin
		SDA	**I/O**	I^2C data I/O pin
10	8	P3.5	**I/O**	Digital GPIO pin
		T1	**I/O**	Timer 1 external event counter input pin
		SCL	**I/O**	I^2C clock I/O pin
11		NC		Not connected
12		NC		Not connected
13		NC		Not connected

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
14	9	P3.6	I/O	Digital GPIO pin
		CPO0	O	Analog comparator output pin
		CKO	O	Frequency divider output pin
		T1EX	I	Timer 1 external capture/reset trigger input pin
15	10	P5.1	I/O	Digital GPIO pin
		XTAL2	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	P5.0	I/O	Digital GPIO pin
		XTAL1	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	VSS	P	Ground pin for digital circuit
	33			
18		LDO_CAP	P	LDO output pin
19		P5.5	I/O	Digital GPIO pin User program must enable pull-up resistor in the QFN-33 package.
20	13	P5.2	I/O	Digital GPIO pin
		INT1	I	External interrupt 1 input pin
21		NC		Not connected
22	14	P2.2	I/O	Digital GPIO pin
		PWM0	O	PWM0 output of PWM unit
23	15	P2.3	I/O	Digital GPIO pin
		PWM1	O	PWM1 output of PWM unit
24	16	P2.4	I/O	Digital GPIO pin
		PWM2	O	PWM2 output of PWM unit
25	17	P2.5	I/O	Digital GPIO pin
		PWM3	O	PWM3 output of PWM unit
26	18	P2.6	I/O	Digital GPIO pin
		PWM4	O	PWM4 output of PWM unit
		CPO1	O	Analog comparator output pin
27		NC		Not connected

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
28		NC		Not connected
29	19	P4.6	I/O	Digital GPIO pin
		ICE_CLK	I	Serial wired debugger clock pin
30	20	P4.7	I/O	Digital GPIO pin
		ICE_DAT	I/O	Serial wired debugger data pin
31		NC		Not connected
32	21	P0.7	I/O	Digital GPIO pin
		SPICLK	I/O	SPI serial clock pin
33	22	P0.6	I/O	Digital GPIO pin
		MISO	I/O	SPI MISO (master in/slave out) pin
34	23	P0.5	I/O	Digital GPIO pin
		MOSI	O	SPI MOSI (master out/slave in) pin
35	24	P0.4	I/O	Digital GPIO pin
		SPISS	I/O	SPI slave select pin
		PWM5	O	PWM5 output of PWM unit
36		NC		Not connected
37	25	P0.1	I/O	Digital GPIO pin
		RTSn	O	UART RTS pin
		RX	I	UART data receiver input pin
		SPISS	I/O	SPI slave select pin
38	26	P0.0	I/O	Digital GPIO pin
		CTSn	I	UART CTS pin
		TX	O	UART transmitter output pin
39		NC		Not connected
40		NC		Not connected
41	27	P5.3	I/O	Digital GPIO pin
		AIN0	AI	ADC analog input pin
42	28	VDD	P	Power supply for digital circuit
43		AVDD	P	Power supply for analog circuit
44	29	P1.0	I/O	Digital GPIO pin

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
		AIN1	**AI**	ADC analog input pin
45	30	P1.2	**I/O**	Digital GPIO pin
		AIN2	**AI**	ADC analog input pin
		RX	**I**	UART data receiver input pin
46	31	P1.3	**I/O**	Digital GPIO pin
		AIN3	**AI**	ADC analog input pin
		TX	**O**	UART transmitter output pin
47	32	P1.4	**I/O**	Digital GPIO pin
		AIN4	**I/O**	PWM5: PWM output/Capture input
		CPN0	**AI**	Analog comparator negative input pin
48		NC		Not connected

Table 3.3-1 NuMicro Mini51™ Series Pin Description

[1] I/O type description: I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

4 BLOCK DIAGRAM

4.1 NuMicro Mini51™ Block Diagram

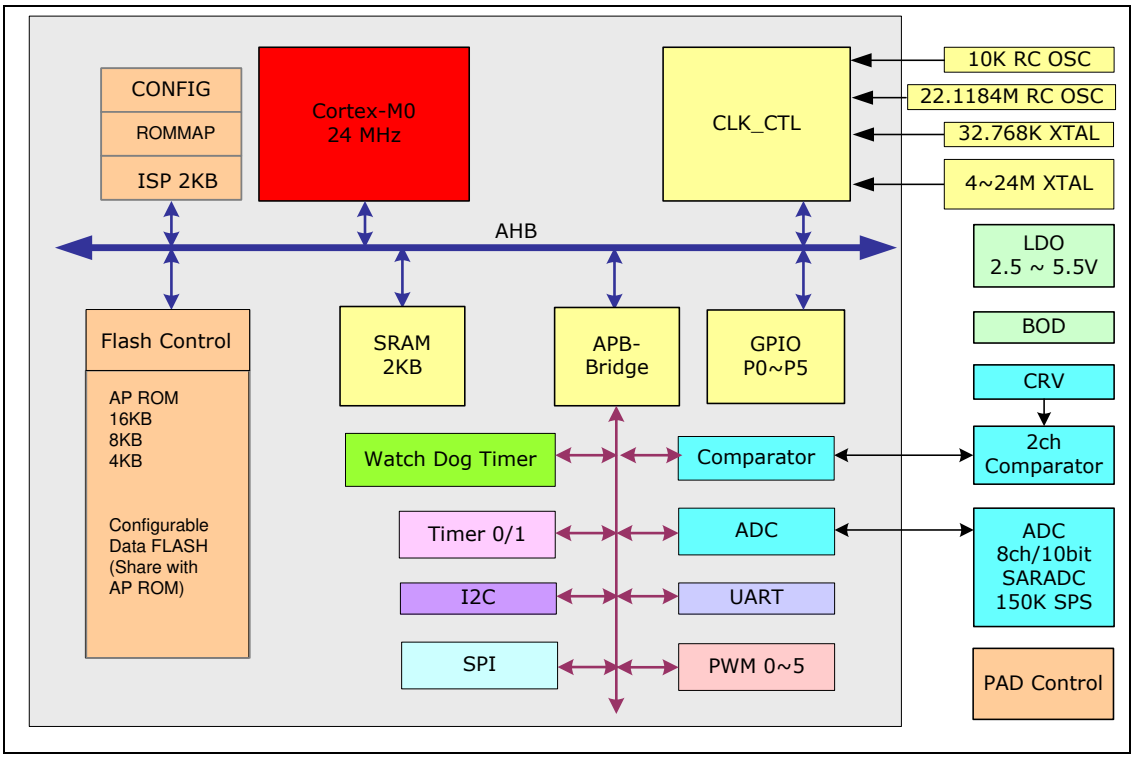

Figure 4.1-1 NuMicro Mini51™ Series Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 Memory Organization

5.1.1 Overview

The NuMicro Mini51™ series provides a 4G-byte address space for programmers. The memory locations assigned to each on-chip modules are shown in **錯誤! 找不到參照來源。**. The detailed register and memory addressing and programming will be described in the following sections for individual on-chip modules. The NuMicro Mini51™ series only supports little-endian data format.

5.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	CMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Controllers Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 5.1-1 Address Space Assignments for On-Chip Modules

5.2 Nested Vectored Interrupt Controller (NVIC)

5.2.1 Overview

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named “Nested Vectored Interrupt Controller (NVIC)”. It is closely coupled to the processor kernel and provides the following features.

5.2.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, the NVIC will also automatically save the processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.2.3 Exception Model and System Interrupt Map

The exception model supported by the NuMicro Mini51™ series is listed in the following table. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that the priority “0” is treated as the fourth priority on the system, after the three system exceptions “Reset”, “NMI” and “Hard

Fault".

Exception Name	Exception Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5.2-1 Exception Model

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception Description	Power-down Wake-up
1 ~ 15	-	**-**	-	System exceptions	-
16	0	**BOD_OUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	**-**	-	-	
28	12	**UART_INT**	UART	UART interrupt	Yes
29	13	**-**	-	-	

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception Description	Power-down Wake-up
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	**-**	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HFIRC_TRIM_INT**	HFIRC	HFIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	No
35 ~ 40	19 ~ 24	**-**	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or 1 interrupt	Yes
42 ~ 43	26 ~ 27	**-**	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	**-**	-	-	

Table 5.2-2 System Interrupt Map

5.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x0000_0000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in the previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number × 0x04	Exception Entry Pointer using that Exception Number

Table 5.2-3 Vector Table Format

5.2.5 NVIC Operation

NVIC interrupts can be enabled or disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, and both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

5.3 System Manager

5.3.1 Overview

The following functions are included in the system manager section:

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.3.2 System Reset

The system reset includes one of the following as the event occurs. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the /RESET pin
- Watchdog Time-out Reset (WDT)
- Brown-out Detected Reset (BOD)
- Cortex™-M0 CPU Reset
- Software one shot Reset

5.3.3 System Power Distribution

In this device, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS supplies power for analog module operation
- Digital power from VDD and VSS supplies power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins
- Built-in capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. **錯誤! 找不到參照來源。** shows the power architecture of this device.