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ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
Mini55 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® Mini55 series 32-bit microcontroller is embedded with ARM® Cortex®-M0 core for industrial control and applications which require high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The Mini55 series can run up to 48 MHz and operate at 2.1V ~ 5.5V, -40℃ ~ 105℃, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The Mini55 series offers 17.5K-bytes embedded program flash, size configurable Data Flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the Mini55 series in order to reduce component count, board space and system cost. These useful functions make the Mini55 series powerful for a wide range of applications.

Additionally, the Mini55 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. The Mini55 series also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage: 2.1V to 5.5V
- Memory
  - 17.5 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - Support 4 ~ 24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Support 32.768 kHz external low speed crystal oscillator (LXT) for idle wake-up and system operation clock
  - Built-in 48 MHz internal high speed RC oscillator (HIRC) for system operation (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±2% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
- I/O Port
  - Up to 33 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional Schmitt trigger input
- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer
    - Supports Event Counter mode

- Supports Toggle Output mode
- Supports external trigger in Pulse Width Measurement mode
- Supports external trigger in Pulse Width Capture mode
- Support Continuous Capture function can continuous capture 4 edge on one signal

- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Up to three built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - Supports edge-alignment or center-alignment
  - Supports fault detection
- UART (Universal Asynchronous Receiver/Transmitters)
  - Two UART devices
  - Buffered receiver and transmitter, 16-byte FIFO for first UART (UART0), and 4-byte FIFO for second UART (UART1)
  - Optional flow control function (CTSn and RTSn) in first UART 0 only
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI device
  - Master up to 25 MHz, and Slave up to 10 MHz
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - RX latching data can be either at rising edge or at falling edge of serial clock
  - TX sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte Suspend mode in 32-bit transmission
- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition (four slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 500 kSPS
  - Up to 12-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger or external pin trigger
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.4V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V/1.7V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 3KV, ESD HBM pass 6KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (4x4)

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® Mini55 Series Naming Rule

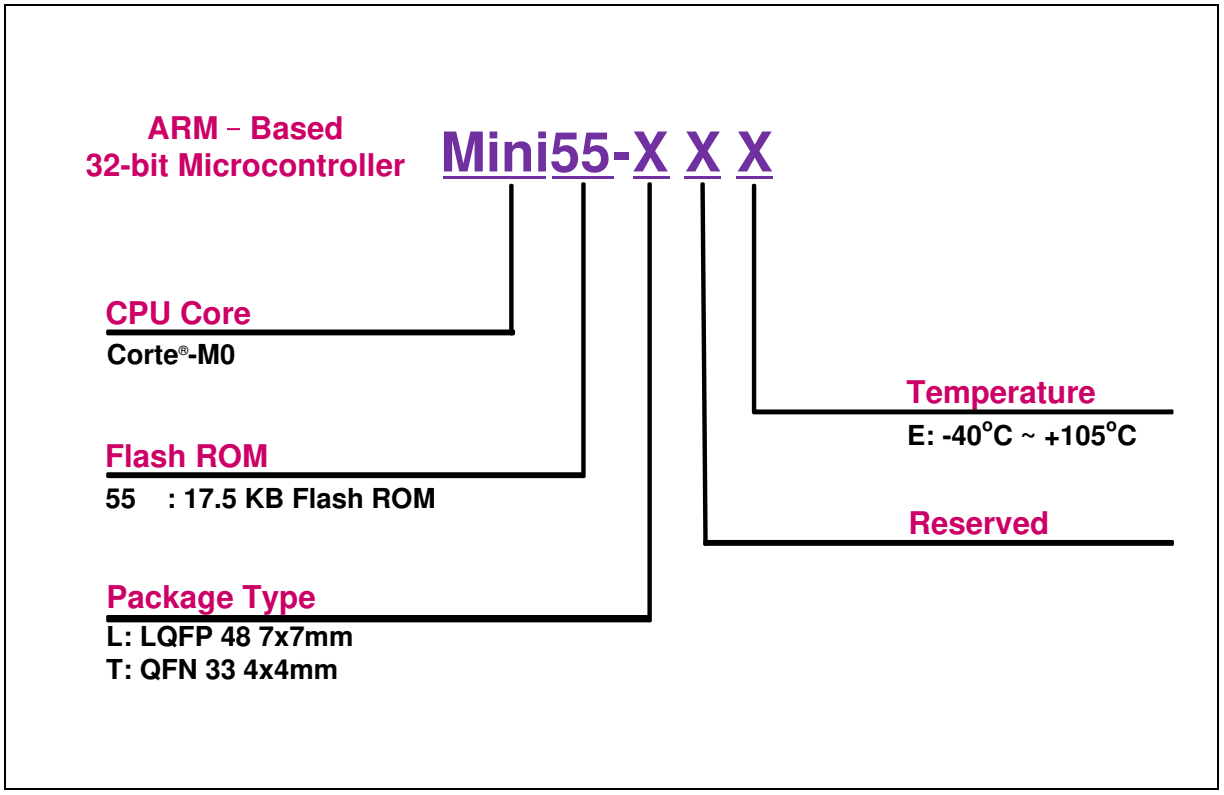

Figure 4.1-1 NuMicro® Mini55 Series Selection Code

4.2 NuMicro® Mini55 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer (32-bit)	Connectivity			Comp.	PWM	ADC (10-bit)	ISP ICP IAP	IRC 48MHz	Package
							UART	SPI	I^2C						
MINI55LDE	17.5 KB	2 KB	Configurable	2 KB	33	2	2	1	1	2	6	12	v	v	LQFP48
MINI55TDE	17.5 KB	2 KB	Configurable	2 KB	29	2	2	1	1	2	6	12	v	v	QFN33(4x4)

Table 4.2-1 NuMicro® Mini55 Series Product Selection Guide

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

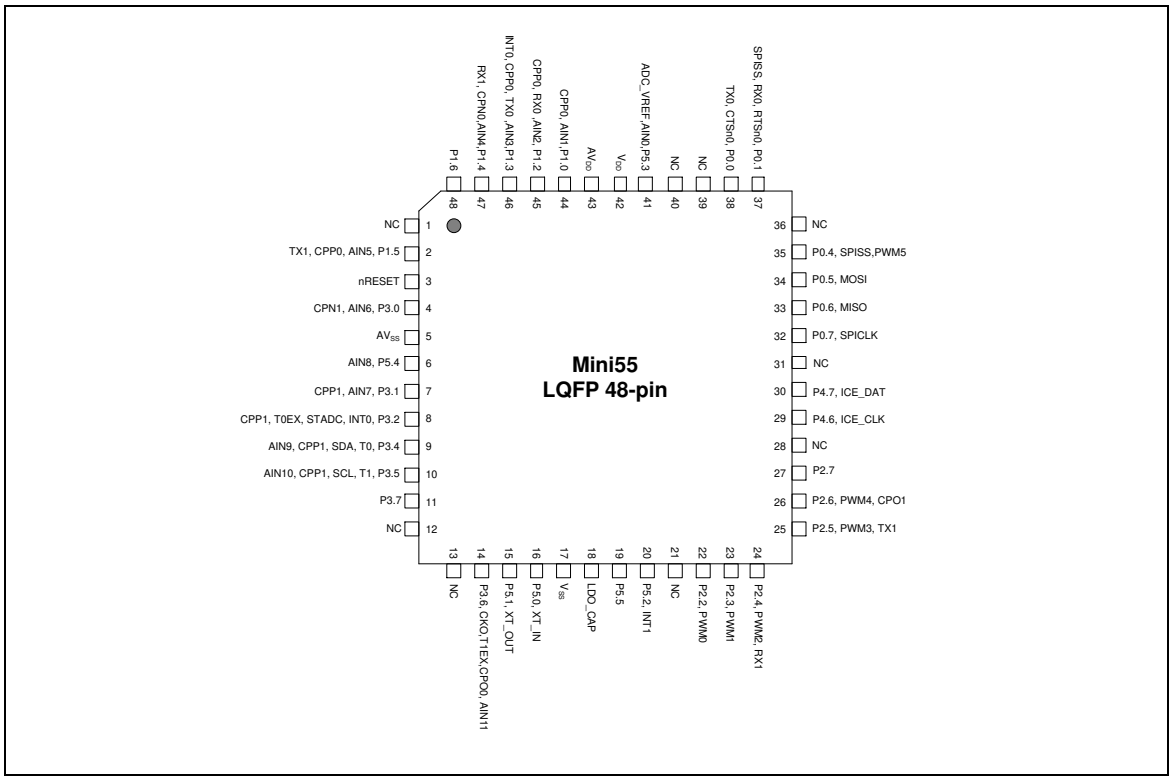

Figure 4.3-1 NuMicro® Mini55 Series LQFP 48-pin Diagram

4.3.2 QFN 33-pin

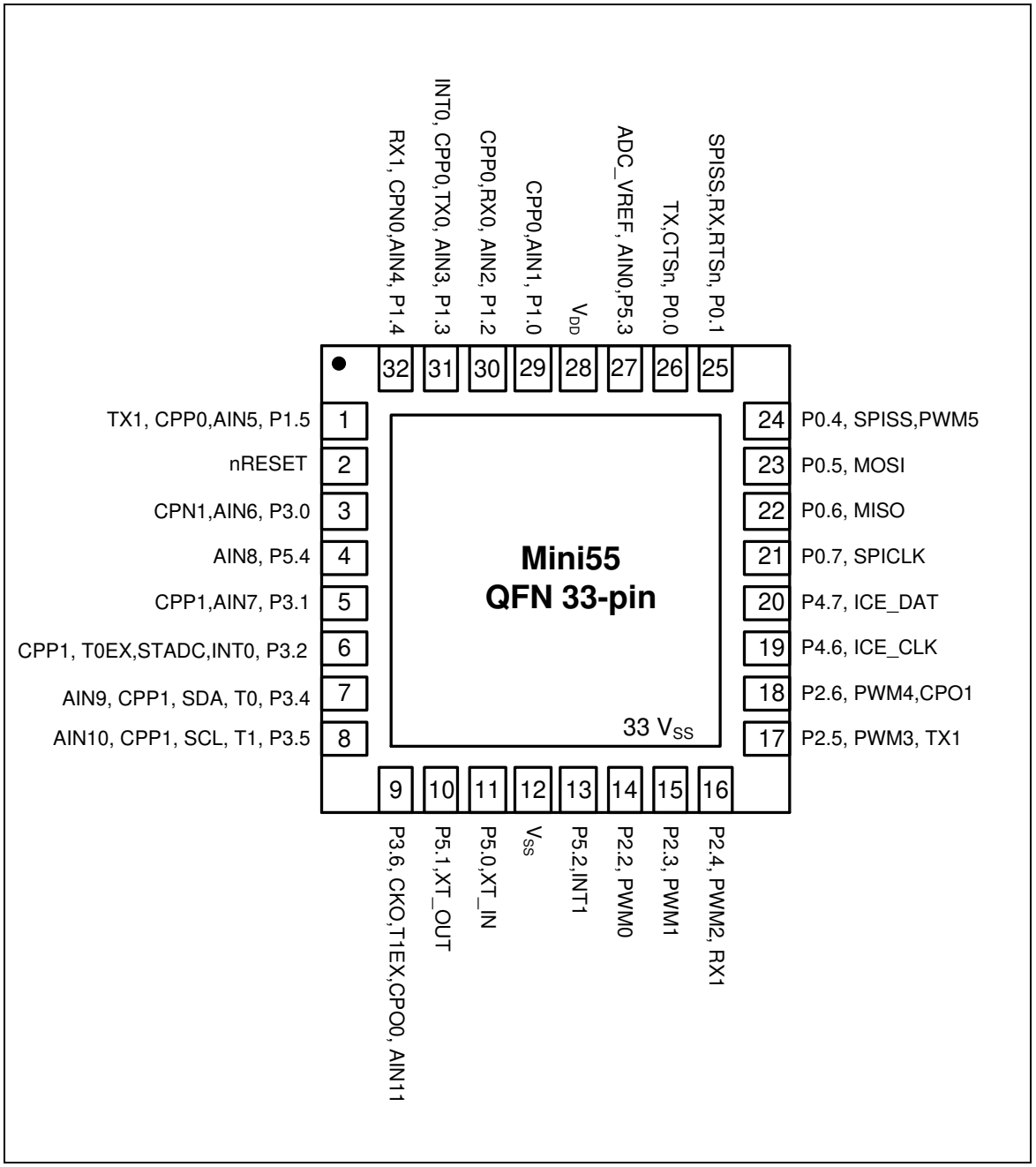

Figure 4.3-2 NuMicro® Mini55 Series QFN 33-pin Diagram

4.4 Pin Description

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
1		NC		Not connected
2	1	P1.5	I/O	General purpose digital I/O pin
		AIN5	AI	ADC analog input pin
		ACMP0_P	AI	Analog comparator positive input pin
		TX1	O	UART1 transmitter output pin
3	2	nRESET	I(ST)	The Schmitt trigger input pin for hardware device reset. A “Low” on this pin for 768 clock counter of Internal RC 48 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	P3.0	I/O	General purpose digital I/O pin
		AIN6	AI	ADC analog input pin
		ACMP1_N	AI	Analog comparator negative input pin
5	33	AV_{SS}	AP	Ground pin for analog circuit
6	4	P5.4	I/O	General purpose digital I/O pin
		AIN8	AI	ADC analog input pin
7	5	P3.1	I/O	General purpose digital I/O pin
		AIN7	AI	ADC analog input pin
		ACMP1_P	AI	Analog comparator positive input pin
8	6	P3.2	I/O	General purpose digital I/O pin
		INT0	I	External interrupt 0 input pin
		STADC	I	ADC external trigger input pin
		T0EX	I	Timer 0 external capture/reset trigger input pin
		ACMP1_P	AI	Analog comparator positive input pin
9	7	P3.4	I/O	General purpose digital I/O pin
		T0	I/O	Timer 0 external event counter input pin
		SDA	I/O	I2C data I/O pin

		ACMP1_P	AI	Analog comparator positive input pin
		AIN9	AI	ADC analog input pin
10	8	P3.5	I/O	General purpose digital I/O pin
		T1	I/O	Timer 1 external event counter input pin
		SCL	I/O	I2C clock I/O pin
		ACMP1_P	AI	Analog comparator positive input pin
		AIN10	AI	ADC analog input pin
11		P3.7	I/O	General purpose digital I/O pin
12		NC		Not connected
13		NC		Not connected
14	9	P3.6	I/O	General purpose digital I/O pin
		ACMP0_O	O	Analog comparator output pin
		CKO	O	Frequency divider output pin
		T1EX	I	Timer 1 external capture/reset trigger input pin
		AIN11	AI	ADC analog input pin
15	10	P5.1	I/O	General purpose digital I/O pin
		XT_OUT	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XT_IN.
16	11	P5.0	I/O	General purpose digital I/O pin
		XT_IN	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12 33	V_{SS}	P	Ground pin for digital circuit
18		LDO_CAP	P	LDO output pin
19		P5.5	I/O	General purpose digital I/O pin User program must enable pull-up resistor in the QFN-33 package.
20	13	P5.2	I/O	General purpose digital I/O pin
		INT1	I	External interrupt 1 input pin
21		NC		Not connected
22	14	P2.2	I/O	General purpose digital I/O pin

		PWM0	O	PWM0 output of PWM unit
23	15	P2.3	I/O	General purpose digital I/O pin
		PWM1	O	PWM1 output of PWM unit
24	16	P2.4	I/O	General purpose input/output digital pin
		PWM2	O	PWM2 output of PWM unit
		RX1	I	UART1 data receiver input pin
25	17	P2.5	I/O	General purpose digital I/O pin
		PWM3	O	PWM3 output of PWM unit
		TX1	O	UART1 transmitter output pin
26	18	P2.6	I/O	General purpose digital I/O pin
		PWM4	O	PWM4 output of PWM unit
		ACMP1_O	O	Analog comparator output pin
27		P2.7	I/O	General purpose digital I/O pin
28		NC		Not connected
29	19	P4.6	I/O	General purpose digital I/O pin
		ICE_CLK	I	Serial wired debugger clock pin
30	20	P4.7	I/O	General purpose digital I/O pin
		ICE_DAT	I/O	Serial wired debugger data pin
31		NC		Not connected
32	21	P0.7	I/O	General purpose digital I/O pin
		SPICLK	I/O	SPI serial clock pin
33	22	P0.6	I/O	General purpose digital I/O pin
		MISO	I/O	SPI MISO (master in/slave out) pin
34	23	P0.5	I/O	General purpose digital I/O pin
		MOSI	O	SPI MOSI (master out/slave in) pin
35	24	P0.4	I/O	General purpose digital I/O pin
		SPISS	I/O	SPI slave select pin
		PWM5	O	PWM5 output of PWM unit
36		NC		Not connected
37	25	P0.1	I/O	General purpose digital I/O pin
		RTSn	O	UART0 RTS pin

		RX0	I	UART0 data receiver input pin
		SPISS	I/O	SPI slave select pin
38	26	P0.0	I/O	General purpose digital I/O pin
		CTSn	I	UART0 CTS pin
		TX0	O	UART0 transmitter output pin
39		NC		Not connected
40		NC		Not connected
41	27	P5.3	I/O	General purpose digital I/O pin
		AIN0	AI	ADC analog input pin
		ADC VREF	AI	External voltage reference of ADC
42	28	V_{DD}	P	Power supply for digital circuit
43		AV_{DD}	P	Power supply for analog circuit
44	29	P1.0	I/O	General purpose digital I/O pin
		AIN1	AI	ADC analog input pin
		ACMP0_P	AI	Analog comparator positive input pin
45	30	P1.2	I/O	General purpose digital I/O pin
		AIN2	AI	ADC analog input pin
		RX	I	UART data receiver input pin
		ACMP0_P	AI	Analog comparator positive input pin
46	31	P1.3	I/O	General purpose digital I/O pin
		AIN3	AI	ADC analog input pin
		TX	O	UART transmitter output pin
		ACMP0_P	AI	Analog comparator positive input pin
		INT0	I	External interrupt 0 input pin
47	32	P1.4	I/O	General purpose digital I/O pin
		AIN4	I/O	PWM5: PWM output/Capture input
		ACMP0_N	AI	Analog comparator negative input pin
		RX1	I	UART1 data receiver input pin
48		P1.6	I/O	General purpose digital I/O pin

Table 4.4-1 NuMicro® Mini55 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 BLOCK DIAGRAM

5.1 NuMicro® Mini55 Block Diagram

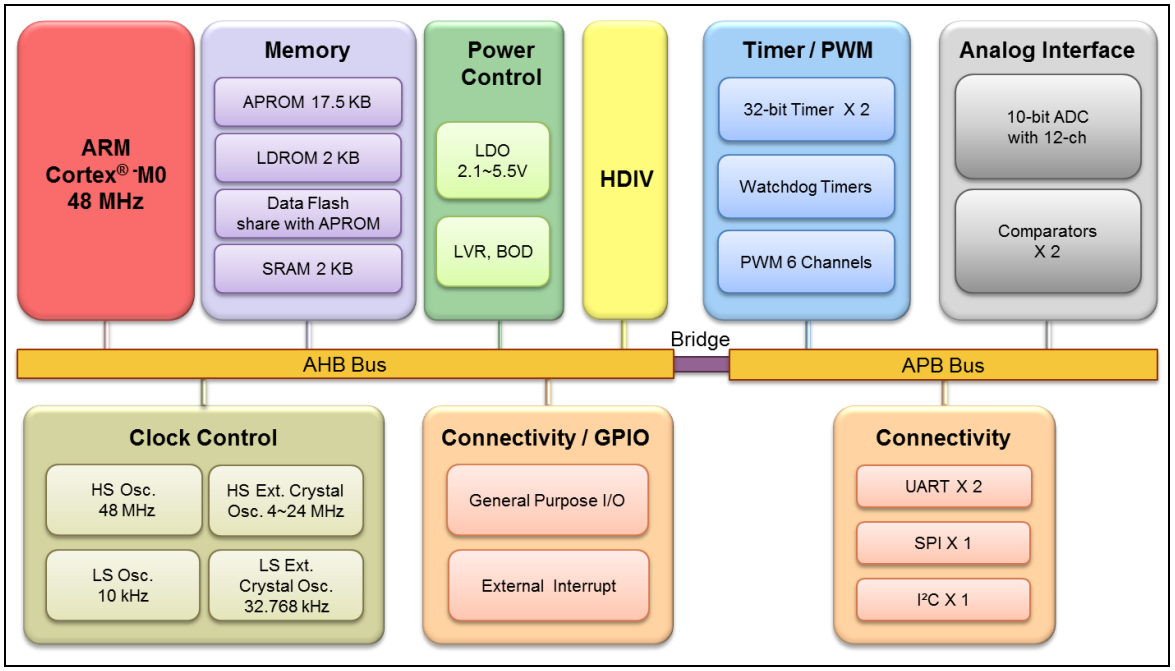

Figure 5.1-1 NuMicro® Mini55 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

6.1.1 Overview

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of the processor.

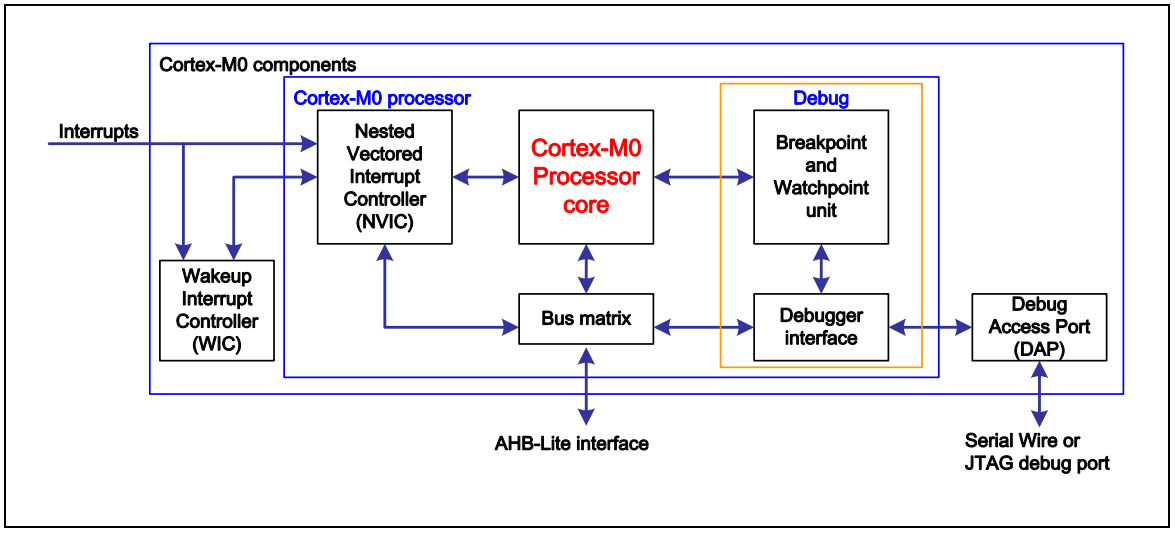

Figure 6.1-1 Functional Block Diagram

6.1.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset events flags can be read by SYS_RSTSTS register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - CPU Reset
    - Write 1 to CPURST (SYS_IPRST0[1])
  - Whole Chip Reset
    - Write 1 to SYSRESETREQ (SYS_AIRCR[2])
    - Write 1 to CHIPRST (SYS_IPRST0[0])

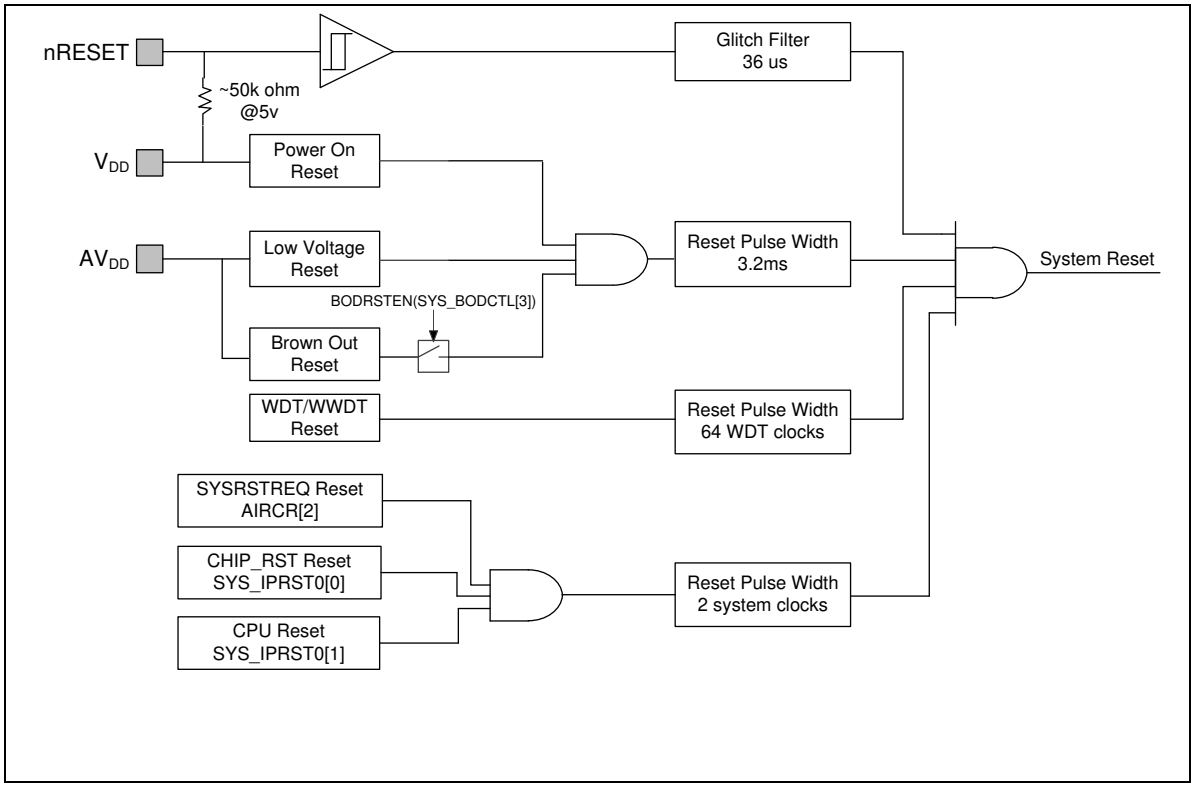

Figure 6.2-1 System Rese Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex-M0 only; the other reset sources will reset Cortex-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	0x001	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])								
BODRSTEN (SYS_BODCTL[3])								
XTLEN (CLK_PWRCTL[1:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x8	0x8	0x8	0x8	0x8	0x8	0x8	-
WDTSEL	0x3	0x3	-	-	-	-	-	-

(CLK_CLKSEL1[1:0])								
XLTSTB **(CLK_STATUS[0])**	0x0	-	-	-	-	-	-	-
LIRCSTB **(CLK_STATUS[3])**	0x0							
HIRCSTB **(CLK_STATUS[4])**	0x0	-	-	-	-	-	-	-
CLKSFAIL **(CLK_STATUS[7])**	0x0	0x0	-	-	-	-	-	-
WDT_CTL	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
BS **(FMC_ISPCTL[1])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
ISPEN **(FMC_ISPCTL[16])**								
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS **(FMC_ISPSTS[2:1])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP **(FMC_ISPSTS[20:9])**	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.