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## K20 Sub-Family

Supports the following:

MK20DN32VLF5, MK20DX32VLF5,  
MK20DN64VLF5, MK20DX64VLF5,  
MK20DN128VLF5, MK20DX128VLF5,  
MK20DN32VFT5, MK20DX32VFT5,  
MK20DN64VFT5, MK20DX64VFT5,  
MK20DN128VFT5, MK20DX128VFT5

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 50 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 128 KB program flash.
  - Up to 32 KB FlexNVM on FlexMemory devices
  - 2 KB FlexRAM on FlexMemory devices
  - Up to 16 KB RAM
  - Serial programming interface (EzPort)
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 4-channel DMA controller, supporting up to 41 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip
- Analog modules
  - 16-bit SAR ADC
  - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two-channel quadrature decoder/general purpose timer
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - SPI module
  - I2C module
  - Three UART modules
  - I2S module

## K20P48M50SF0



Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: PK20 and MK20 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K20</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

## Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"><li>• 32 = 32 KB</li><li>• 64 = 64 KB</li><li>• 128 = 128 KB</li><li>• 256 = 256 KB</li><li>• 512 = 512 KB</li><li>• 1M0 = 1 MB</li></ul>
R	Silicon revision	<ul style="list-style-type: none"><li>• Z = Initial</li><li>• (Blank) = Main</li><li>• A = Revision after main</li></ul>
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• V = -40 to 105</li><li>• C = -40 to 85</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• FM = 32 QFN (5 mm x 5 mm)</li><li>• FT = 48 QFN (7 mm x 7 mm)</li><li>• LF = 48 LQFP (7 mm x 7 mm)</li><li>• LH = 64 LQFP (10 mm x 10 mm)</li><li>• MP = 64 MAPBGA (5 mm x 5 mm)</li><li>• LK = 80 LQFP (12 mm x 12 mm)</li><li>• MB = 81 MAPBGA (8 mm x 8 mm)</li><li>• LL = 100 LQFP (14 mm x 14 mm)</li><li>• ML = 104 MAPBGA (8 mm x 8 mm)</li><li>• MC = 121 MAPBGA (8 mm x 8 mm)</li><li>• LQ = 144 LQFP (20 mm x 20 mm)</li><li>• MD = 144 MAPBGA (13 mm x 13 mm)</li><li>• MJ = 256 MAPBGA (17 mm x 17 mm)</li></ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"><li>• 5 = 50 MHz</li><li>• 7 = 72 MHz</li><li>• 10 = 100 MHz</li><li>• 12 = 120 MHz</li><li>• 15 = 150 MHz</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li><li>• (Blank) = Trays</li></ul>

## 2.4 Example

This is an example part number:

MK20DN32VLF5

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

### 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

#### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

### 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

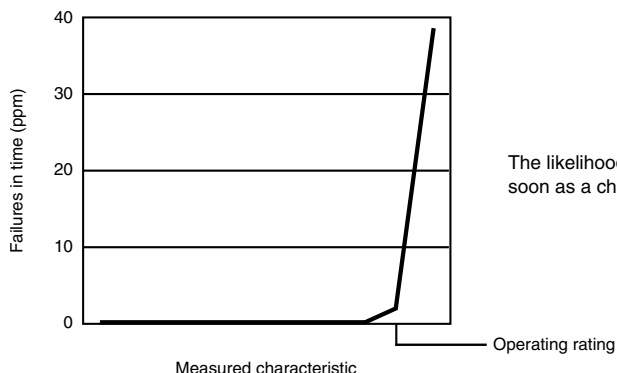
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

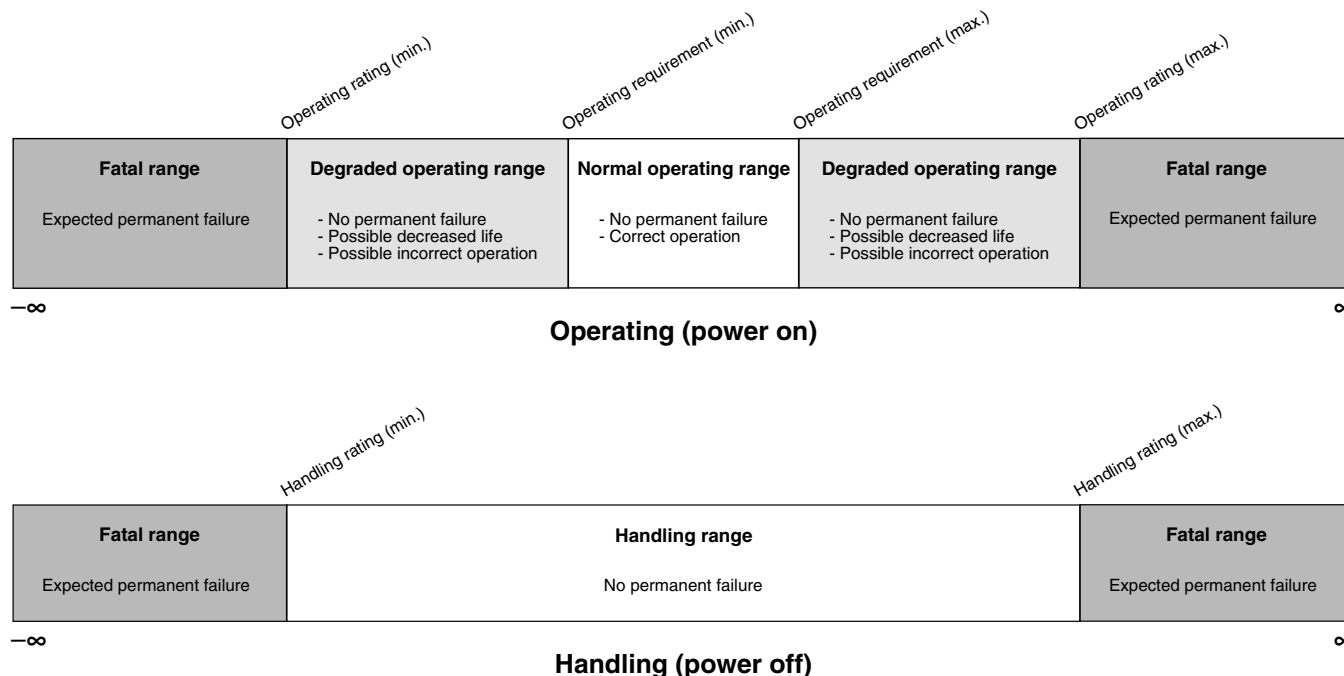
Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	−0.3	1.2	V

## 3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

### 3.6 Relationship between ratings and operating requirements



### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.



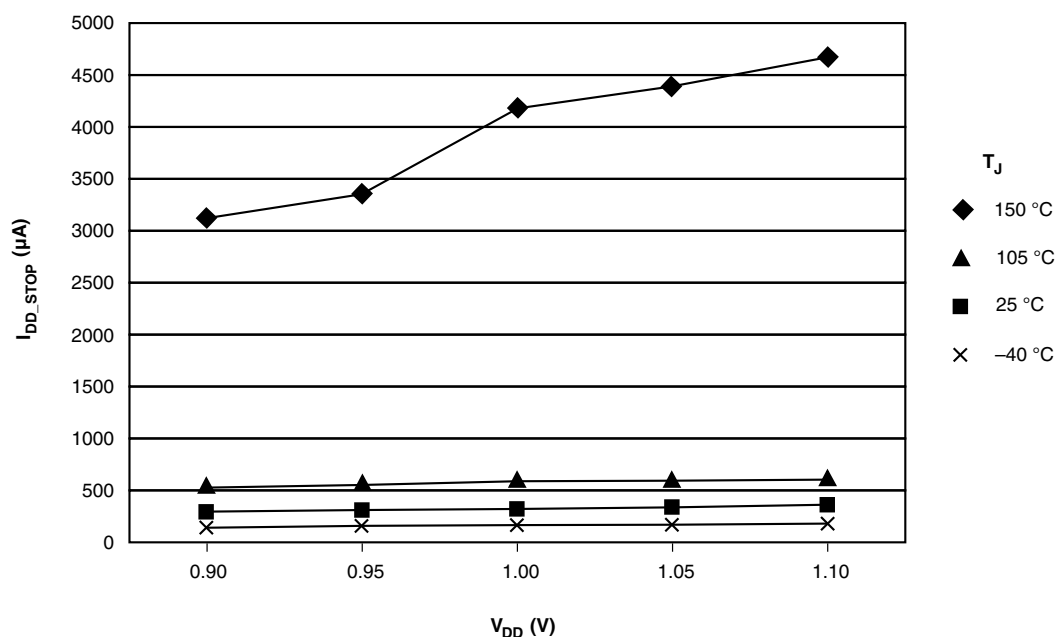
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
$T_A$	Ambient temperature	25	°C
$V_{DD}$	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	–55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	–100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

### 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	–0.3	3.8	V

Table continues on the next page...

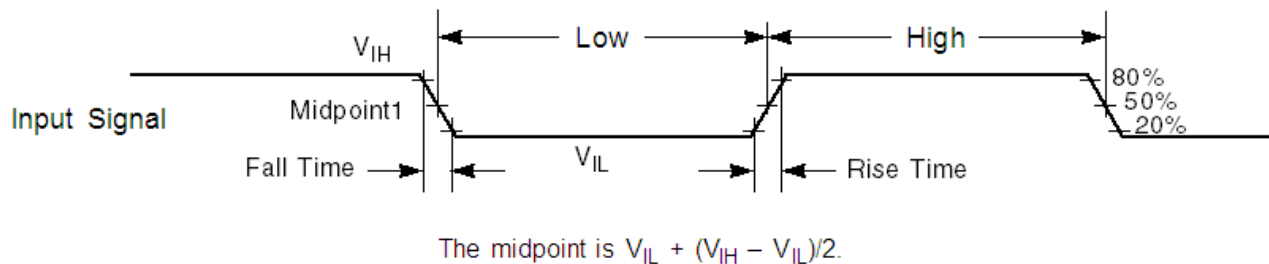
Symbol	Description	Min.	Max.	Unit
$I_{DD}$	Digital supply current	—	155	mA
$V_{DIO}$	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB\_DP}$	USB_DP input voltage	-0.3	3.63	V
$V_{USB\_DM}$	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

### 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
  - have  $C_L=30\text{pF}$  loads,
  - are configured for fast slew rate ( $\text{PORTx\_PCRn[SRE]}=0$ ), and
  - are configured for high drive strength ( $\text{PORTx\_PCRn[DSE]}=1$ )
2. input pins
  - have their passive filter disabled ( $\text{PORTx\_PCRn[PFE]}=0$ )

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{BAT}$	RTC battery supply voltage	1.71	3.6	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{ICIO}$	I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math> (Negative current injection)</li> <li><math>V_{IN} &gt; V_{DD}+0.3\text{V}</math> (Positive current injection)</li> </ul>	-3 —	— +3	mA	1
$I_{ICcont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	$V_{POR\_VBAT}$	—	V	

1. All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  ( $=V_{SS}-0.3\text{V}$ ) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$  ( $=V_{DD}+0.3\text{V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub> V <sub>LVW2H</sub> V <sub>LVW3H</sub> V <sub>LVW4H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub> V <sub>LVW2L</sub> V <sub>LVW3L</sub> V <sub>LVW4L</sub>	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	1
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -9\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$	—	V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OL}$	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 9\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 3\text{ mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 2\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 0.6\text{ mA}$	—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	$\mu\text{A}$	1
	• @ 25 °C	—	0.1	$\mu\text{A}$	
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$I_{OZ}$	Total Hi-Z (off-state) leakage current (all input pins)	—	4	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	22	50	k $\Omega$	2
$R_{PD}$	Internal pulldown resistors	22	50	k $\Omega$	3

1. Tested by ganged leakage method

2. Measured at  $V_{input} = V_{SS}$

3. Measured at  $V_{input} = V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz



**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu s$	1
	• VLLS0 → RUN	—	130	$\mu s$	
	• VLLS1 → RUN	—	130	$\mu s$	
	• VLLS2 → RUN	—	70	$\mu s$	
	• VLLS3 → RUN	—	70	$\mu s$	
	• LLS → RUN	—	6	$\mu s$	
	• VLPS → RUN	—	5.2	$\mu s$	
	• STOP → RUN	—	5.2	$\mu s$	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash	—	13.7	15.1	mA	2
		—	13.9	15.3	mA	
$I_{DD\_RUN}$	Run mode current — all peripheral clocks enabled, code executing from flash	—	16.1	18.2	mA	3, 4
		—	16.3	17.7	mA	
		—	16.7	18.4	mA	
		—	16.7	18.4	mA	
$I_{DD\_WAIT}$	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	8.4	mA	2
$I_{DD\_WAIT}$	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	6.4	mA	5

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	867	—	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	—	509	—	μA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	310	426	μA	
		—	384	458	μA	
		—	629	1100	μA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	3.5	22.6	μA	
		—	20.7	52.9	μA	
		—	85	220	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	2.1	3.7	μA	
		—	7.7	43.1	μA	
		—	32.2	68	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	1.5	2.9	μA	
		—	4.8	22.5	μA	
		—	20	37.8	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	1.4	2.8	μA	
		—	4.1	19.2	μA	
		—	17.3	32.4	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.678	1.3	μA	
		—	2.8	13.6	μA	
		—	13.6	24.5	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.367	1.0	μA	
		—	2.4	13.3	μA	
		—	13.2	24.1	μA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD\_VLLS0}$	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	— — —	0.176 2.2 13	0.859 13.1 23.9	μA μA μA	
$I_{DD\_VBAT}$	Average current with RTC and 32kHz disabled at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	— — —	0.19 0.49 2.2	0.22 0.64 3.2	μA μA μA	
$I_{DD\_VBAT}$	Average current when CPU is not accessing RTC registers <ul style="list-style-type: none"> <li>• @ 1.8V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul> </li> <li>• @ 3.0V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul> </li> </ul>	— — — — — — —	0.57 0.90 2.4 0.67 1.0 2.7	0.67 1.2 3.5 0.94 1.4 3.9	μA μA μA μA μA μA	9

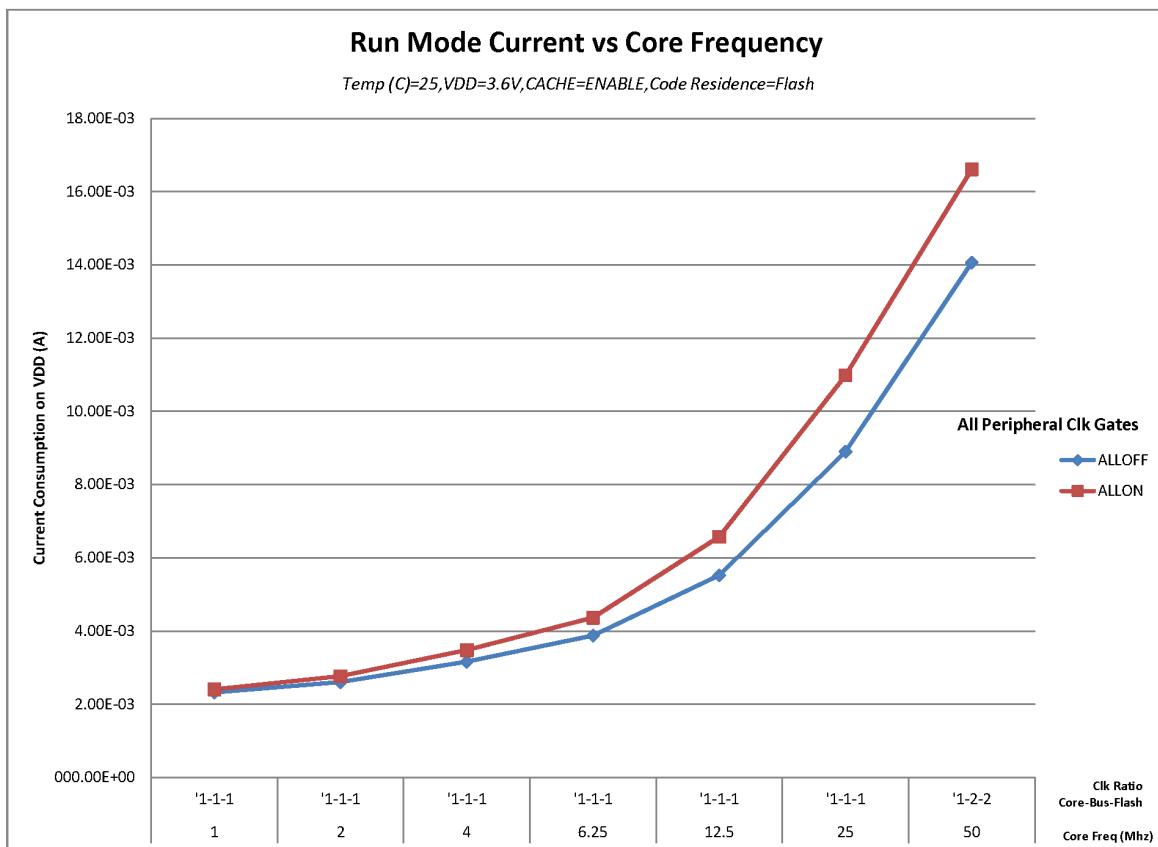
1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical $I_{DD\_RUN}$ operating behavior

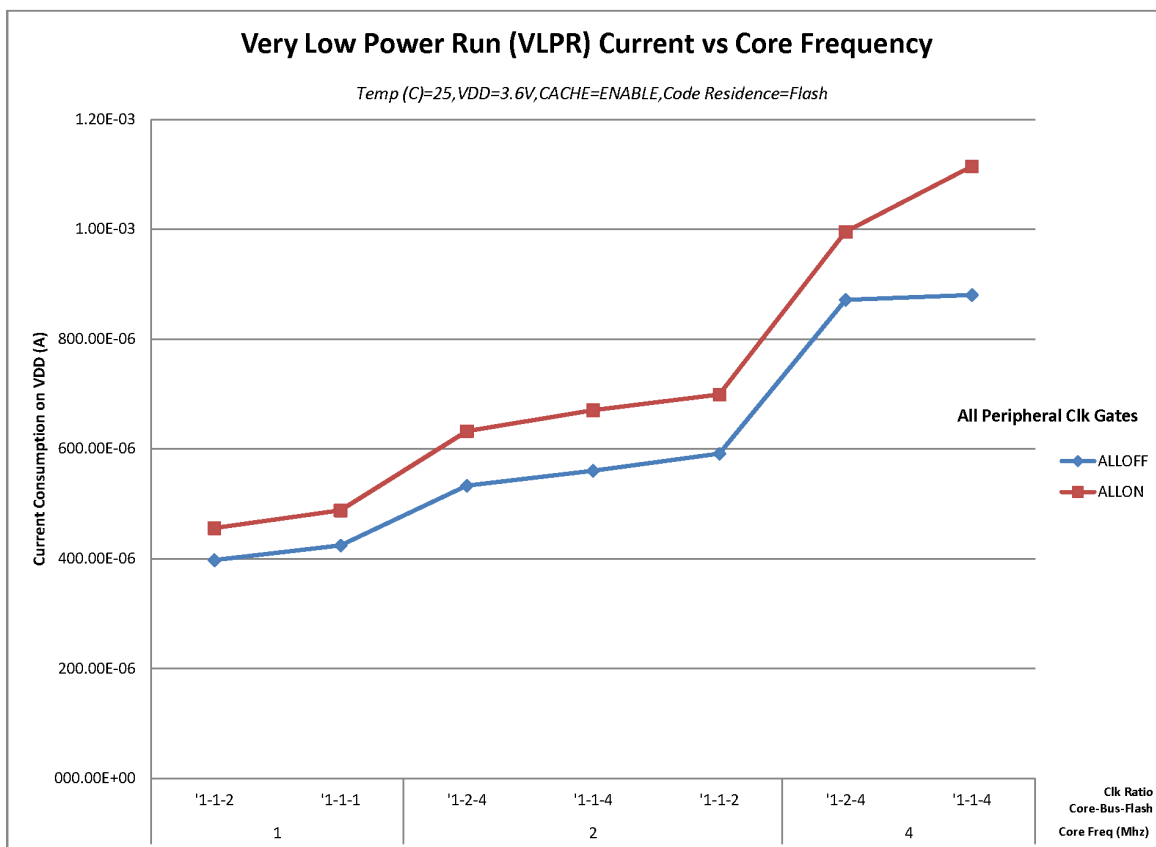
The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



**Figure 2. Run mode supply current vs. core frequency**



**Figure 3. VLPR mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

**Table 7. EMC radiated emissions operating behaviors for 64LQFP**

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	19	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	21	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	19	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	11	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $f_{OSC} = 12\text{ MHz}$  (crystal),  $f_{SYS} = 48\text{ MHz}$ ,  $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	50	MHz	
$f_{SYS\_USB}$	System and core clock when Full Speed USB in operation	20	—	MHz	
$f_{BUS}$	Bus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	

Table continues on the next page...



**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$f_{FLASH}$	Flash clock	—	1	MHz	
$f_{ERCLK}$	External reference clock	—	16	MHz	
$f_{LPTMR\_pin}$	LPTMR clock	—	25	MHz	
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz	
$f_{I2S\_MCLK}$	I2S master clock	—	12.5	MHz	
$f_{I2S\_BCLK}$	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I<sup>2</sup>C signals.

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>Slew disabled <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>Slew enabled <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— — — —	13  7 36 24	ns ns ns ns	4

Table continues on the next page...

**Table 10. General switching specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	<ul style="list-style-type: none"> <li>Slew disabled <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>Slew enabled <ul style="list-style-type: none"> <li><math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li><math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	12	ns	
		—	6	ns	
		—	36	ns	
		—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	−40	125	°C
$T_A$	Ambient temperature	−40	105	°C

### 5.4.2 Thermal attributes

Board type	Symbol	Description	48 LQFP	48 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	70	81	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	47	28	°C/W	1, 3

Table continues on the next page...

## Peripheral operating requirements and behaviors

Board type	Symbol	Description	48 LQFP	48 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	58	66	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	40	23	°C/W	,
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	11	°C/W	5
—	$R_{\theta JC}$	Thermal resistance, junction to case	18	1.4	°C/W	6
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
5. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
6. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
7. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

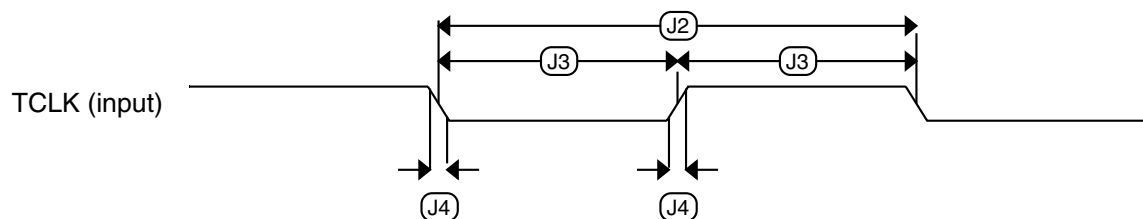
### 6.1 Core modules

## 6.1.1 JTAG electricals

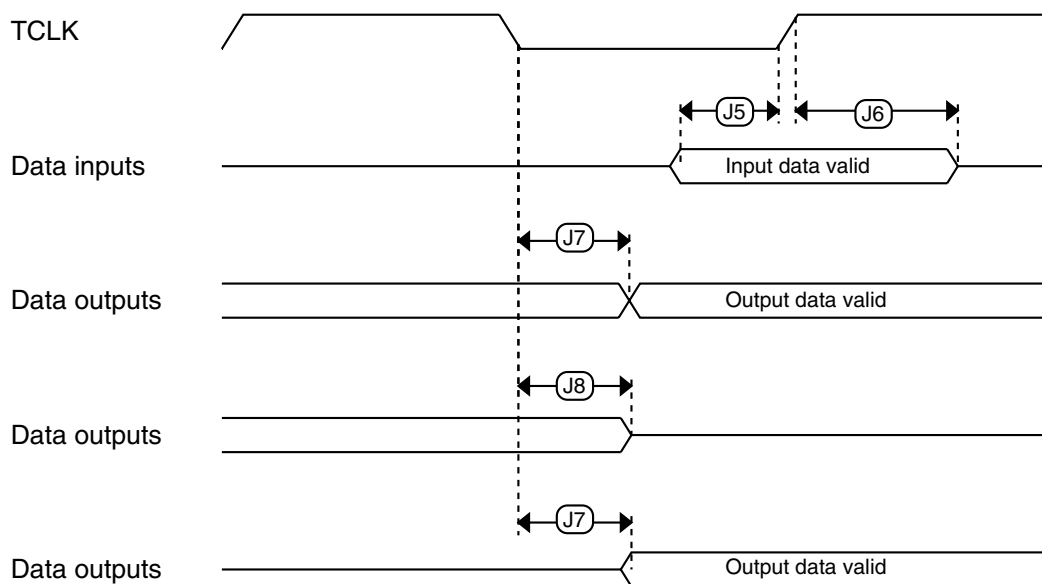
**Table 12. JTAG voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	— —	10 5	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	100 200	— —	ns ns ns
J4	TCLK rise and fall times	—	1	ns
J5	TMS input data setup time to TCLK rise <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	53 112	— —	ns
J6	TDI input data setup time to TCLK rise	8	—	ns
J7	TMS input data hold time after TCLK rise <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li></ul>	3.4 3.4	— —	ns
J8	TDI input data hold time after TCLK rise	3.4	—	ns
J9	TCLK low to TMS data valid <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	— —	48 85	ns
J10	TCLK low to TDO data valid	—	48	ns
J11	Output data hold/invalid time after clock edge <sup>1</sup>	—	3	ns

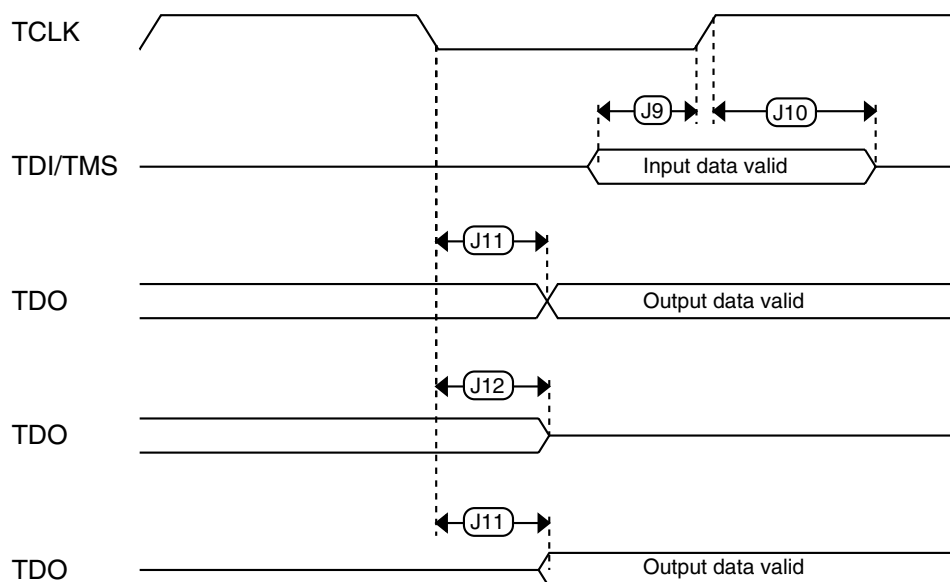
1. They are common for JTAG and CJTAG. Input transition = 1 ns and Output load = 50pf



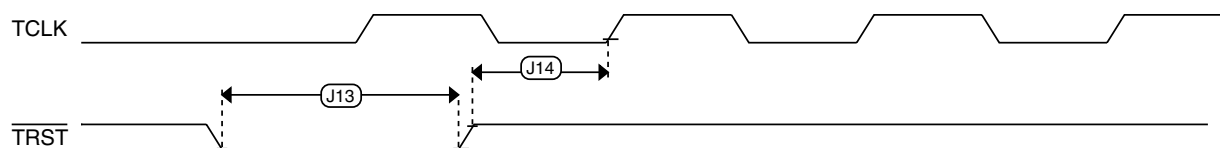
**Figure 4. Test clock input timing**



**Figure 5. Boundary scan (JTAG) timing**



**Figure 6. Test Access Port timing**

Figure 7.  $\overline{\text{TRST}}$  timing

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

Table 13. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints\_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints\_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	$\pm 0.3$	$\pm 0.6$	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	$\pm 3$	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	$\pm 0.3$	—	$\%f_{\text{dco}}$	1
$f_{\text{intf\_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf\_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc\_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints\_t}}$	—	—	kHz	
$f_{\text{loc\_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints\_t}}$	—	—	kHz	
FLL						

Table continues on the next page...