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## K21P80M50SF4



### K21 Sub-Family

Supports the following:

MK21DX128VLK5, MK21DX256VLK5,  
MK21DN512VLK5

#### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 50 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 512 KB of program flash for devices without FlexNVM.
  - Up to 256 KB program flash for devices with FlexNVM.
  - 64 KB FlexNVM on FlexMemory devices
  - 4 KB FlexRAM on FlexMemory devices
  - Up to 64 KB RAM
  - Serial programming interface (EzPort)
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 16-channel DMA controller, supporting up to 63 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - Tamper detect and secure storage
  - Hardware random-number generator
  - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC
  - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two 2-channel general purpose timers, one with quadrature decoder functionality
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect
  - Two SPI modules
  - Two I2C modules
  - Four UART modules
  - I2S module

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: PK21 and MK21 .

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K21</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

## Part identification

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>• 32 = 32 KB</li> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> <li>• 512 = 512 KB</li> <li>• 1M0 = 1 MB</li> <li>• 2M0 = 2 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>• Z = Initial</li> <li>• (Blank) = Main</li> <li>• A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>• V = -40 to 105</li> <li>• C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 5 = 50 MHz</li> <li>• 7 = 72 MHz</li> <li>• 10 = 100 MHz</li> <li>• 12 = 120 MHz</li> <li>• 15 = 150 MHz</li> <li>• 18 = 180 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK21DX128VLK5

## 2.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
##	Kinetis family	<ul style="list-style-type: none"> <li>1# = K11/K12</li> <li>2# = K21/K22</li> </ul>
C	Speed	<ul style="list-style-type: none"> <li>G = 50 MHz</li> </ul>
F	Flash memory configuration	<ul style="list-style-type: none"> <li>G = 128 KB + Flex</li> <li>H = 256 KB + Flex</li> <li>9 = 512 KB</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>MC = 121 MAPBGA</li> </ul>

This table lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK21DX128VMC5	M21GGVMC
MK21DX256VMC5	M21GHVMC
MK21DN512VMC5	M21G9VMC

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

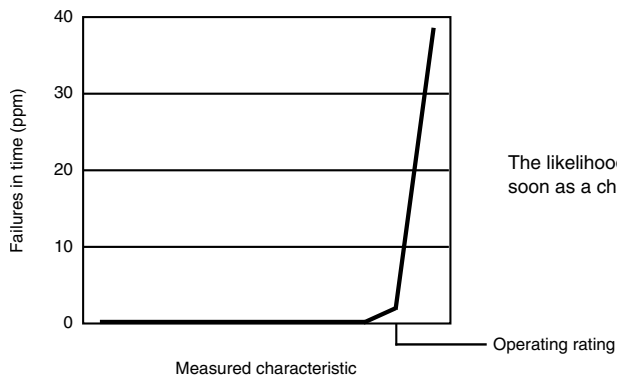
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

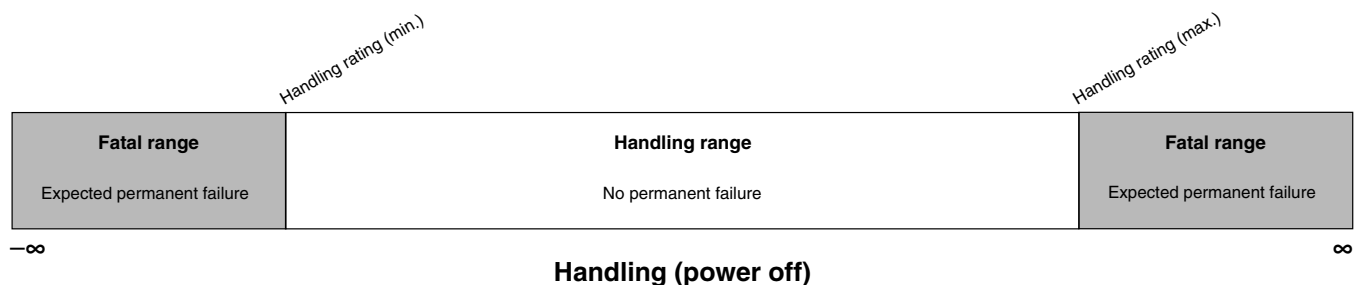
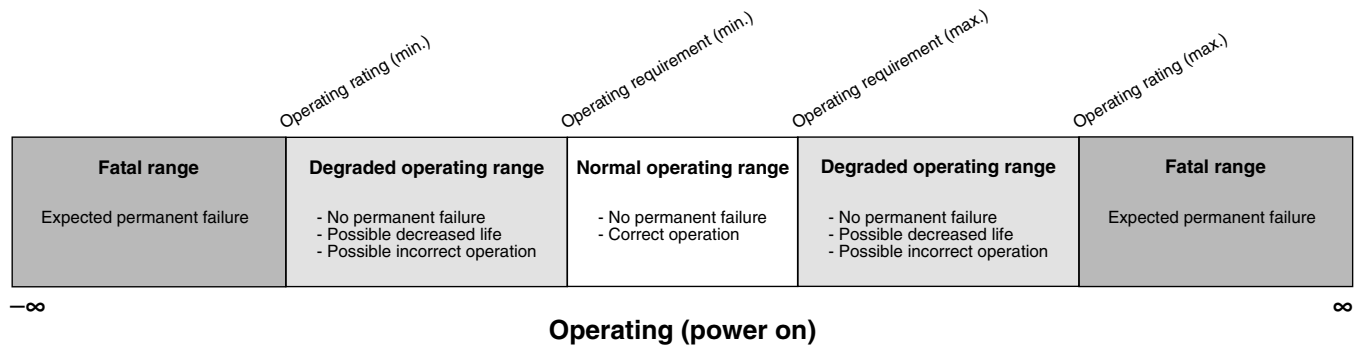
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



### 3.6 Relationship between ratings and operating requirements





### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

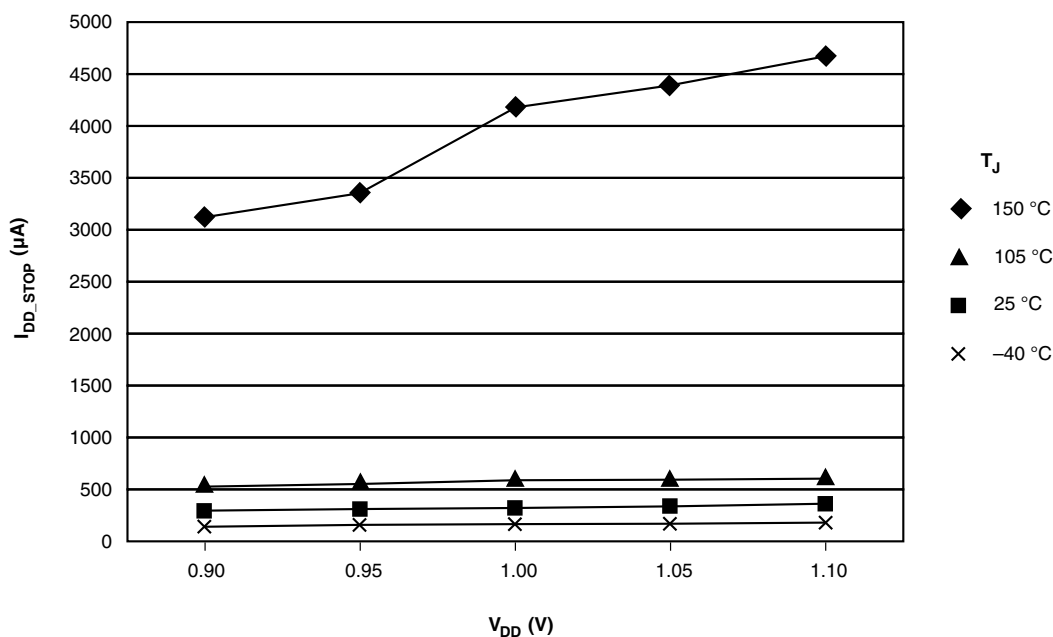
#### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

#### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



### 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	155	mA
V <sub>DIO</sub>	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3		V
V <sub>AIO</sub>	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	V <sub>DD</sub> + 0.3	V
I <sub>D</sub>	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V <sub>DDA</sub>	Analog supply voltage	V <sub>DD</sub> - 0.3	V <sub>DD</sub> + 0.3	V
V <sub>USB0_DP</sub>	USB0_DP input voltage	-0.3	3.63	V
V <sub>USB0_DM</sub>	USB0_DM input voltage	-0.3	3.63	V
V <sub>REGIN</sub>	USB regulator input	-0.3	6.0	V
V <sub>BAT</sub>	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

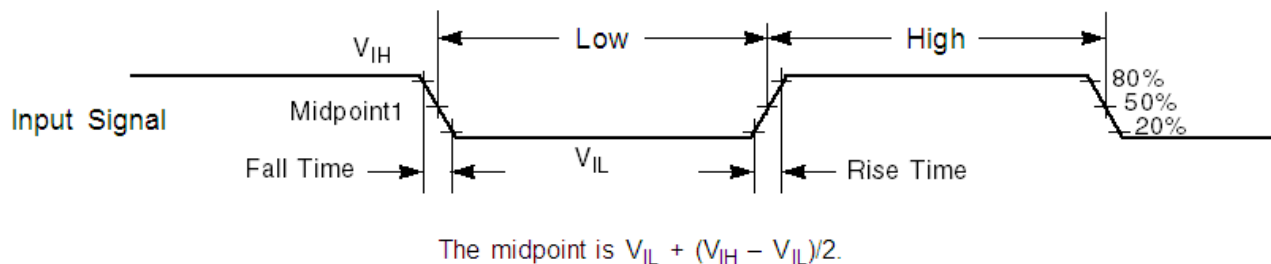


Figure 1. Input signal measurement reference

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{BAT}$	RTC battery supply voltage	1.71	3.6	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	—	V V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	—	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{CIO}$	I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math> (Negative current injection)</li> <li><math>V_{IN} &gt; V_{DD}+0.3\text{V}</math> (Positive current injection)</li> </ul>	-3 —	— +3	mA	1

Table continues on the next page...

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$I_{Ccont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	$V_{POR\_VBAT}$	—	V	

- All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is less than  $V_{AIO\_MIN}$  or greater than  $V_{AIO\_MAX}$ , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{CAIO}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{CAIO}|$ . Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

## 5.2.2 LVD and POR operating requirements

**Table 2.  $V_{DD}$  supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
$V_{LVW1H}$	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	2.62	2.70	2.78	V	1
$V_{LVW2H}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	2.72	2.80	2.88	V	
$V_{LVW3H}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	2.82	2.90	2.98	V	
$V_{LVW4H}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
$V_{LVW1L}$	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	1.74	1.80	1.86	V	1
$V_{LVW2L}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	1.84	1.90	1.96	V	
$V_{LVW3L}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	1.94	2.00	2.06	V	
$V_{LVW4L}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
$V_{BG}$	Bandgap voltage reference	0.97	1.00	1.03	V	
$t_{LPO}$	Internal low power oscillator period — factory trimmed	900	1000	1100	$\mu$ s	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

### 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — high drive strength				
	• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -9 mA	V <sub>DD</sub> - 0.5	—	V	
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -3 mA	V <sub>DD</sub> - 0.5	—	V	
	Output high voltage — low drive strength				
V <sub>OL</sub>	Output low voltage — high drive strength				
	• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 9 mA	—	0.5	V	
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
I <sub>OLT</sub>	Output low current total for all ports				
	• 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 2 mA	—	0.5	V	
	• 1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 0.6 mA	—	0.5	V	
	Output low current total for all ports	—	100	mA	
I <sub>IN</sub>	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	μA	1
	• @ 25 °C	—	0.1	μA	
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I <sub>OZ</sub>	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R <sub>PU</sub>	Internal pullup resistors	22	50	kΩ	2
R <sub>PD</sub>	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at V<sub>input</sub> = V<sub>SS</sub>
3. Measured at V<sub>input</sub> = V<sub>DD</sub>

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. <ul style="list-style-type: none"> <li>• 1.71 V / (<math>V_{DD}</math> slew rate) <math>\leq</math> 300 <math>\mu</math>s</li> <li>• 1.71 V / (<math>V_{DD}</math> slew rate) <math>&gt;</math> 300 <math>\mu</math>s</li> </ul>	—	300 1.7 V / ( $V_{DD}$ slew rate)	$\mu$ s	1
	• VLLS0 $\rightarrow$ RUN	—	135	$\mu$ s	
	• VLLS1 $\rightarrow$ RUN	—	135	$\mu$ s	
	• VLLS2 $\rightarrow$ RUN	—	85	$\mu$ s	
	• VLLS3 $\rightarrow$ RUN	—	85	$\mu$ s	
	• LLS $\rightarrow$ RUN	—	6	$\mu$ s	
	• VLPS $\rightarrow$ RUN	—	5.2	$\mu$ s	
	• STOP $\rightarrow$ RUN	—	5.2	$\mu$ s	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash <ul style="list-style-type: none"> <li>• @ 1.8 V</li> <li>• @ 3.0 V</li> </ul>	—	12.98	14	mA	2
		—	12.93	13.8	mA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8 V	—	17.04	19.3	mA	
	• @ 3.0 V					
	• @ 25°C	—	17.01	18.9	mA	
		—	19.8	21.3	mA	
I <sub>DD_WAIT</sub>	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.95	9.5	mA	2
I <sub>DD_WAIT</sub>	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.88	7.4	mA	5
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V	—			μA	
	• @ -40 to 25°C		320	436		
	• @ 50°C		360	489		
	• @ 70°C		410	620		
	• @ 105°C		610	1100		
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	754	—	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	—	437	—	μA	8
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V	—			μA	
	• @ -40 to 25°C		7.33	24.2		
	• @ 50°C		14	32		
	• @ 70°C		28	48		
	• @ 105°C		110	280		
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V	—			μA	
	• @ -40 to 25°C		3.14	4.8		
	• @ 50°C		6.48	28.3		
	• @ 70°C		13.85	44.6		
	• @ 105°C		55.53	71.3		
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V	—			μA	
	• @ -40 to 25°C		2.19	3.4		
	• @ 50°C		4.35	4.35		
	• @ 70°C		8.92	24.6		
	• @ 105°C		35.33	45.3		
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V	—			μA	
	• @ -40 to 25°C		1.77	3.1		
	• @ 50°C		2.81	13.8		
	• @ 70°C		5.20	22.3		
	• @ 105°C		19.88	34.2		

Table continues on the next page...



**Table 6. Power consumption operating behaviors (continued)**

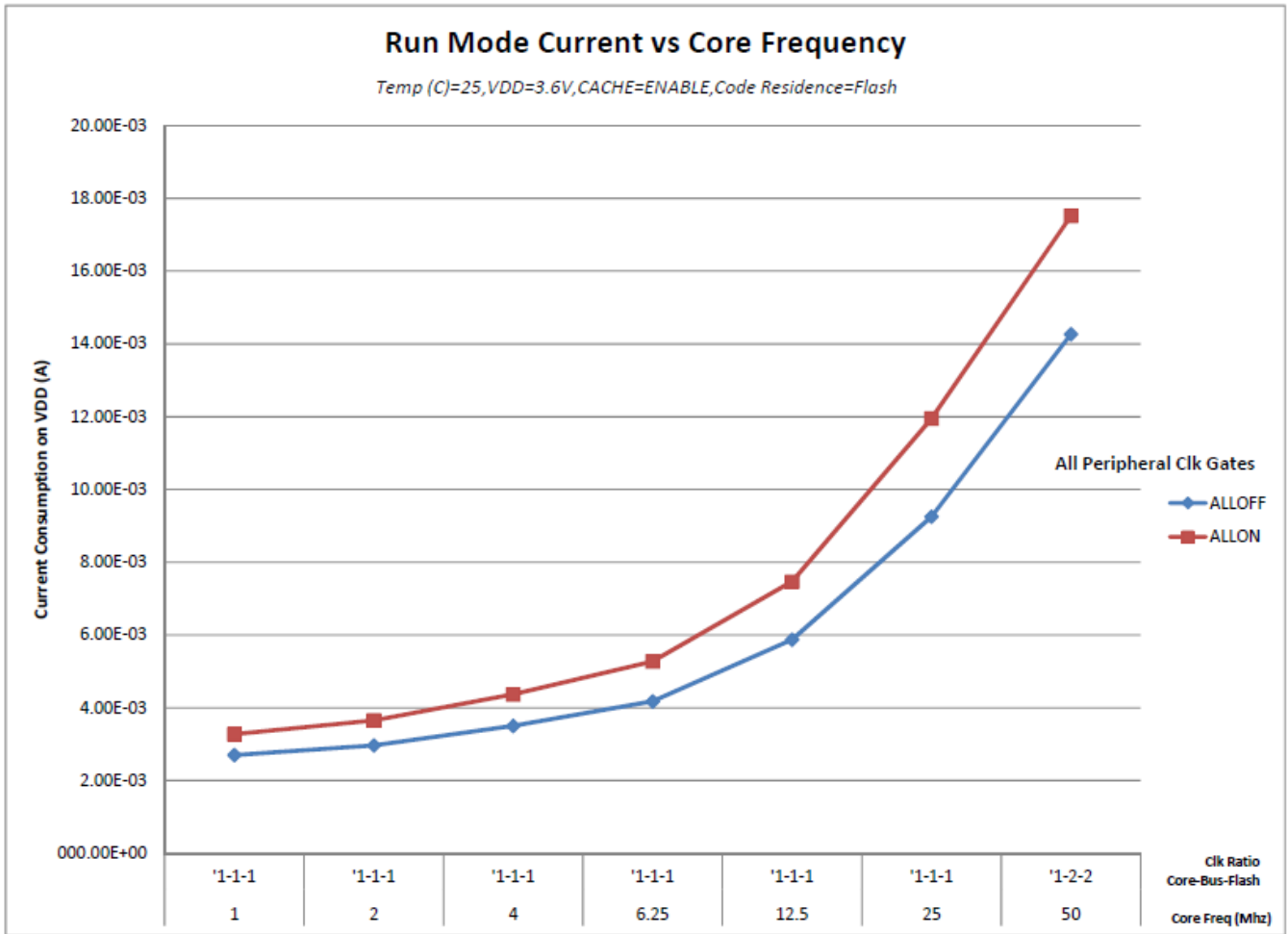
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	1.03 1.92 4.03 17.43	1.8 7.5 15.9 28.7	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.543 1.36 3.39 16.52	1.1 7.58 14.3 24.1	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.359 1.03 2.87 15.20	0.95 6.8 15.4 25.3	μA	
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.91 1.1 1.5 4.3	1.1 1.35 1.85 5.7	μA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



**Figure 2. Run mode supply current vs. core frequency**

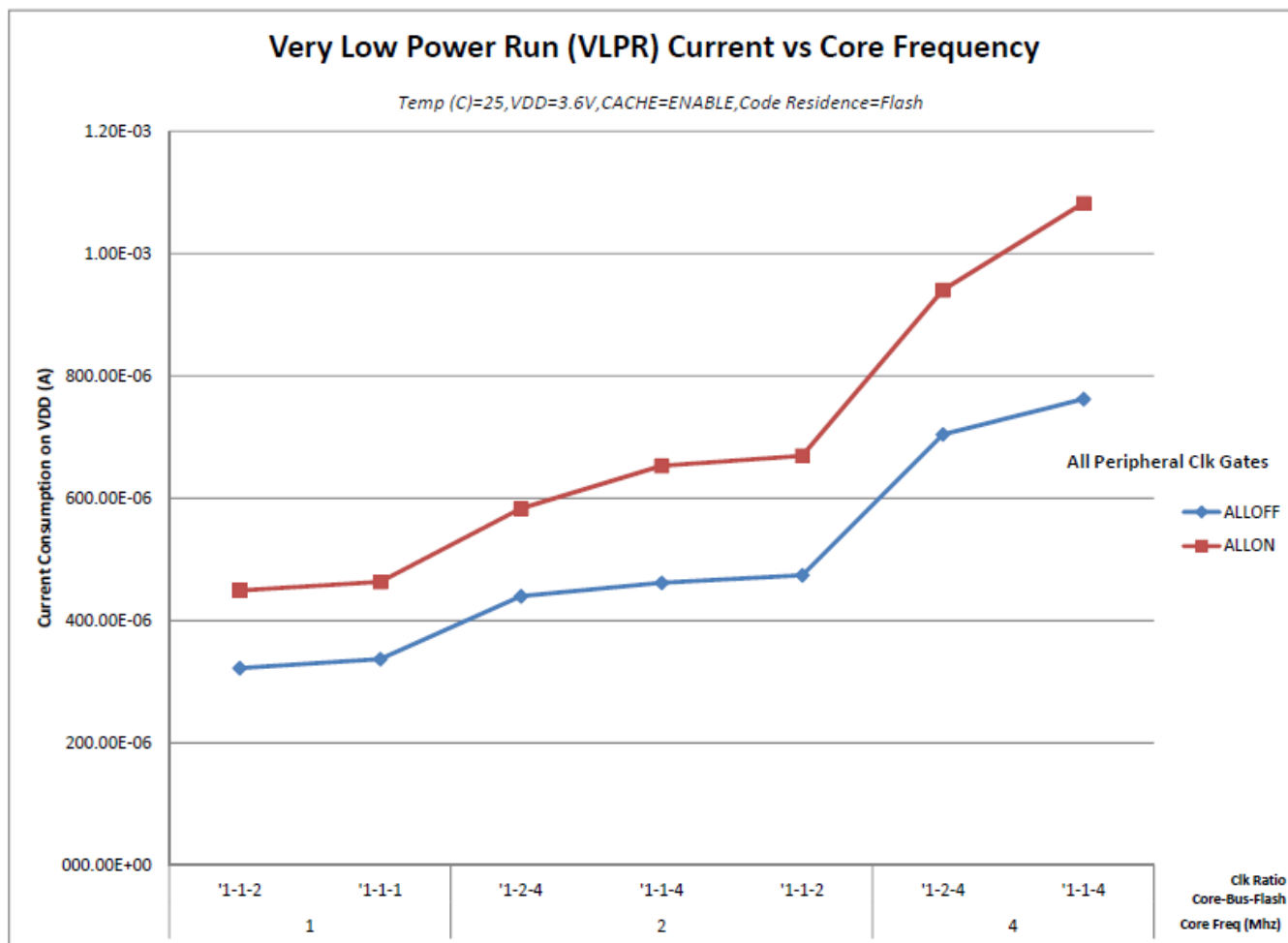


Figure 3. VLPR mode supply current vs. core frequency

## 5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors 1

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	19	dBμV	2, 3
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	21	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	19	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	11	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

3.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $f_{OSC} = 12\text{ MHz}$  (crystal),  $f_{SYS} = 48\text{ MHz}$ ,  $f_{BUS} = 48\text{ MHz}$
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 9. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	50	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
$f_{BUS}$	Bus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	
$f_{ERCLK}$	External reference clock	—	16	MHz	
$f_{LPTMR\_pin}$	LPTMR clock	—	25	MHz	

*Table continues on the next page...*

**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	
f <sub>I2S_MCLK</sub>	I2S master clock	—	12.5	MHz	
f <sub>I2S_BCLK</sub>	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	13	ns	4
		—	7	ns	
		—	36	ns	
		—	24	ns	
	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	12	ns	5
		—	6	ns	
		—	36	ns	
		—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.

3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

### 5.4.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	29	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	19	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8	°C/W	5

Table continues on the next page...

## Peripheral operating requirements and behaviors

Board type	Symbol	Description	80 LQFP	Unit	Notes
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
- Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
- Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
- Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 JTAG electricals

Table 12. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	0	10	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	50	—	ns
J4	TCLK rise and fall times	—	3	ns

Table continues on the next page...

**Table 12. JTAG limited voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

**Table 13. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns



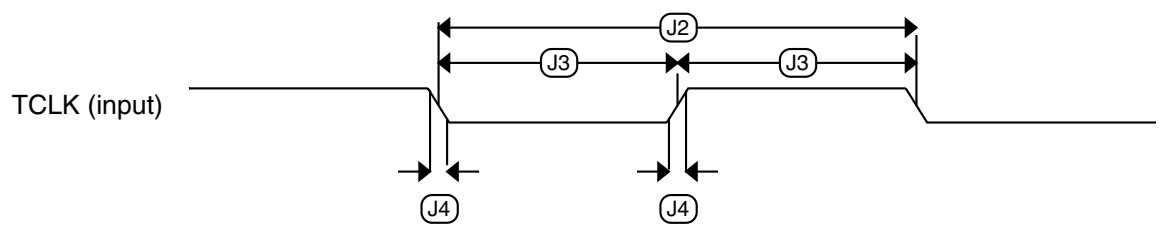


Figure 4. Test clock input timing

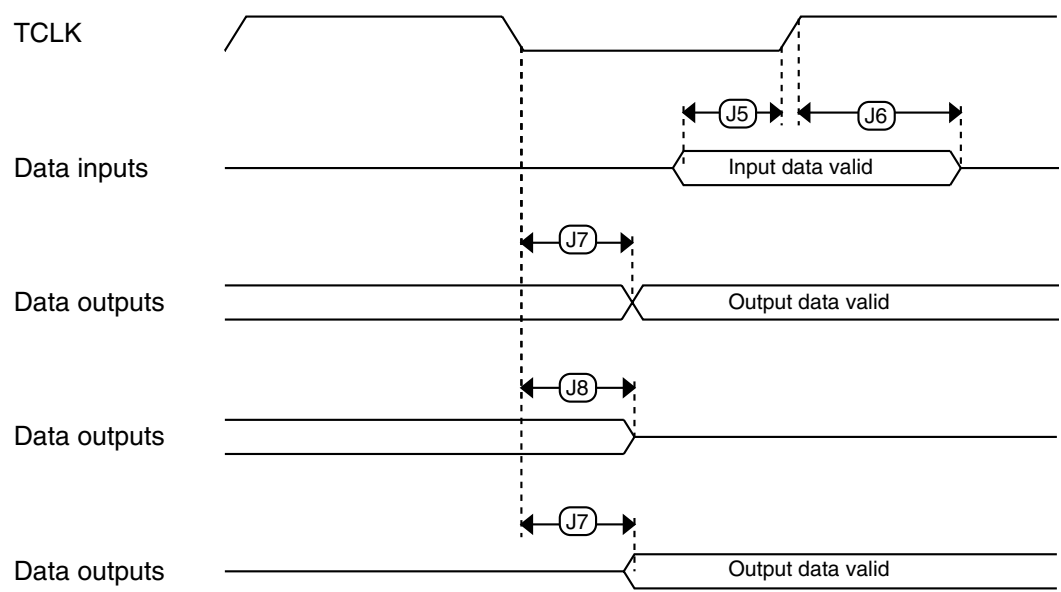


Figure 5. Boundary scan (JTAG) timing

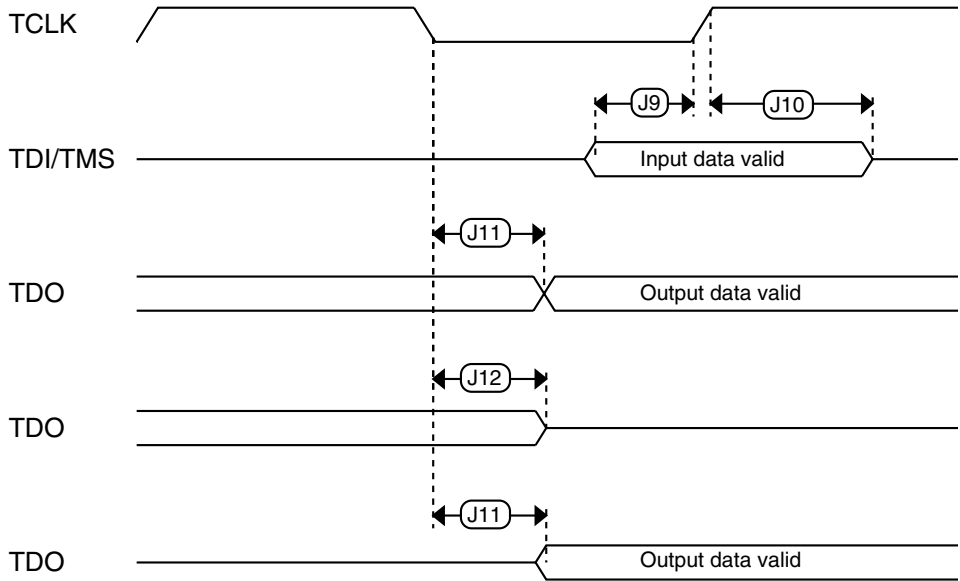


Figure 6. Test Access Port timing

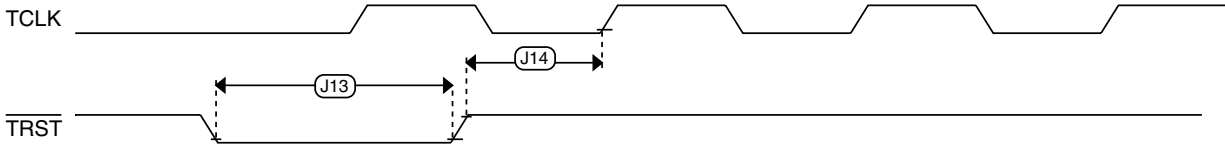


Figure 7. TRST timing

### 6.2 System modules

There are no specifications necessary for the device's system modules.

### 6.3 Clock modules