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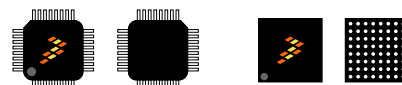
Kinetis K21F Sub-Family Data Sheet

120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K21 product family members are optimized for cost-sensitive applications requiring low-power, USB connectivity, processing efficiency with floating point unit and the need for extensive tamper protection, such as Electronic Point of Sales. It shares the comprehensive enablement and scalability of the Kinetis family. This product offers:

- Up to 1 MB of flash memory with up to 128 KB of SRAM
- Drylce Tamper Detection with active/passive pin, temperature, clock, supply voltage monitoring
- Run power consumption down to 279 μ A/MHz. Static power consumption down to 5.1 μ A with full state retention and 5 μ s wakeup. Lowest Static mode down to 268 nA
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator

MK21FX512VLQ12
MK21FN1M0VLQ12
MK21FX512VMD12
MK21FN1M0VMD12



144 LQFP 20 x 20 x 1.6 mm Pitch 0.5 mm
144 BGA 13 x 13 x 1.7 mm Pitch 1 mm

Performance

- Up to 120 MHz ARM Cortex-M4-based core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

Memories and memory interfaces

- Up to 1 MB program flash memory and 128 KB RAM
- Up to 128 KB FlexNVM and 4 KB FlexRAM on FlexMemory devices
- FlexBus external bus interface

System peripherals

- Multiple low-power modes; low leakage wakeup unit
- Memory protection unit with multi-master protection
- 16-channel DMA controller
- External watchdog monitor and software watchdog

Security and integrity modules

- Hardware CRC module
- Tamper detect and secure storage
- Hardware random-number generator
- Hardware encryption
- 128-bit unique identification (ID) number per chip

Analog modules

- Two 16-bit SAR ADCs
- Two 12-bit DACs

Communication interfaces

- USB full-/low-speed On-the-Go controller
- USB Device Charger detect
- Controller Area Network (CAN) module
- Three SPI modules
- Three I2C modules
- Six UART modules
- Secure Digital host controller (SDHC)
- I2S module

Timers

- Two 8-channel Flex-Timers (PWM/Motor Control)
- Two 2-channel Flex-Timers (PWM/Quad Decoder)
- Periodic interrupt timers and 16-bit low-power timer
- Carrier modulator transmitter
- Real-time clock
- Programmable delay block

Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- PLL, FLL, and multiple internal oscillators

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

- Three analog comparators (CMP)
- Voltage reference

Ordering Information ¹

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MK21FX512VLQ12	512 KB	128	104
MK21FN1M0VLQ12	1 MB	128	104
MK21FX512VMD12	512 KB	128	104
MK21FN1M0VMD12	1 MB	128	104

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K20PB ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K21P144M50SF5RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K21P144M50SF5 ¹
Package drawing	Package dimensions are provided in package drawings.	<ul style="list-style-type: none"> • LQFP 144-pin: 98ASS23177W¹ • MAPBGA 144-pin: 98ASA00222D¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

Kinetic K21D Family

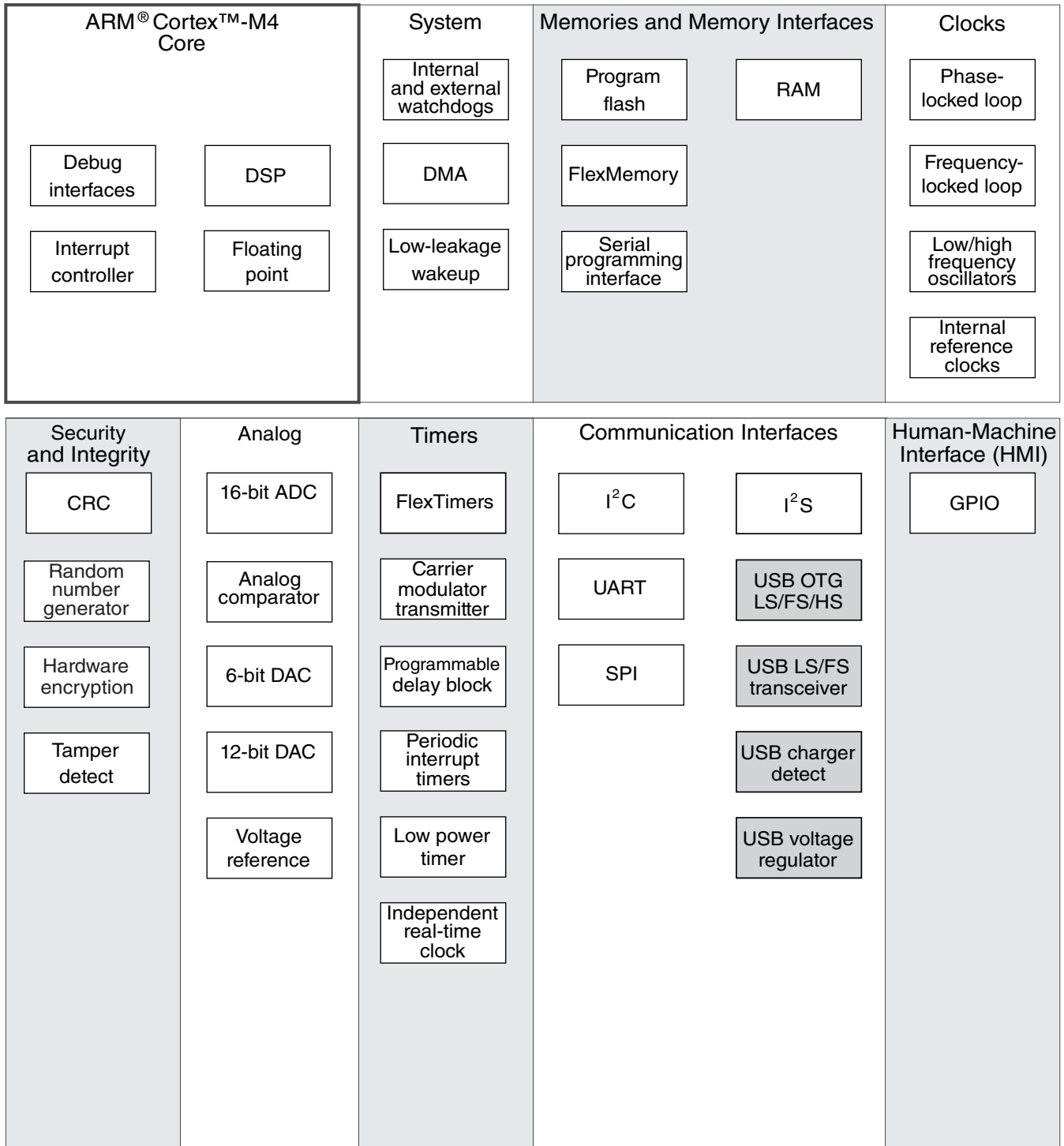


Figure 1. K20 block diagram



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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

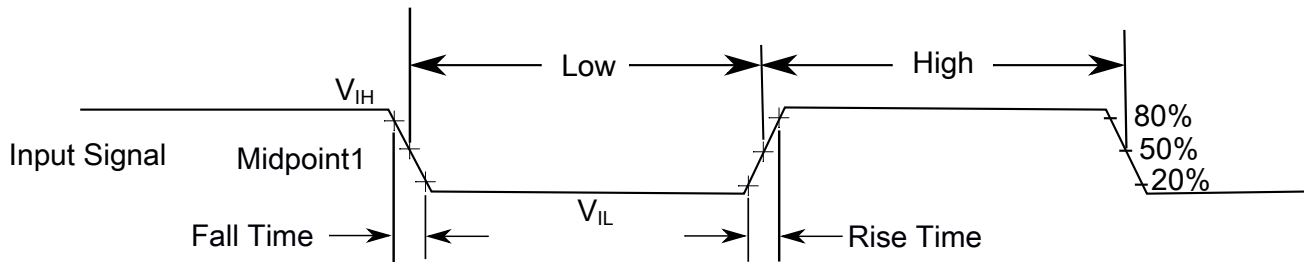
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn}[\text{SRE}]=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn}[\text{DSE}]=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn}[\text{PFE}]=0$)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{CDIO}	Digital pin (except Tamper pins) negative DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ 	-5	—	mA	1
I_{CAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection) 	-5 —	— +5	mA	3
I_{Ccont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection Positive current injection 	-25 —	— +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	4
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} is less than V_{DIO_MIN} , a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} ($=V_{SS}-0.3\text{V}$) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{CDIO}|$.

General

- Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{CAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{CAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
- Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H}	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	2.62	2.70	2.78	V	1
V_{LVW2H}		2.72	2.80	2.88	V	
V_{LVW3H}		2.82	2.90	2.98	V	
V_{LVW4H}		2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	1.74	1.80	1.86	V	1
V_{LVW2L}		1.84	1.90	1.96	V	
V_{LVW3L}		1.94	2.00	2.06	V	
V_{LVW4L}		2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μ s	

- Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -8mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA 	V _{DD} - 0.5	—	—	V	
V _{OH}	Output high voltage — low drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA 	V _{DD} - 0.5	—	—	V	
I _{OHT}	Output high current total for all ports	—	—	100	mA	
V _{OH_Tamper}	Output high voltage — high drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA 	V _{BAT} - 0.5	—	—	V	
V _{OH_Tamper}	Output high voltage — low drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA 	V _{BAT} - 0.5	—	—	V	
I _{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V _{OL}	Output low voltage — high drive strength					1
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA 	—	—	0.5	V	
V _{OL}	Output low voltage — low drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA 	—	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
V _{OL_Tamper}	Output low voltage — high drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA 	—	—	0.5	V	
V _{OL_Tamper}	Output low voltage — low drive strength					
	<ul style="list-style-type: none"> • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA 	—	—	0.5	V	
I _{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	
I _{IND}	Input leakage current, digital pins					2, 3
	<ul style="list-style-type: none"> • V_{SS} ≤ V_{IN} ≤ V_{IL} • All digital pins 	—	0.002	0.5	μA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ	Max.	Unit	Notes
	<ul style="list-style-type: none"> $V_{IN} = V_{DD}$ All digital pins except PTD7 PTD7 	—	0.002	0.5	μA	
		—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins <ul style="list-style-type: none"> $V_{IL} < V_{IN} < V_{DD}$ $V_{DD} = 3.6 V$ $V_{DD} = 3.0 V$ $V_{DD} = 2.5 V$ $V_{DD} = 1.7 V$ 	—	18	26	μA	2
		—	12	19	μA	
		—	8	13	μA	
		—	3	6	μA	
I_{IND}	Input leakage current, digital pins <ul style="list-style-type: none"> $V_{DD} < V_{IN} < 5.5 V$ 	—	1	50	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	0.25	μA	
I_{OZ_Tamper}	Hi-Z (off-state) leakage current (per Tamper pin)	—	—	0.25	μA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	35	50	$k\Omega$	4
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	35	50	$k\Omega$	5

1. Open drain outputs must be pulled to V_{DD} .
2. Measured at $V_{DD}=3.6V$
3. Internal pull-up/pull-down resistors disabled.
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$
5. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	
	• VLLS0 → RUN	—	183	μs	
	• VLLS1 → RUN	—	183	μs	
	• VLLS2 → RUN	—	105	μs	
	• VLLS3 → RUN	—	105	μs	
	• LLS → RUN	—	5.0	μs	
	• VLPS → RUN	—	4.4	μs	
	• STOP → RUN	—	4.4	μs	

2.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	33.57	36.2	mA	
	• @ 3.0V	—	33.51	36.1	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	46.36	50.1	mA	
	• @ 3.0V					
	• @ 25°C	—	46.31	49.9	mA	
	• @ 125°C	—	57.4	—	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	18.2	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	7.2	—	mA	5

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.21	—	mA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.88	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.80	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.528	2.25	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	78	700	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	5.1	15	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	3.1	7.5	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	2.0	5	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	1.25	2.1	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.745	1.65	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.268	1.25	μA	
		—	3.7	15	μA	
		—	22.9	95	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.19	0.22	μA	
		—	0.49	0.64	μA	
		—	2.2	3.2	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers <ul style="list-style-type: none"> • @ 1.8V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C • @ 3.0V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.68	0.8	μA	9
		—	1.2	1.56	μA	
		—	3.6	5.3	μA	
		—	0.81	0.96	μA	
		—	1.45	1.89	μA	
		—	4.3	6.33	μA	
		—	4.3	6.33	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

2.2.5.1 Diagram: Typical I_{DD_RUN} operating behavior

The following data was measured under these conditions:

- MCG in PEE mode at greater than 100 MHz frequencies

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

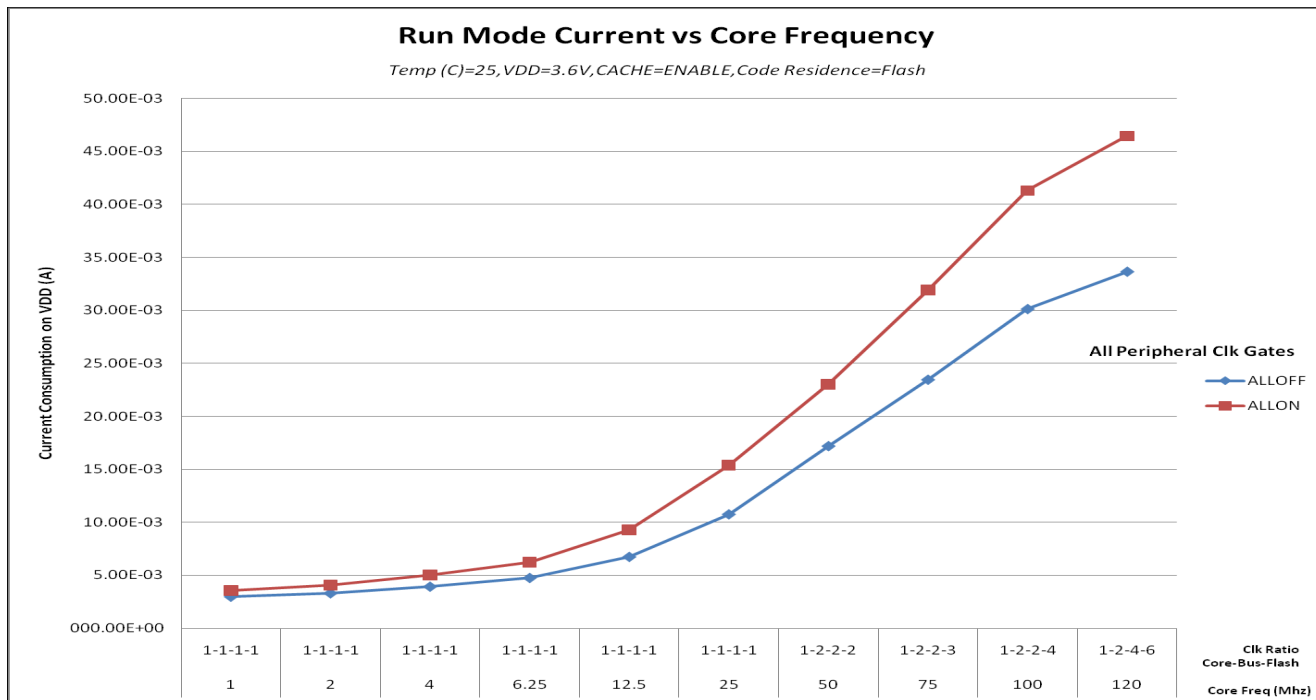


Figure 3. Run mode supply current vs. core frequency

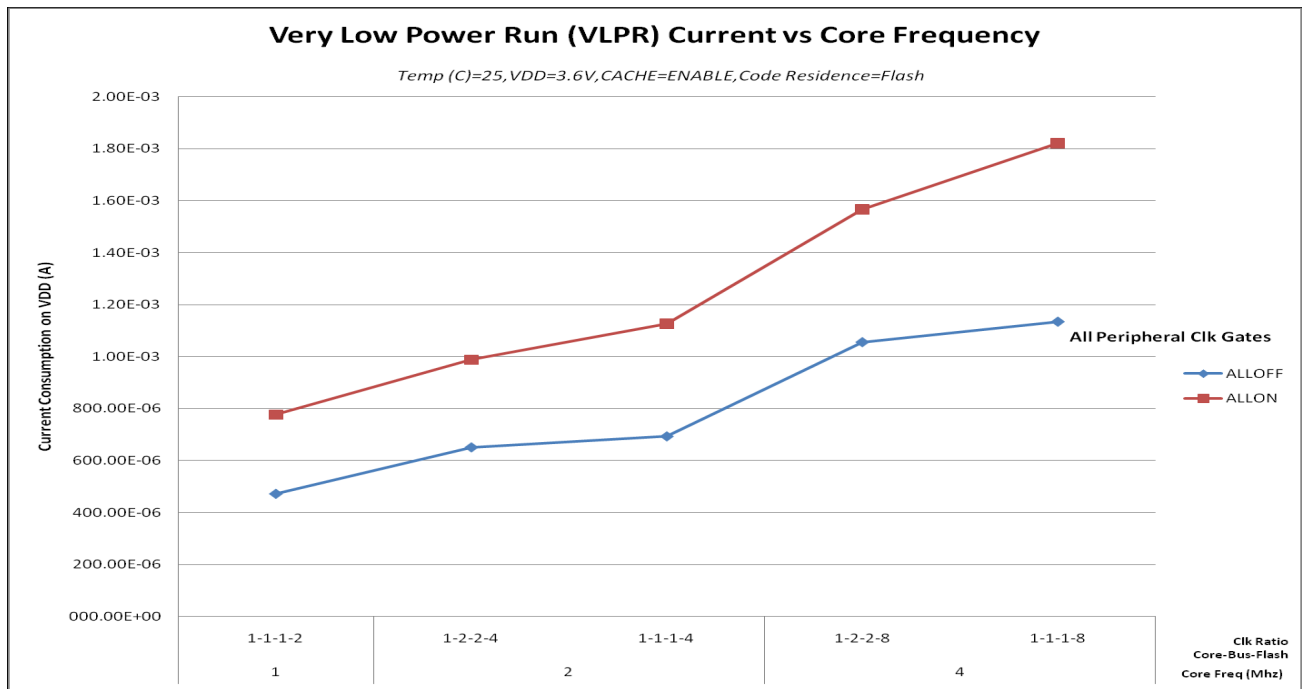


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic

General

application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 96\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
FB_CLK	FlexBus clock	—	4	MHz	
f _{FLASH}	Flash clock	—	0.8	MHz	
f _{ERCLK}	External reference clock	—	16	MHz	
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{FlexCAN_ERCLK}	FlexCAN external reference clock	—	8	MHz	
f _{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength)				4
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	12	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	36	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	<ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ 	—	12	ns	
		—	6	ns	
		—	36	ns	
		—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	105	°C

2.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance,	36	29	°C/W	1

Table continues on the next page...

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
		junction to ambient (natural convection)				
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

Notes

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent (limited to 50 MHz)		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

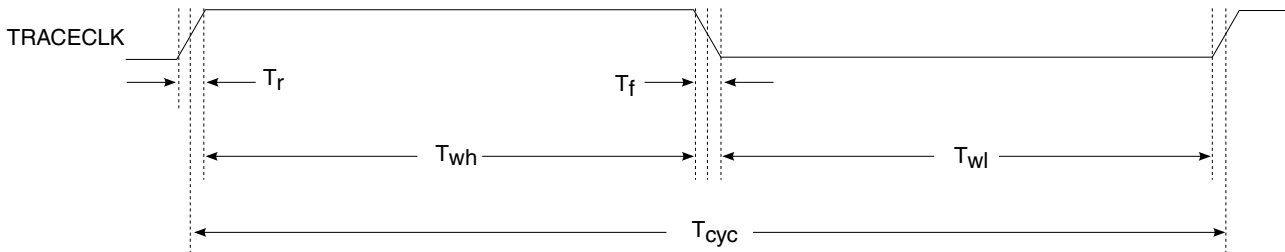


Figure 5. TRACE_CLKOUT specifications

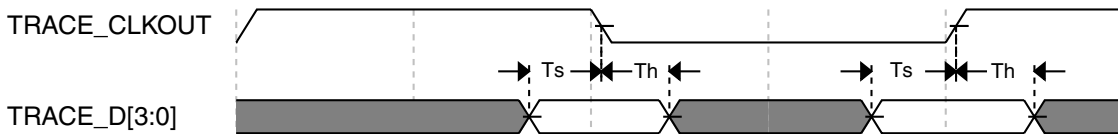


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug 	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug 	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug 	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug 	50 25 12.5	— — —	ns ns ns

Table continues on the next page...

Table 14. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

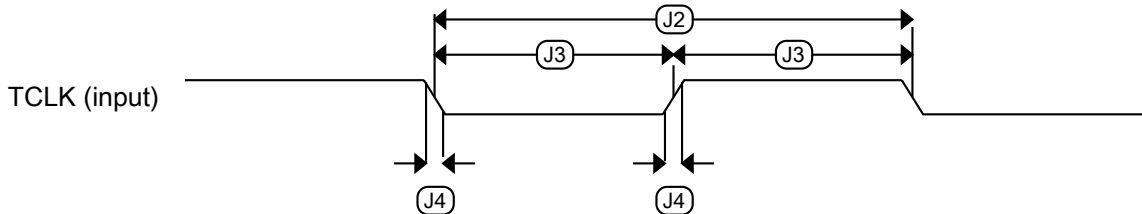


Figure 7. Test clock input timing

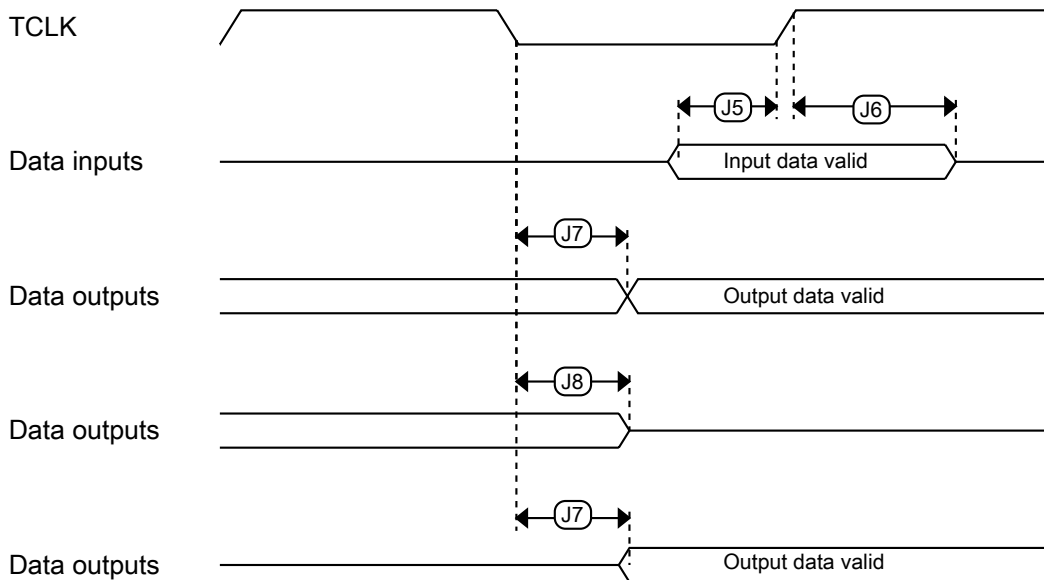


Figure 8. Boundary scan (JTAG) timing

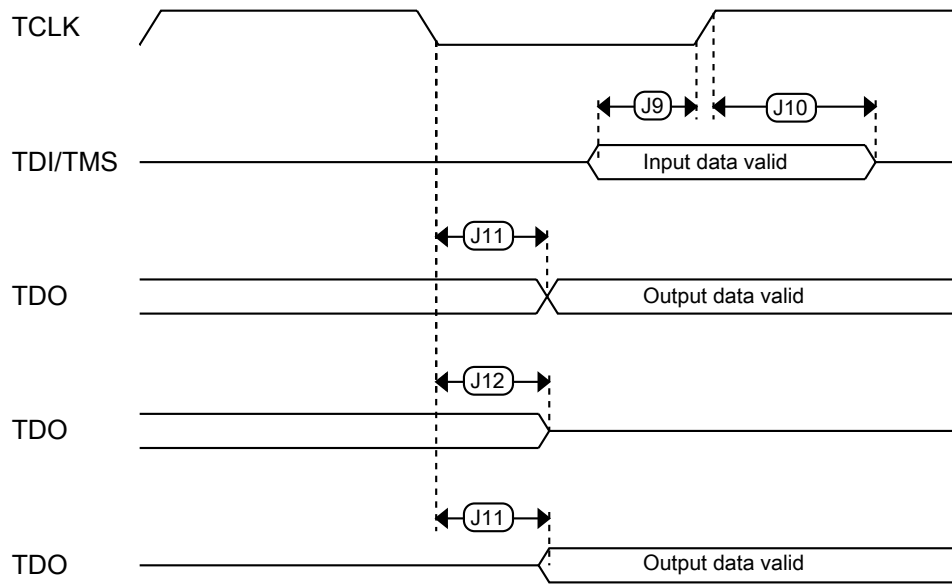


Figure 9. Test Access Port timing

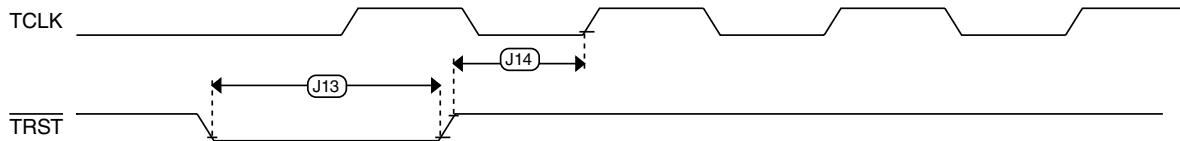


Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
I_{ints}	Internal reference (slow clock) current	—	20	—	μA		
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1	
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% f_{dco}	1	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	% f_{dco}	1, 2	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1	% f_{dco}	1	
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz		
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
I_{intf}	Internal reference (fast clock) current	—	25	—	μA		
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints_t}$	—	—	kHz		
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints_t}$	—	—	kHz		
FLL							
f_{fill_ref}	FLL reference frequency range	31.25	—	39.0625	kHz		
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{fill_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) $1280 \times f_{fill_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fill_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fill_ref}$	80	83.89	100	MHz	
$f_{dco_t_DMX3}$ 2	DCO output frequency	Low range (DRS=00) $732 \times f_{fill_ref}$	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) $1464 \times f_{fill_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

