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Kinetis K22F 256 KB Flash

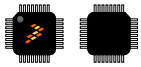
120 MHz ARM® Cortex®-M4-Based Microcontroller with FPU

MK22FN256VDC12
MK22FN256VLL12
MK22FN256VMP12
MK22FN256VLH12

The Kinetis K22 product family members are optimized for cost-sensitive applications requiring low-power, USB connectivity, high peripheral integration and processing efficiency with floating point unit. These devices share the comprehensive enablement and scalability of the Kinetis family.
This product offers:

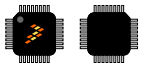
- Run power consumption down to 153 µA/MHz and static power consumption down to 2.6 µA with full state retention and 6 µs wakeup. Lowest static mode down to 120 nA
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator. USB FS device crystal-less functionality.

121 XFBGA (DC)
8 x 8 x 0.5 Pitch 0.65 mm



100 LQFP (LL)
14 x 14 x 1.4 Pitch 0.5 mm

64 MAPBGA (MP)
5 x 5 x 1.2 Pitch 0.5 mm



64 LQFP (LH)
10 x 10 x 1.4 Pitch 0.5 mm

Performance
- 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

Memories and memory interfaces
- 256 KB of embedded flash and 48 KB of RAM
- Serial programming interface (EzPort)
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

System peripherals
- Flexible low-power modes, multiple wake up sources
- 16-channel DMA controller
- Independent external and software watchdog monitor

Clocks
- Two crystal oscillators: 32 kHz (RTC) and 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz
- Multi-purpose clock generator with PLL and FLL

Security and integrity modules
- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Hardware random-number generator
- Flash access control to protect proprietary software

Human-machine interface
- Up to 70 general-purpose I/O (GPIO)

Analog modules
- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- One 12-bit DAC
- Two analog comparators (CMP) with 6- bit DAC
- Accurate internal voltage reference

Communication interfaces
- USB LS/FS OTG 2.0 with on-chip transceiver and USB LDO voltage regulator
- USB full-speed device crystal-less operation
- Two SPI modules
- Three UART modules and one low-power UART
- Two I2C modules: Support for up to 1 Mbps operation
- I2S module

Timers
- One 8-channel general purpose/ PWM timer
- Two 2-channel general purpose timers with quadrature decoder functionality
- Periodic interrupt timers
- 16-bit low-power timer
- Real-time clock with independent power domain
- Programmable delay block

Operating Characteristics
- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Ordering Information

Part Number	Memory		Number of GPIOs
	Flash (KB)	SRAM (KB)	
MK22FN256VDC12	256	48	70
MK22FN256VLL12	256	48	66
MK22FN256VMP12	256	48	40
MK22FN256VLH12	256	48	40

Device Revision Number

Device Mask Set Number	SIM_SDID[REVID]	JTAG ID Register[PRN]
0N51M	0001	0001

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector	KINETISKMCUSELGD
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K22FPB
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K22P121M120SF8RM
Data Sheet	The Data Sheet is this document. It includes electrical characteristics and signal connections.	K22P121M120SF8
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_K_*x*N51M [1]
Package drawing	Package dimensions are provided by part number: • MK22FN256VDC12 • MK22FN256VLL12 • MK22FN256VMP12 • MK22FN256VLH12	Package drawing: • 98ASA00595D • 98ASS23308W • 98ASA00420D • 98ASS23234W

1. To find the associated resource, go to nxp.com and perform a search using this term with the *x* replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

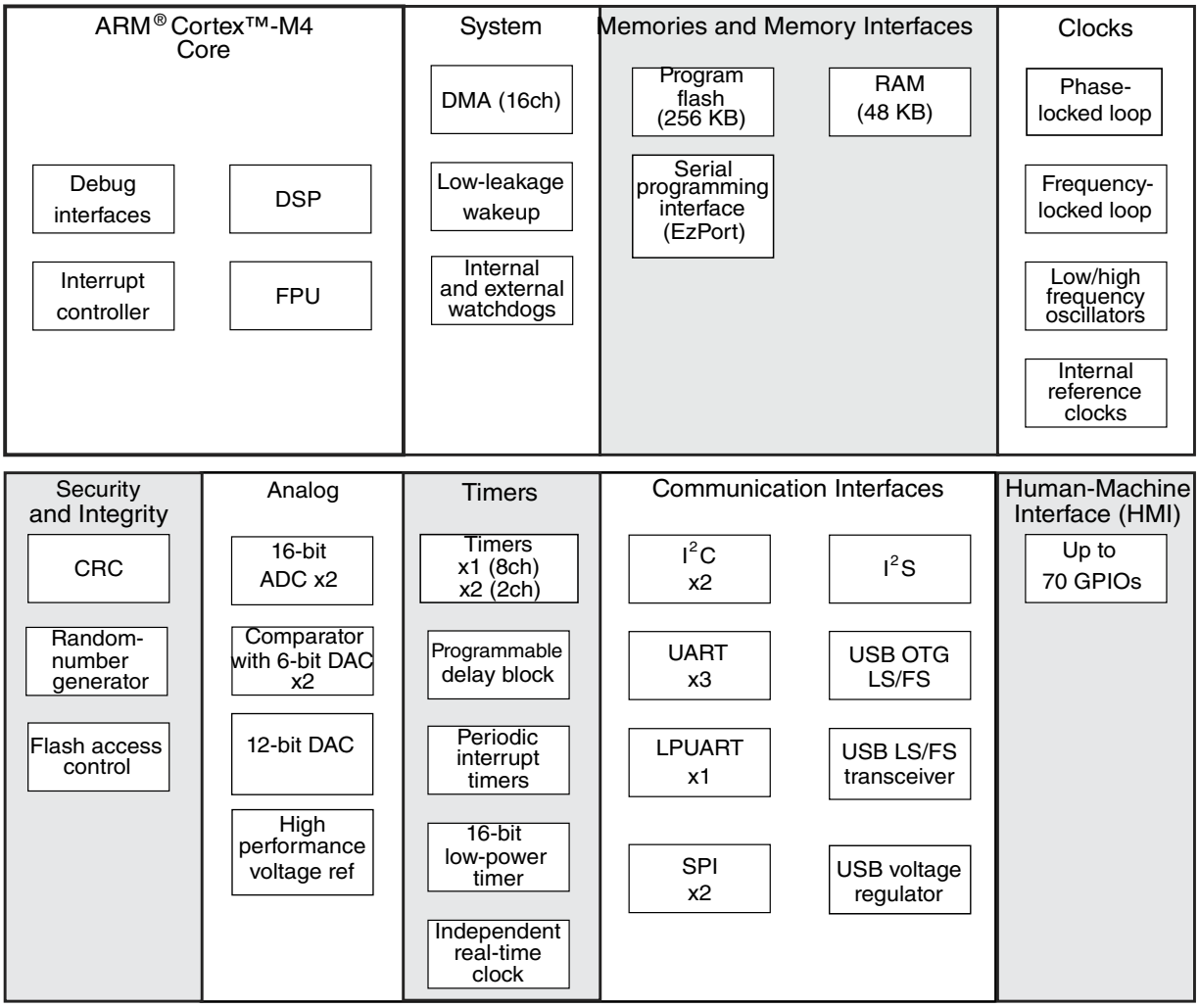


Figure 1. Functional block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

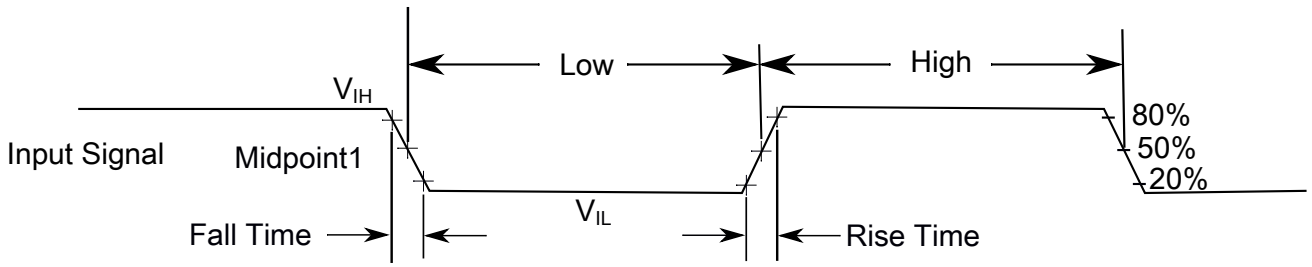
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	158	mA
V_{DIO}	Digital input voltage	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1]	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Analog and I/O pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection)	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	1

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	—	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DD} – 0.5	—	—	V	
V_{OH}	Output high voltage — High drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	—	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	—	0.5	V	
V_{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	—	0.5	V	
V_{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 3 mA	—	—	0.5	V	
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	µA	1, 2
	High drive port pins	—	0.004	0.5	µA	
I_{IN}	Input leakage current (total all pins) for full temperature range	—	—	1.0	µA	2
R_{PU}	Internal pullup resistors	20	—	50	kΩ	3
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at VDD=3.6V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the	—	—	300	µs	1

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	first instruction across the operating temperature range of the chip.					
	• VLLS0 → RUN	—	—	140	µs	
	• VLLS1 → RUN	—	—	140	µs	
	• VLLS2 → RUN	—	—	80	µs	
	• VLLS3 → RUN	—	—	80	µs	
	• LLS2 → RUN	—	—	6	µs	
	• LLS3 → RUN	—	—	6	µs	
	• VLPS → RUN	—	—	5.7	µs	
	• STOP → RUN	—	—	5.7	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash @ 1.8V	—	25.66	26.35	mA	2, 3, 4

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 3.0V	—	25.75	26.44	mA	
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	23.6	24.29	mA	2
	@ 3.0V	—	23.7	24.39	mA	
I_{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	31.9	32.59	mA	5
	@ 3.0V	—	32.0	32.69	mA	
I_{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	15.8	16.49	mA	3, 4, 6
	@ 3.0V	—	15.8	16.49	mA	
I_{DD_RUN}	Run mode current in Compute operation — code executing from flash					
	@ 1.8V	—	14.00	15.50	mA	6
	@ 3.0V	—	14.00	15.69	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	15.3	15.99	mA	7
	@ 3.0V	—	15.4	16.09	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	20.4	21.09	mA	8
	@ 3.0V					
	• @ 25°C	—	20.5	21.19	mA	
	• @ 70°C	—	20.5	21.19	mA	
	• @ 85°C	—	20.5	21.19	mA	
	• @ 105°C	—	21.4	22.09	mA	
I_{DD_RUN}	Run mode current — Compute operation, code executing from flash					
	@ 1.8V	—	14.0	14.69	mA	9
	@ 3.0V					
	• @ 25°C	—	14.0	14.69	mA	
	• @ 70°C	—	14.0	14.69	mA	
	• @ 85°C	—	14.0	14.69	mA	
	• @ 105°C	—	15.0	15.69	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	8.1	8.79	mA	7

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	4.4	5.09	mA	10
I_{DD_VLPR}	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	0.70	0.88	mA	3, 4, 11
	@ 3.0V	—	0.70	0.88	mA	
I_{DD_VLPR}	Very-low-power run mode current in Compute operation, code executing from flash		0.61	0.79		
	@ 1.8V	—			mA	11
	@ 3.0V	—	0.61	0.79	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.68	0.87	mA	12
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.10	1.28	mA	13
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.38	0.57	mA	14
I_{DD_STOP}	Stop mode current at 3.0 V					
	@ -40°C to 25°C	—	0.27	0.35	mA	
	@ 70°C	—	0.32	0.47	mA	
	@ 85°C	—	0.32	0.51	mA	
	@ 105°C	—	0.45	0.77	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	@ -40°C to 25°C	—	4.5	12.00	µA	
	@ 70°C	—	16.8	42.40	µA	
	@ 85°C	—	28.9	73.45	µA	
	@ 105°C	—	60.8	141.90	µA	
I_{DD_LLS3}	Low leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	—	2.6	3.75	µA	
	@ 70°C	—	6.6	12.00	µA	
	@ 85°C	—	10.5	17.25	µA	
	@ 105°C	—	21.0	40.70	µA	
I_{DD_LLS2}	Low leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	2.4	3.40	µA	
	@ 70°C	—	5.3	8.90	µA	
	@ 85°C	—	5.1	10.05	µA	
	@ 105°C	—	15.9	28.85	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	—	1.9	2.30	µA	
	@ 70°C	—	4.8	8.10	µA	
	@ 85°C	—	7.6	11.30	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 105°C	—	15.3	27.65	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	1.7	2.10	µA	
	@ 70°C	—	3.4	4.85	µA	
	@ 85°C	—	5.1	8.80	µA	
	@ 105°C	—	9.8	15.70	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	—	0.71	0.96	µA	
	@ 70°C	—	1.79	2.10	µA	
	@ 85°C	—	2.9	4.70	µA	
	@ 105°C	—	5.7	8.10	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.40	0.56	µA	
	@ 70°C	—	1.39	1.70	µA	
	@ 85°C	—	2.5	4.25	µA	
	@ 105°C	—	5.3	7.50	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.12	0.38	µA	
	@ 70°C	—	1.05	1.38	µA	
	@ 85°C	—	2.20	3.95	µA	
	@ 105°C	—	4.9	7.10	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ -40°C to 25°C	—	0.18	0.21	µA	
	@ 70°C	—	0.66	0.86	µA	
	@ 85°C	—	1.52	2.24	µA	
	@ 105°C	—	2.92	4.30	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					
	@ 1.8V					
	• @ -40°C to 25°C	—	0.59	0.70	µA	15
	• @ 70°C	—	1.00	1.3	µA	
	• @ 85°C	—	1.76	2.59	µA	
	• @ 105°C	—	3.00	4.42	µA	
	@ 3.0V					
	• @ -40°C to 25°C	—	0.71	0.84	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 70°C	—	1.22	1.59	µA	
	• @ 85°C	—	2.08	3.06	µA	
	• @ 105°C	—	3.50	5.15	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120MHz core and system clock, 60MHz bus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. Cache on and prefetch on, low compiler optimization.
4. Coremark benchmark compiled using IAR 7.2 with optimization level low.
5. 120MHz core and system clock, 60MHz bus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
6. 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
7. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
8. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
15. Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by							

Table continues on the next page...

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	µA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

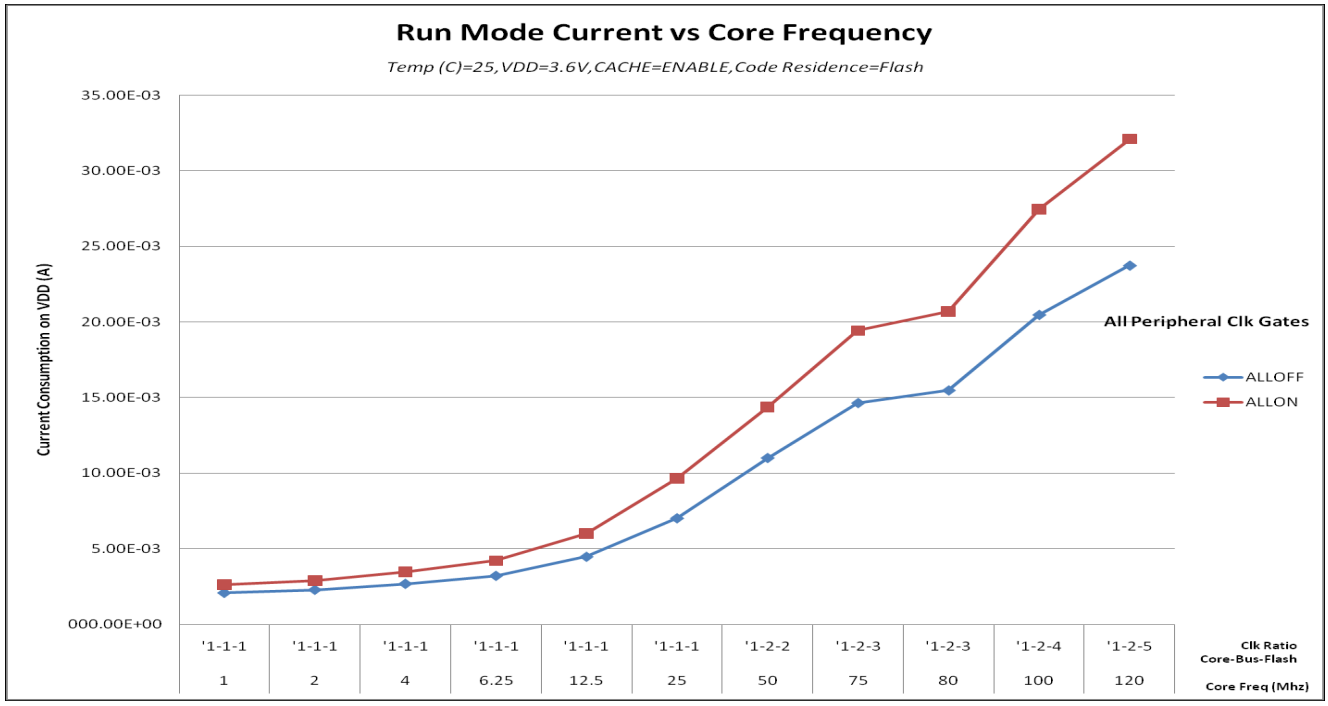


Figure 3. Run mode supply current vs. core frequency

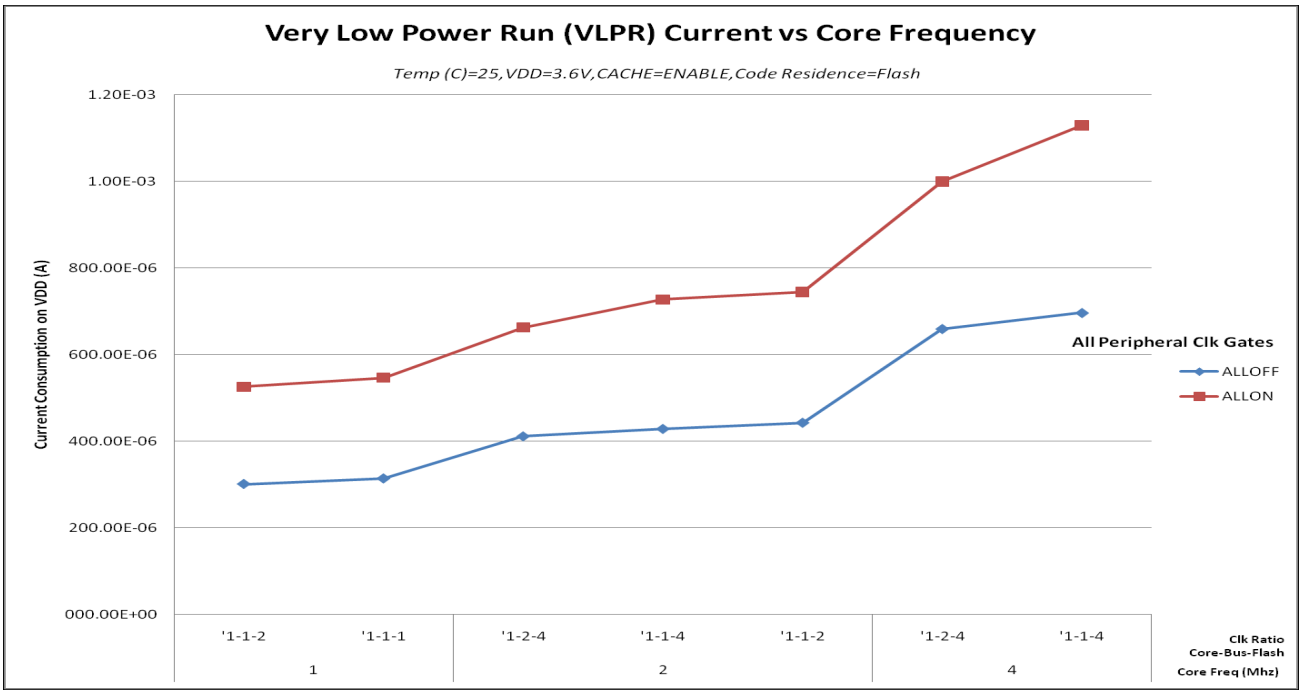


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V_{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: • VREGIN (USB) = 5.0 V • VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MK22FN512VLH12 .

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	80	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	26.67	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time				5
	• Slew disabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	10	ns	
	• $2.7 \le V_{DD} \le 3.6V$		5	ns	
	• Slew enabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	30	ns	
	• $2.7 \le V_{DD} \le 3.6V$		16	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.

4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	44.4	61	67	47.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	48	48	38.9	°C/W	2
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	37.2	51	55	40.1	°C/W	3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	23.7	42	42	35.3	°C/W	3

Table continues on the next page...

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	23.5	34	31	35.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	17.4	16	16	29.2	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	3	3	0.4	°C/W	6

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).
3. Determined according to JEDEC Standard JESD51-6, Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air) with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation • Serial wire debug	0	33	MHz

Table continues on the next page...

Table 13. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width • Serial wire debug	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

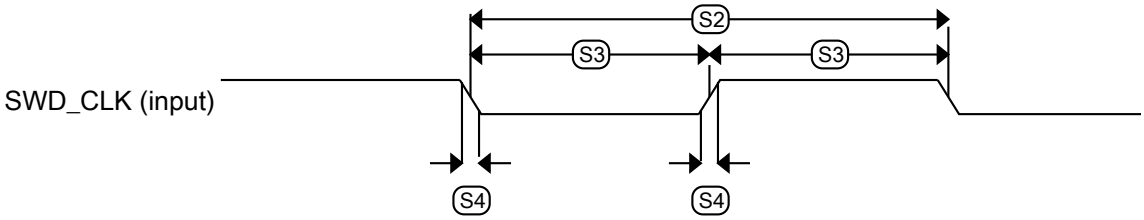


Figure 5. Serial wire clock input timing

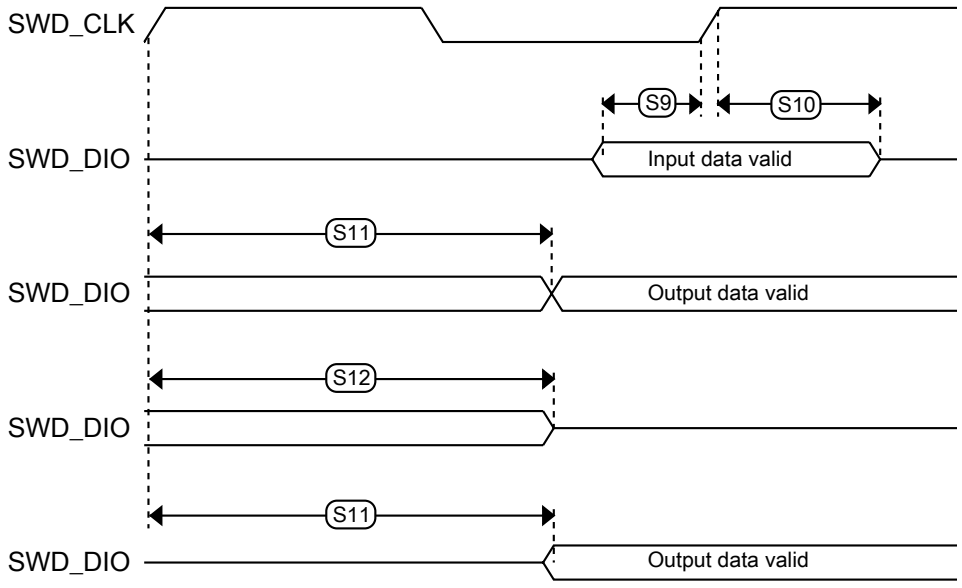


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns

Table continues on the next page...

Table 15. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

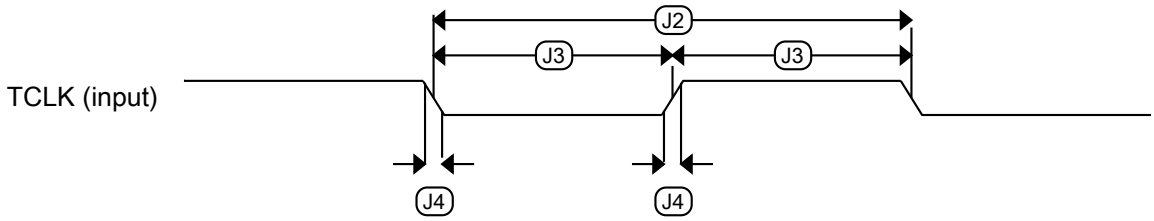


Figure 7. Test clock input timing

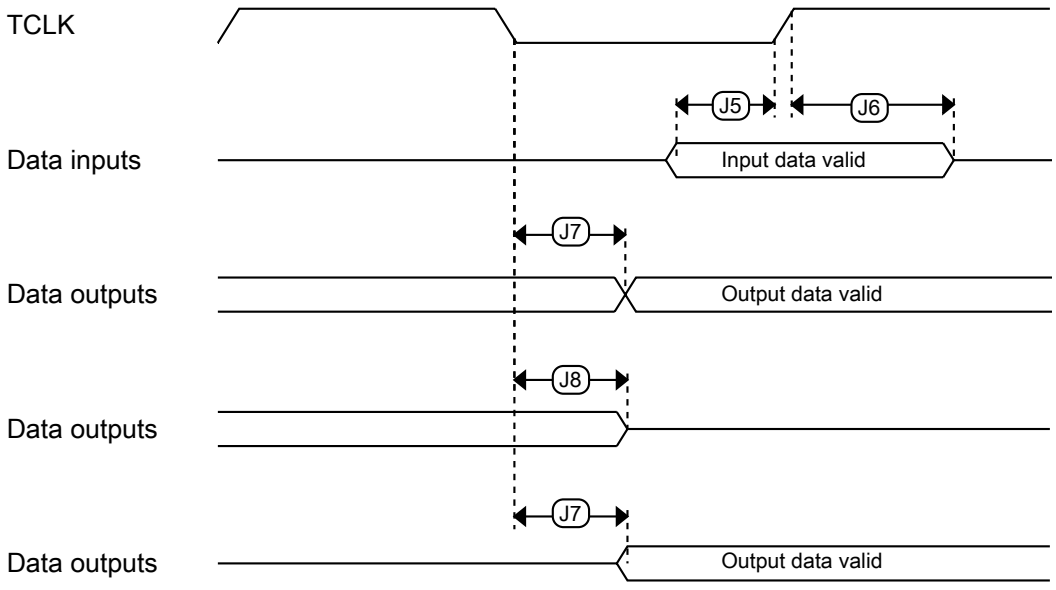


Figure 8. Boundary scan (JTAG) timing

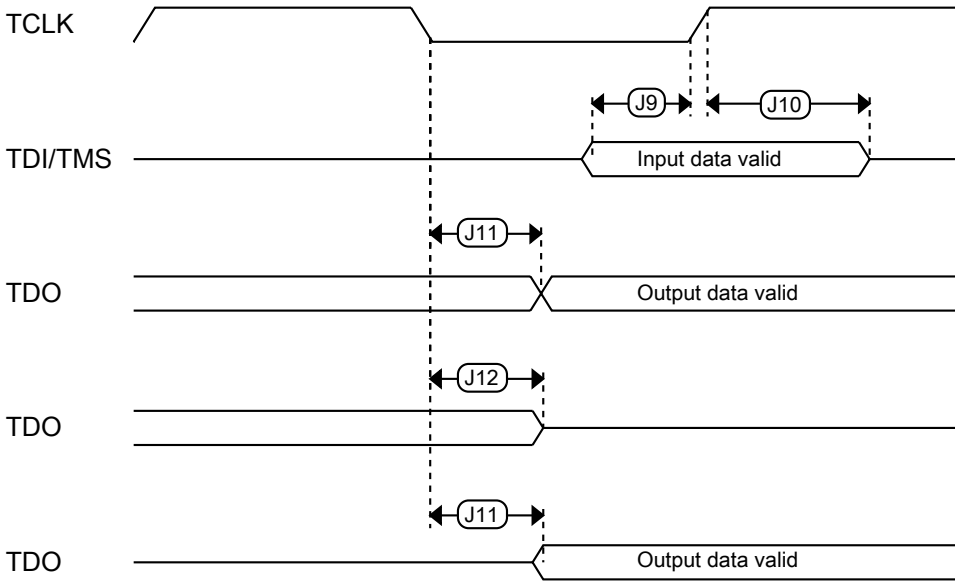


Figure 9. Test Access Port timing

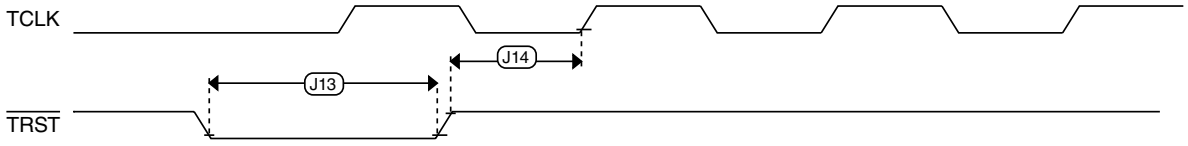


Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules