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Kinetis K22F 512KB Flash

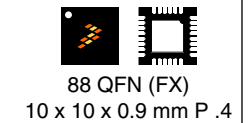
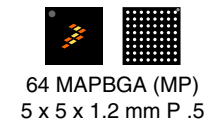
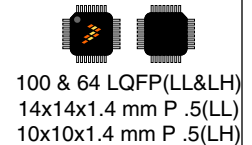
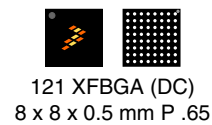
120 MHz ARM® Cortex®-M4 Based Microcontroller with FPU

The Kinetis K22 product family members are optimized for cost-sensitive applications requiring low-power, USB connectivity, and processing efficiency and high peripheral integration with a floating point unit. These devices share the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- Run power consumption down to 156 $\mu\text{A}/\text{MHz}$ and static power consumption down to 3.8 μA , full state retention and 6 μS wakeup. Lowest static mode down to 140 nA.
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator. USB FS device crystal-less functionality.

MK22FN512VDC12
MK22FN512VLL12
MK22FN512VLH12
MK22FN512VMP12
MK22FN512VFX12



Performance

- 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

Memories and memory interfaces

- 512 KB of embedded flash and 128 KB of RAM
- FlexBus external bus interface ¹
- Serial programming interface (EzPort)
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

Timers

- Two 8-ch general purpose/PWM timers
- Two 2-ch general purpose timers with quadrature decoder functionality
- Periodic interrupt timers
- 16-bit low-power timer
- Real-time clock with independent power domain
- Programmable delay block

Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Hardware random-number generator
- Flash access control to protect proprietary software

Operating Characteristics

- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Analog modules

- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- Two 12-bit DACs ²
- Two analog comparators (CMP) with 6-bit DAC
- Accurate internal voltage reference

System peripherals

- Flexible low-power modes, multiple wake-up sources
- 16-channel DMA controller
- Independent external and software watchdog monitor

Clocks

- Two crystal oscillators: 32 kHz (RTC) and 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, & 48 MHz
- Multipurpose clock generator with PLL and FLL

Communication interfaces

- USB full/low-speed On-the-Go controller
- USB full-speed device crystal-less operation
- Two SPI modules and I2S module
- Three UART modules and one low-power UART
- Two I2C: Support for up to 1 Mbps operation

Human-machine interface

- Up to 81 general-purpose I/O (GPIO)



1. MK22FN512VFX12 (88QFN) does not support the FlexBus function.
2. MK22FN512VFX12 (88QFN) does not support the DAC1 function.

Ordering Information

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MK22FN512VDC12	512	128	81
MK22FN512VLL12	512	128	66
MK22FN512VLH12	512	128	40
MK22FN512VMP12	512	128	40
MK22FN512VFX12	512	128	60

Device Revision Number

Device Mask Set Number	SIM_SDID[REVID]	JTAG ID Register[PRN]
0N50M	0001	0001

Related Resources

Type	Description	Document
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector	KINETISKMCUSELGD
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K22FPB
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K22P121M120SF7RM
Data Sheet	The Data Sheet is this document. It includes electrical characteristics and signal connections.	K22P121M120SF7
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_K_xN50M¹
Package drawing	Package dimensions are provided by part number: <ul style="list-style-type: none"> • MK22FN512VDC12 • MK22FN512VLL12 • MK22FN512VLH12 • MK22FN512VMP12 • MK22FN512VFX12 	Package drawing: <ul style="list-style-type: none"> • 98ASA00595D • 98ASS23308W • 98ASS23234W • 98ASA00420D • 98ASA00935D
Engineering Bulletin	This engineering bulletin gives connection recommendations specifically for microcontrollers in DFN and QFN packages.	Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages.

1. To find the associated resource, go to [nxp.com](#) and perform a search using this term with the x replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

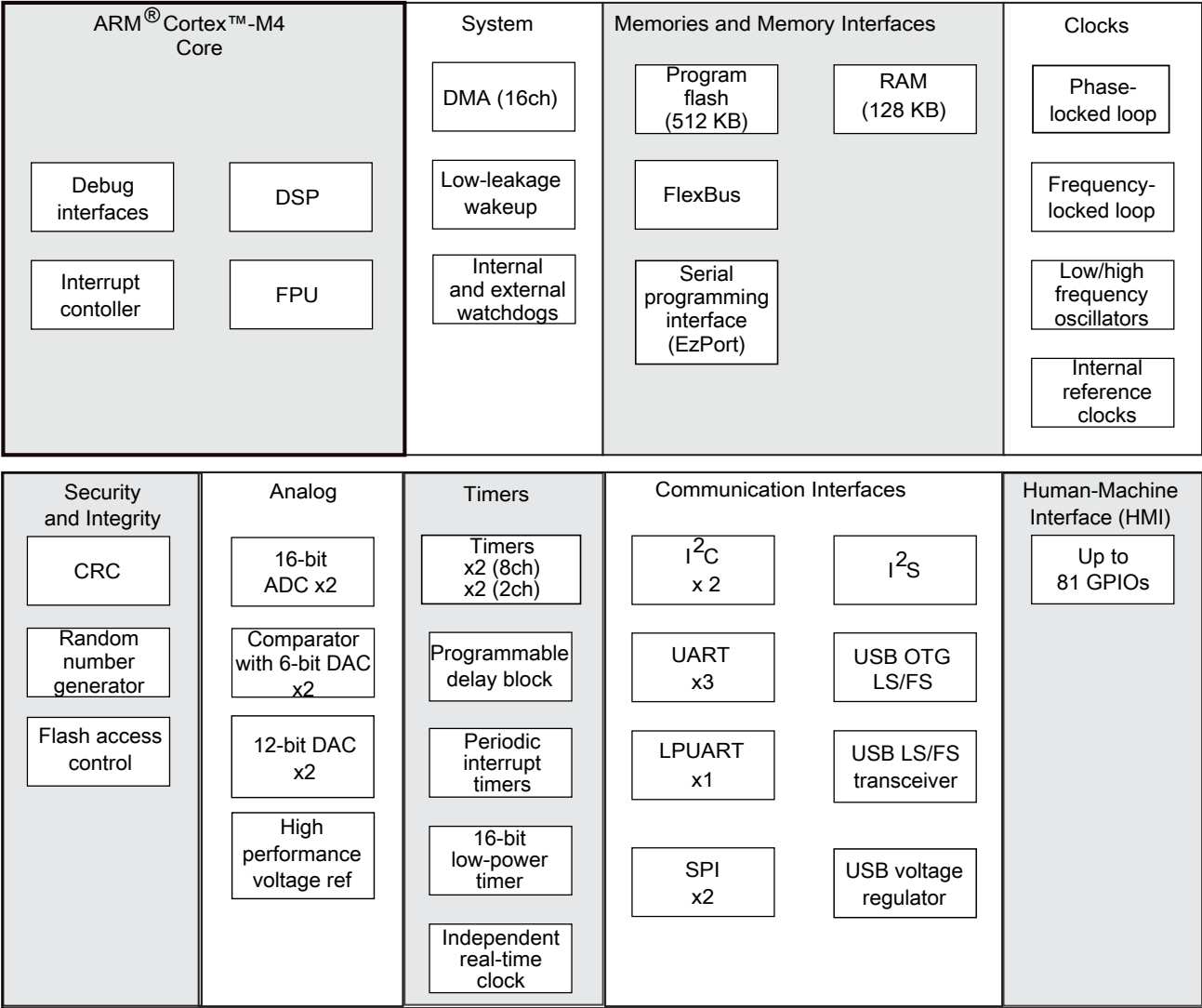


Figure 1. Functional block diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

General

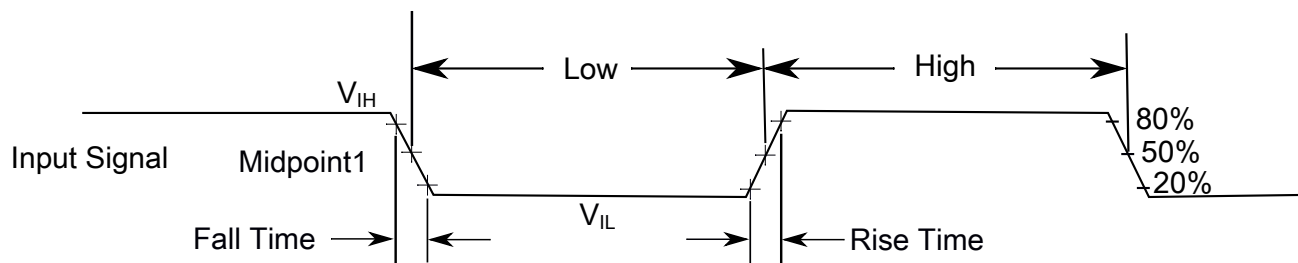
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	169	mA
V_{DIO}	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
V _{DD} – V _{DDA}	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
V _{SS} – V _{SSA}	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	
V _{IH}	Input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	0.7 × V _{DD} 0.75 × V _{DD}	— —	V V	
V _{IL}	Input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	— —	0.35 × V _{DD} 0.3 × V _{DD}	V V	
V _{HYS}	Input hysteresis	0.06 × V _{DD}	—	V	
I _{ICIO}	Analog and I/O pin DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V (Negative current injection) 	-3	—	mA	1
I _{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection 	-25	—	mA	
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	—	V	
V _{RFVBAT}	V _{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}	—	V	

1. All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN}) / |I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H}	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> • Level 1 falling (LVWV=00) 	2.62	2.70	2.78	V	1

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L}	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -5 mA	V _{DD} - 0.5	—	—	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -2.5 mA	V _{DD} - 0.5	—	—	V	
V _{OH}	Output high voltage — High drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -20 mA	V _{DD} - 0.5	—	—	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -10 mA	V _{DD} - 0.5	—	—	V	
I _{OHT}	Output high current total for all ports	—	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 2.5 mA	—	—	0.5	V	
V _{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 10 mA	—	—	0.5	V	
V _{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 3 mA	—	—	0.5	V	
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 1.5 mA	—	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	μA	1, 2
	High drive port pins	—	0.004	0.5	μA	
I _{IN}	Input leakage current (total all pins) for full temperature range	—	—	1.0	μA	2
R _{PU}	Internal pullup resistors	20	—	50	kΩ	3
R _{PD}	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD}=3.6V
3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLS_x→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- FlexBus clock = 20 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• VLLS0 → RUN	—	—	140	μs	
	• VLLS1 → RUN	—	—	140	μs	
	• VLLS2 → RUN	—	—	80	μs	
	• VLLS3 → RUN	—	—	80	μs	
	• LLS2 → RUN	—	—	6	μs	
	• LLS3 → RUN	—	—	6	μs	
	• VLPS → RUN	—	—	5.7	μs	
	• STOP → RUN	—	—	5.7	μs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The I_{DD} typical values represent the statistical mean at 25°C, and the I_{DD} maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 1.8V @ 3.0V	— —	28.0 28.0	29.33 29.33	mA mA	2, 3, 4
I _{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	25.6 25.7	26.93 27.03	mA mA	2
I _{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V	— —	35.5 35.6	36.83 36.93	mA mA	5
I _{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	17.5 17.5	18.83 18.83	mA mA	3, 4, 6
I _{DD_RUN}	Run mode current in Compute operation — code executing from flash @ 1.8V @ 3.0V	— —	15.10 15.10	17.10 17.33	mA mA	6
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	16.6 16.8	17.93 18.13	mA mA	7
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C • @ 105°C	— — — — —	22.8 22.9 23.1 23.5 23.8	24.13 24.23 24.43 24.83 25.13	mA mA mA mA mA	8
I _{DD_RUN}	Run mode current — Compute operation, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C • @ 105°C	— — — — —	15.1 15.1 15.4 15.6 16.0	16.43 16.43 16.73 16.93 17.33	mA mA mA mA mA	9

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	9.3	10.63	mA	7
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.4	6.73	mA	10
I _{DD_VLPR}	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	—	0.88	1.02	mA	3, 4, 11
		—	0.89	1.03	mA	
I _{DD_VLPR}	Very-low-power run mode current in Compute operation, code executing from flash @ 1.8V @ 3.0V	—	0.62	0.77	mA	11
		—	0.63	0.77	mA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.76	0.90	mA	12
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.2	1.34	mA	13
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.45	0.59	mA	14
I _{DD_STOP}	Stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	0.28	0.37	mA	
		—	0.34	0.51	mA	
		—	0.38	0.55	mA	
		—	0.50	0.80	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	8.7	18.10	μA	
		—	31.1	79.55	μA	
		—	50.3	110.15	μA	
		—	98.6	238.30	μA	
I _{DD_LLS3}	Low leakage stop mode 3 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	3.8	5.65	μA	
		—	12.5	28.75	μA	
		—	20.2	47.60	μA	
		—	39.5	91.25	μA	
I _{DD_LLS2}	Low leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	3.0	4.10	μA	
		—	7.8	16.40	μA	
		—	12.3	30.15	μA	
		—	23.6	55.30	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V @ -40°C to 25°C	—	2.8	3.95	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 70°C @ 85°C @ 105°C	— — —	9.5 15.3 30.1	21.25 34.65 66.05	μA μA μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	— — — —	1.9 4.5 6.8 13.0	2.45 8.50 12.15 25.50	μA μA μA μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	— — — —	0.73 1.8 3.0 5.9	1.42 3.90 5.25 10.80	μA μA μA μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	— — — —	0.43 1.4 2.6 5.4	0.55 2.45 4.00 9.30	μA μA μA μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	— — — —	0.14 1.1 2.3 5.1	0.24 2.15 3.85 9.00	μA μA μA μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	— — — —	0.18 0.66 1.52 2.92	0.21 0.86 2.24 4.30	μA μA μA μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8V • @ -40°C to 25°C • @ 70°C • @ 85°C • @ 105°C @ 3.0V	— — — —	0.59 1.00 1.76 3.00	0.70 1.3 2.59 4.42	μA μA μA μA	15

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> @ -40°C to 25°C 	—	0.71	0.84	μA	
	<ul style="list-style-type: none"> @ 70°C 	—	1.22	1.59	μA	
	<ul style="list-style-type: none"> @ 85°C 	—	2.08	3.06	μA	
	<ul style="list-style-type: none"> @ 105°C 	—	3.50	5.15	μA	

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
- Cache on and prefetch on, low compiler optimization.
- Coremark benchmark compiled using IAR 7.2 with optimization level low.
- 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
- 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
- 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
- 25MHz core and system clock, 25MHz bus clock, and 25MHz FlexBus and flash clock. MCG configured for FEI mode.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHZ}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHZ}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{EREFSTEN4MHZ}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I _{EREFSTEN32KHZ}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN							

Table continues on the next page...

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. VLLS1 VLLS3 LLS VLPS STOP	440 440 490 510 510	490 490 490 560 560	540 540 540 560 560	560 560 560 560 560	570 570 570 610 610	580 580 680 680 680	nA
I _{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock) >OSCECLK (4 MHz external crystal)	 66 214	 66 237	 66 246	 66 254	 66 260	 66 268	 μA
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

General

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

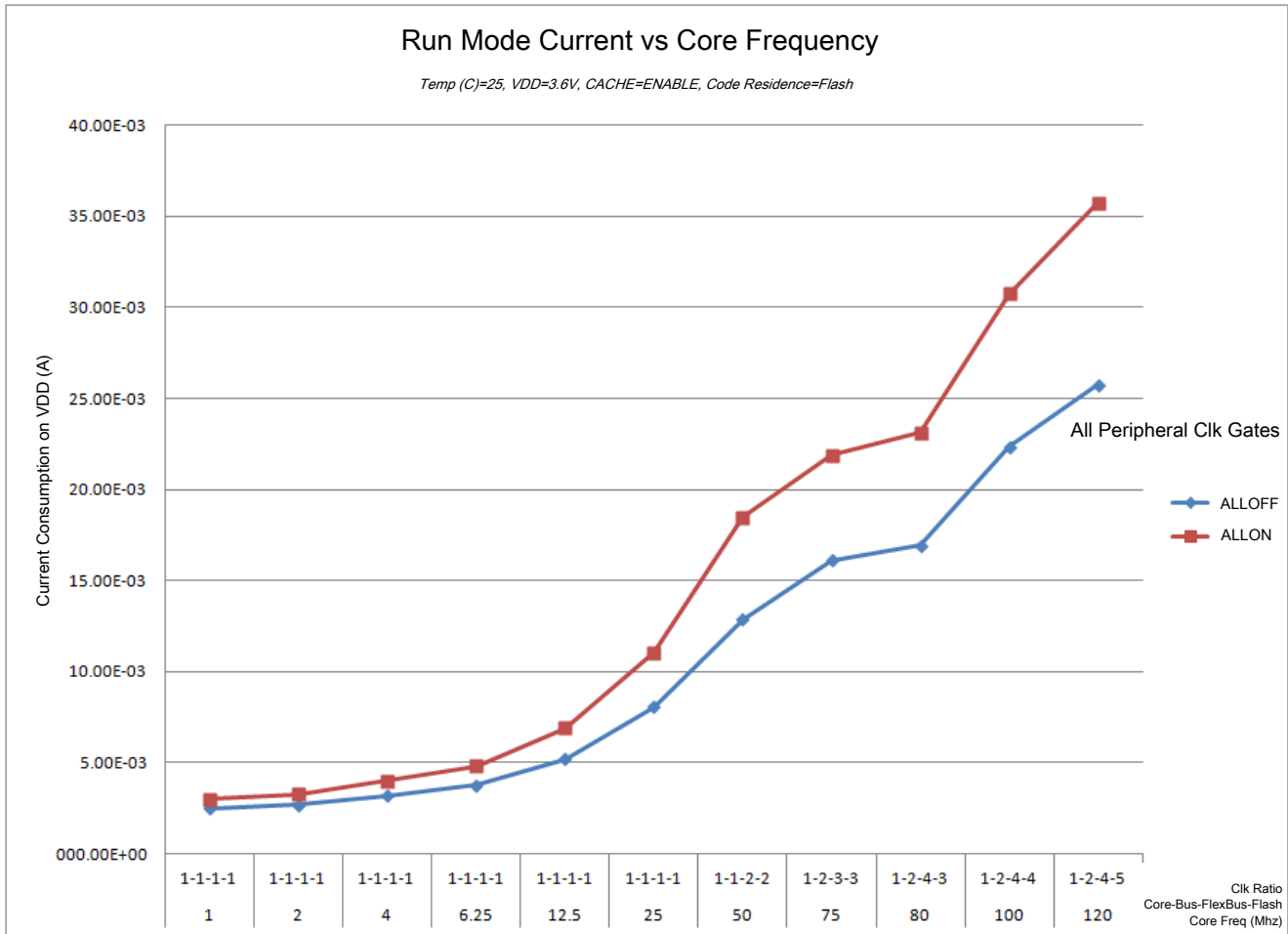


Figure 3. Run mode supply current vs. core frequency

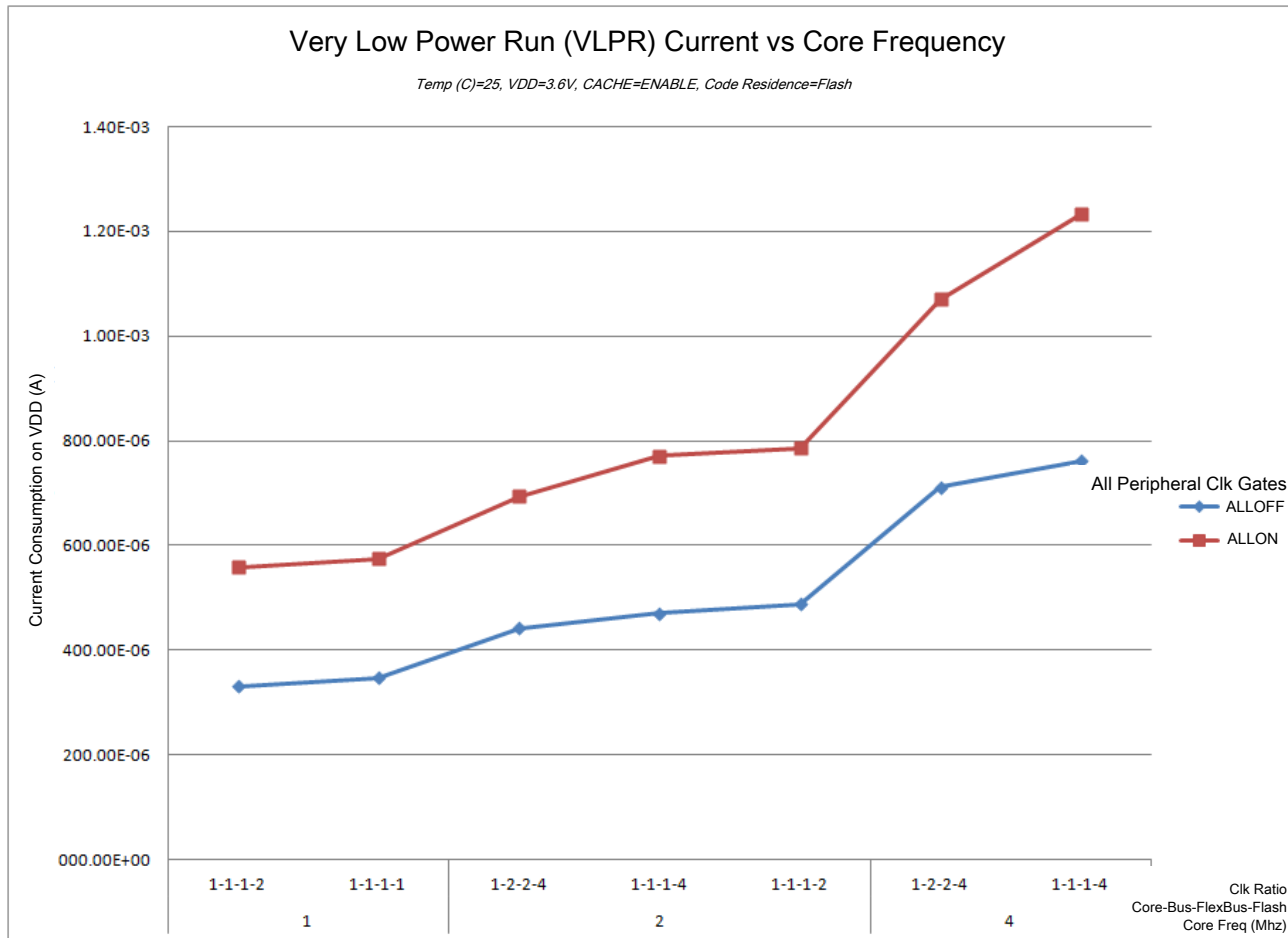


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V _{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: <ul style="list-style-type: none"> VREGIN (USB) = 5.0 V VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MK22FN512VLH12 .

General

- The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
- IEC Level Maximums: $M \leq 18\text{dBmV}$, $L \leq 24\text{dBmV}$, $K \leq 30\text{dBmV}$, $I \leq 36\text{dBmV}$, $H \leq 42\text{dBmV}$.

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	80	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f_{FLASH}	Flash clock	—	26.67	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select ($\overline{EZP_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ 	— — — —	10 5 30 16	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.

General

2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _J	Die junction temperature	-40	125	°C	
T _A	Ambient temperature	-40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	44.4	61	67	95.7	°C/W	1
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	27.0	48	48	48.8	°C/W	2
Single-layer (1s)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	37.2	51	55	74.4	°C/W	3
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	23.7	42	42	44.0	°C/W	3
—	R _{θJB}	Thermal resistance, junction to board	23.5	34	31	30.3	°C/W	4
—	R _{θJC}	Thermal resistance, junction to case	17.4	16	16	28.0	°C/W	5
—	Ψ _{JT}	Thermal characterization parameter, junction to package top outside	0.2	3	3	1.0	°C/W	6

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPB GA	Unit	Notes
		center (natural convection)						

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.4.3 Thermal attributes for 88 QFN

Board type	Symbol	Description	88 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	55	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	20	°C/W	1, 2
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	50	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	15	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	1	°C/W	5
—	Ψ_{JT}	Thermal characterization	1	°C/W	6

Peripheral operating requirements and behaviors

Board type	Symbol	Description	88 QFN	Unit	Notes
		parameter, junction to package top outside center (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation <ul style="list-style-type: none"> • Serial wire debug 	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width <ul style="list-style-type: none"> • Serial wire debug 	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

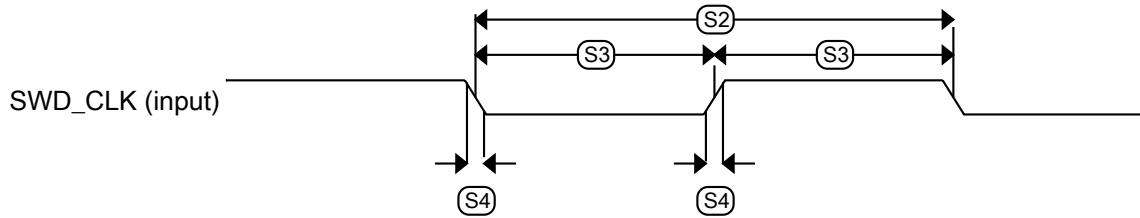


Figure 5. Serial wire clock input timing

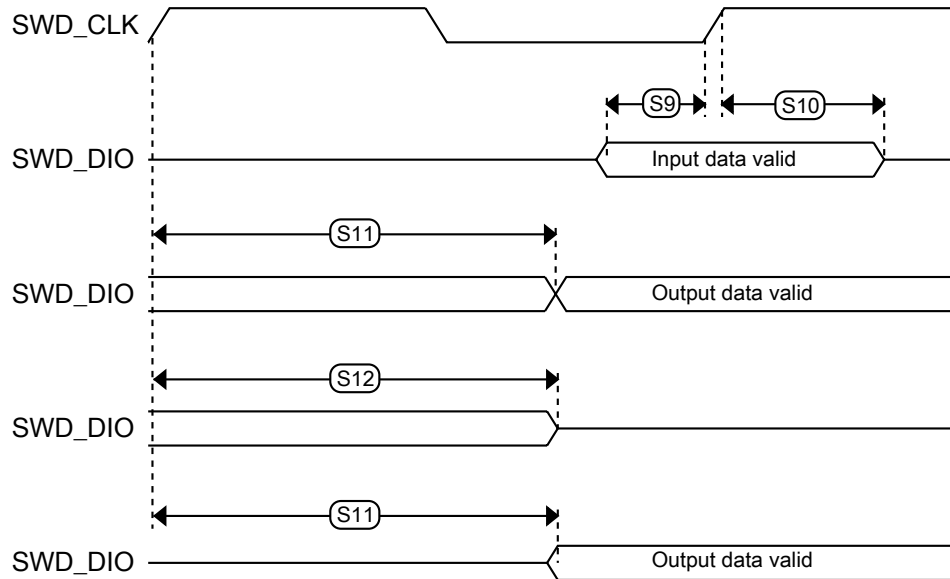


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG 	0 0	10 20	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width	50	—	ns

Table continues on the next page...

Table 14. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	<ul style="list-style-type: none"> Boundary Scan JTAG and CJTAG 	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	<ul style="list-style-type: none"> Boundary Scan JTAG and CJTAG 	0 0	10 15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	<ul style="list-style-type: none"> Boundary Scan JTAG and CJTAG 	50 33	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

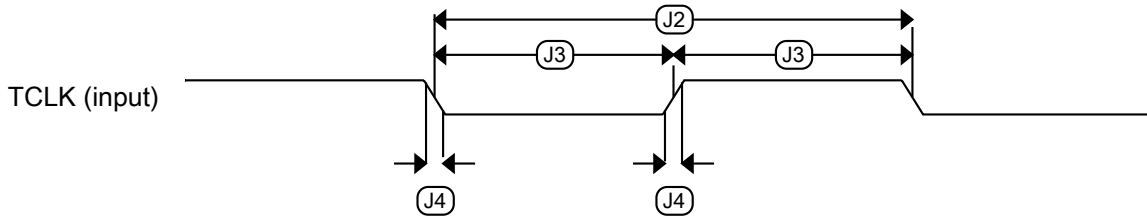


Figure 7. Test clock input timing

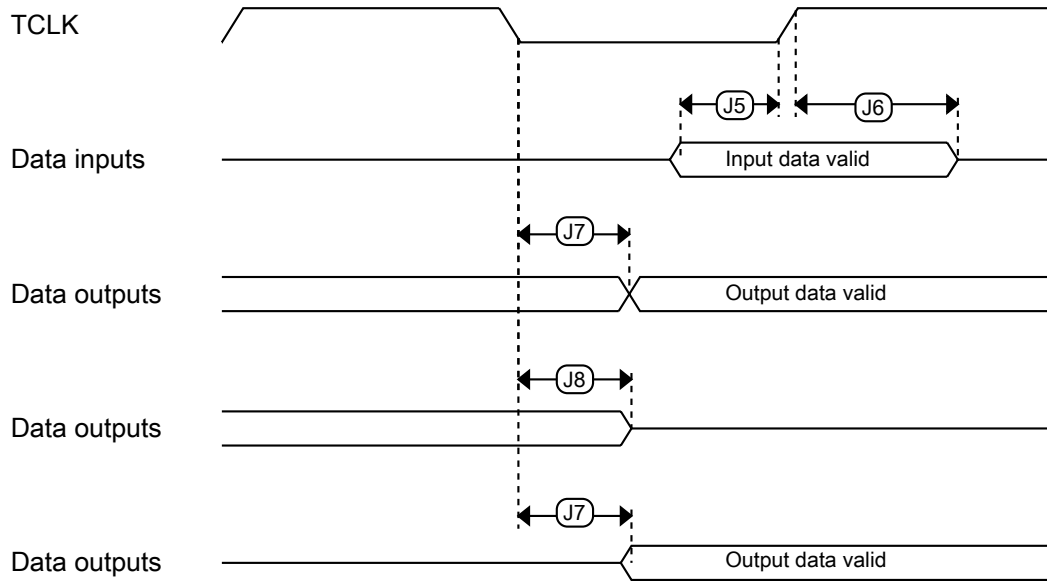


Figure 8. Boundary scan (JTAG) timing