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Kinetis K24F Sub-Family 256 KB Flash Data Sheet

120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K24F product family features high memory densities, low power capabilities, and optimized integration. It shares the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- 1-1 flash to RAM ratio, with 256 KB of embedded flash and 256 KB of embedded RAM to support application with high RAM density requirements.
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator and USB device crystal-less operation.
- Run power consumption down to 220 µA/MHz. Static power consumption down to 3.68 µA with full state retention and 5 µs wakeup. Lowest Static mode down to 173 nA

MK24FN256VDC12

121 XFBGA
8 x 8 x 0.5 mm Pitch 0.65 mm

Performance

- Up to 120 MHz ARM® Cortex®-M4 core with DSP instructions and floating point unit

Memories and memory interfaces

- Up to 256 KB program flash memory and 256 KB RAM
- Serial programming interface (EzPort)
- Pre-programmed Kinetis flashloader for one-time, in-system factory programming

System peripherals

- Multiple low-power modes, low-leakage wakeup unit
- 16-channel DMA controller
- External watchdog monitor
- Software watchdog

Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- Multipurpose clock generator with FLL and PLL
- 32 kHz, and 4 MHz internal reference clock
- 48 MHz internal reference

Analog modules

- Two 16-bit SAR ADCs
- 12-bit DAC
- Two analog comparators (CMP)
- Voltage reference

Communication interfaces

- USB full-/low-speed On-the-Go controller
- USB Device Charger detect (USBDCD)
- Three SPI modules
- Three I2C modules
- Six UART modules
- I2S module

Timers

- Two 8-channel motor control/general purpose/PWM timers
- Two 2-channel quadrature decoder/general purpose timers
- Periodic interrupt timers and 16-bit low power timer
- Carrier modulator transmitter
- Real-time clock
- Programmable delay block

Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): –40 to 105 °C

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM (KB)	
MK24FN256VDC12	256 KB	256	83

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K60PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K24P121M120SF5RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Package drawing	Package dimensions are provided in package drawings.	XFBGA 121-pin: 98ASA00595D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

Kinetis K24 Family

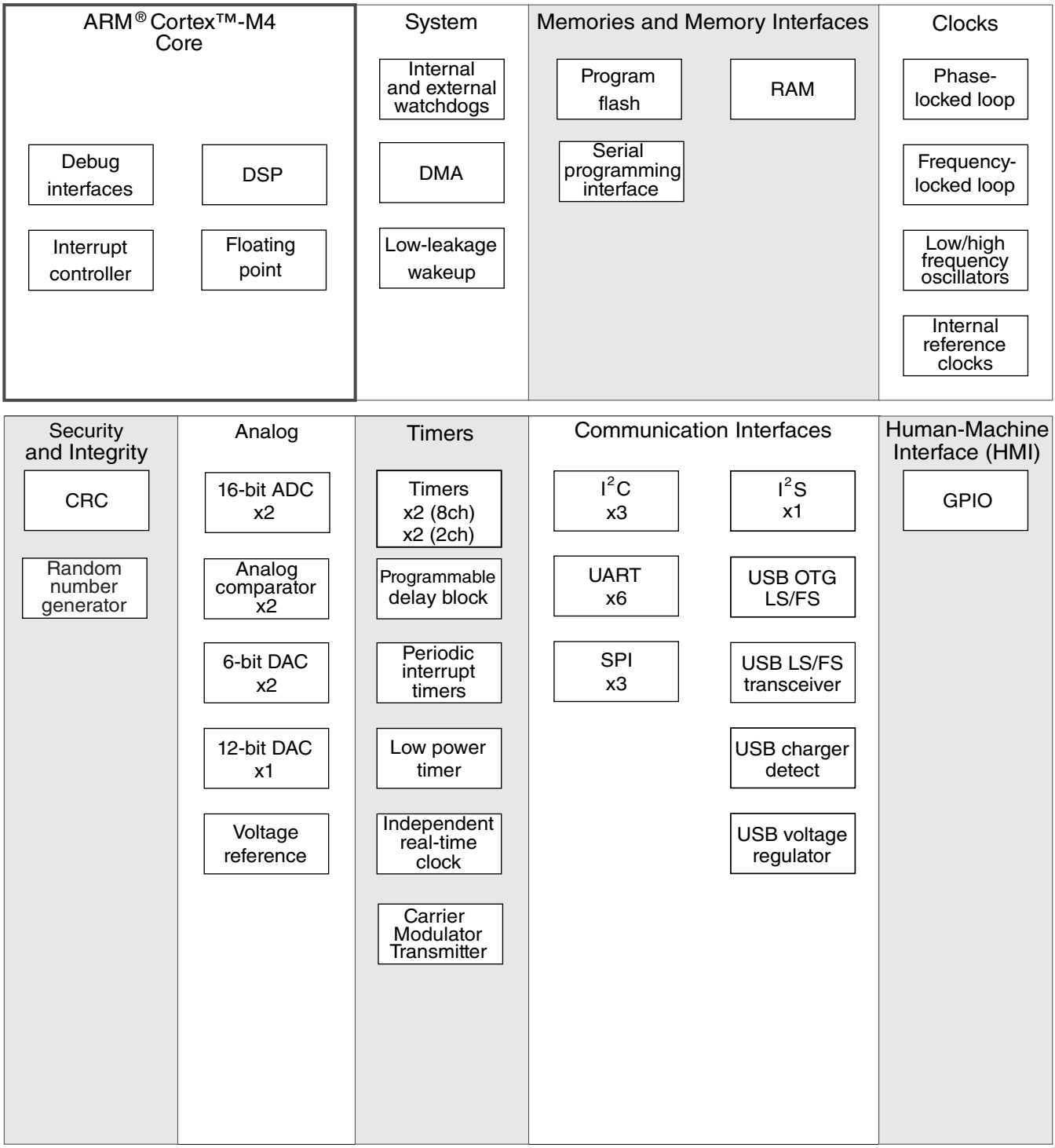


Figure 1. K24 block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 70 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

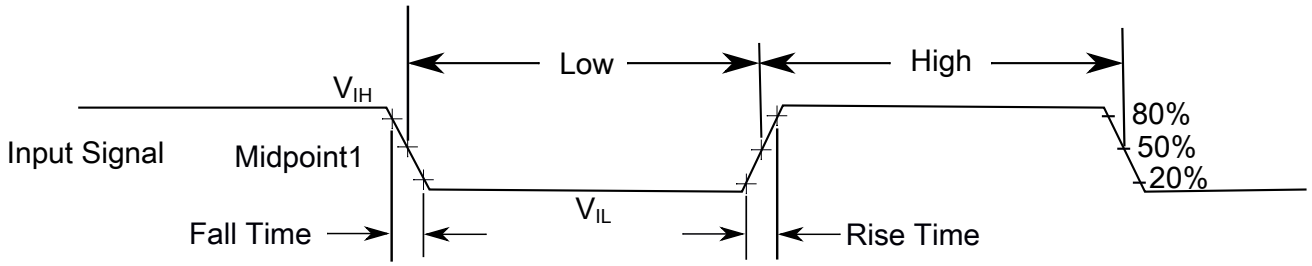
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25.0	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 x V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Analog[1], pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -3 —	 — +3	 mA	2
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	 mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	4

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
2. All analog and I/O pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{IO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
3. Open drain outputs must be pulled to VDD.
4. If VBAT is not used, the pin must be left floating.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1, 2
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage
2. , The reset state of the LVD is low range threshold. To utilize the LVD for the specified VDD range, change the LVD range to 'high range'.

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — High drive pad	$V_{DD} - 0.5$	—	V	1

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA				
	Output high voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage — normal drive pad	V_{BAT} – 0.5	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5 mA	V_{BAT} – 0.5	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -1.5 mA				
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	100	mA	
V_{OL}	Output low voltage — high drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
	Output low voltage — normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage — normal drive pad	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 5mA	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 1.5 mA				
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUP pins	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	2
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	µA	2
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) for full temperature range	—	1	µA	
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) at 25°C	—	0.025	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	0.25	µA	
$I_{OZ\_RTC\_WAKEUP}$	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)	—	0.25	µA	
R_{PU}	Internal pullup resistors (except RTC_WAKEUP pins)	20	50	kΩ	3
R_{PD}	Internal pulldown resistors (except RTC_WAKEUP pins)	20	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at VDD=3.6V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 → RUN	—	130	µs	
	• VLLS1 → RUN	—	130	µs	
	• VLLS2 → RUN	—	65	µs	
	• VLLS3 → RUN	—	65	µs	
	• LLS → RUN	—	4.9	µs	
	• VLPS → RUN	—	4.8	µs	
	• STOP → RUN	—	4.8	µs	

2.2.5 Power consumption operating behaviors

Important

Please note that these specifications are preliminary and as per design targets. These are subject to change.

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 3.0 V	—	27.3	38.8	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 3.0 V					
	• @ 25 °C					
	• @ 70 °C	—	35.6	39	mA	
	• @105 °C	—	36.46	41.39	mA	
		—	38.21	44.67	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	15.0	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.67	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.878	—	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.23	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.538	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25 °C	—	0.458	1.068	mA	
	• @ 70 °C	—	0.964	3.544	mA	
	• @105 °C	—	2.12	9.22	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25 °C	—	50.6	210.57	µA	
	• @ 70 °C	—	225.24	908.25	µA	
	• @105 °C	—	619.98	2273.88	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25 °C	—	3.68	13.03	µA	
	• @ 70 °C	—	14.14	49.34	µA	
	• @ 105 °C	—	51.57	183.11	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25 °C	—	3.02	5.53	µA	
	• @ 70 °C	—	12.06	37.57	µA	
	• @105 °C	—	43.59	140.76	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25 °C	—	1.73	2.26	µA	
	• @ 70 °C	—	3.98	9.36	µA	
	• @ 105 °C	—	13.09	37.68	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25 °C	—	0.777	0.97	µA	
	• @ 70 °C	—	2.14	4.7	µA	
	• @ 105 °C	—	8.52	25.22	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25 °C	—	0.360	0.56	µA	
	• @ 70 °C	—	1.67	4.29	µA	
	• @ 105 °C	—	7.91	24.37	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25 °C	—	0.173	0.246	µA	
	• @ 70 °C	—	1.41	2.25	µA	
	• @ 105 °C	—	7.42	17.02	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25 °C	—	0.18	0.21	µA	
	• @ 70 °C	—	0.66	0.81	µA	
	• @ 105 °C	—	2.92	3.92	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					10
	• @ 3.0 V					
	– @ –40 to 25 °C	—	0.71	0.86	µA	
	– @ 70 °C	—	1.22	1.66	µA	
	– @ 105 °C	—	3.50	5.53	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1.0 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1.0 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 256 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)				Unit
		-10	25	50	85	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.					nA
	VLLS1	440	490	540	560	
	VLLS3	440	490	540	560	
	LLS	490	490	540	560	
	VLPS	510	560	560	560	
	STOP	510	560	560	560	
I_{48MIRC}	48 Mhz internal reference clock	350	350	350	350	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

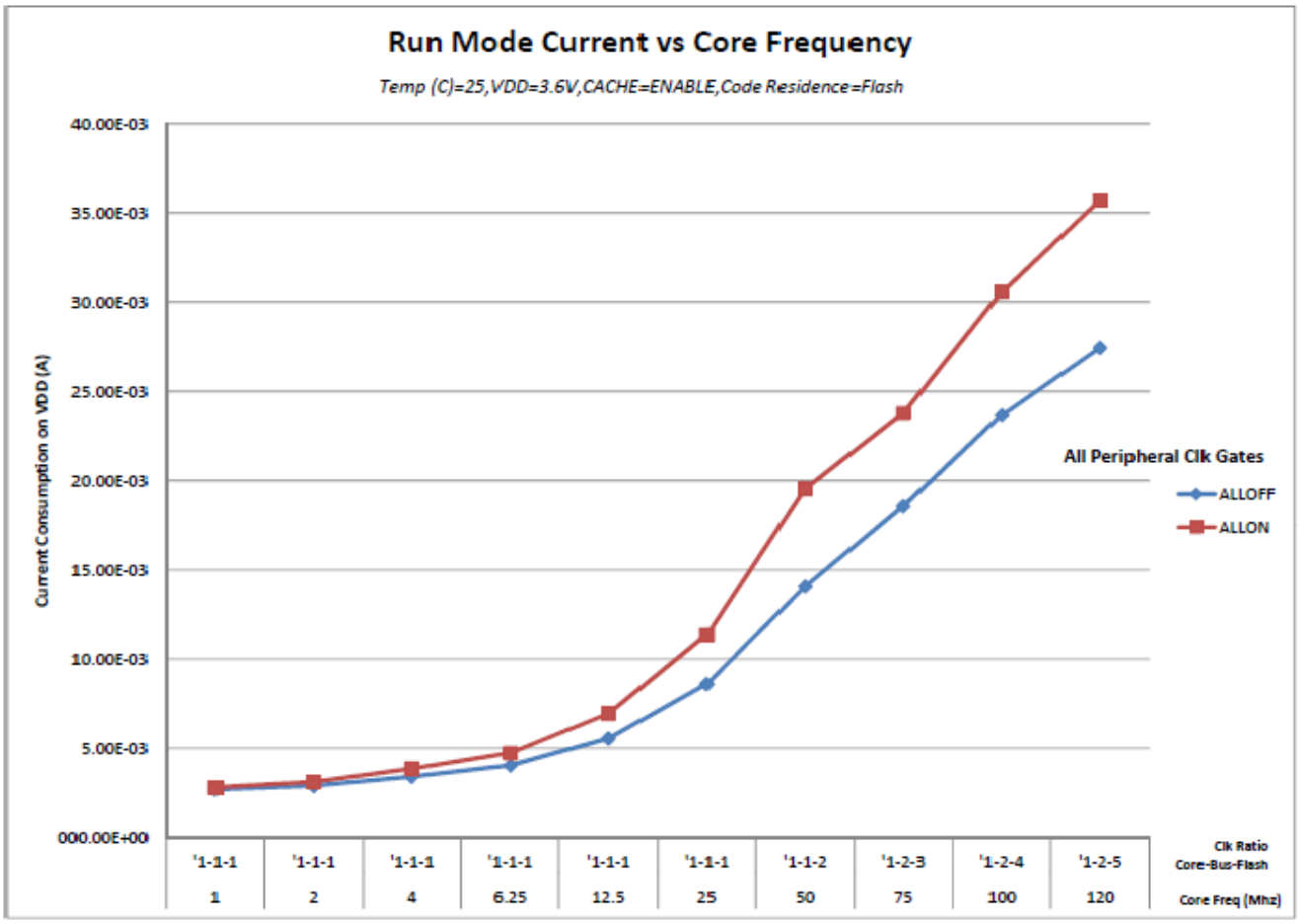


Figure 3. Run mode supply current vs. core frequency

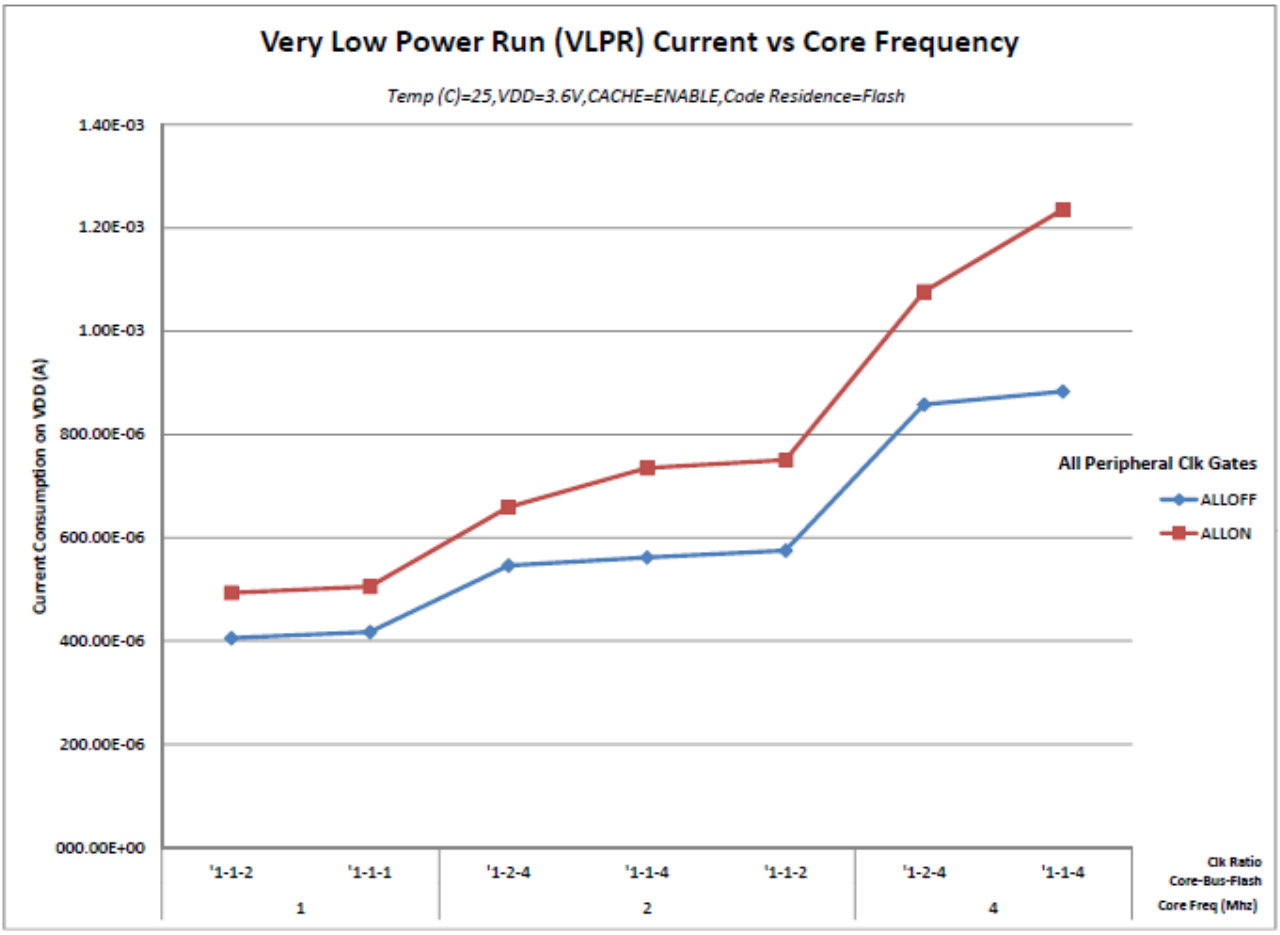


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
			121 XFBGA		
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	16	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	22	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	21	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic

application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 120 MHz, f_{BUS} = 60 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	60	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	0.8	MHz	

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	

	Port rise and fall time (high drive strength)
	• Slew disabled
	  • $1.71 \le V_{DD} \le 2.7$ V
	  • $2.7 \le V_{DD} \le 3.6$ V
	• Slew enabled
	  • $1.71 \le V_{DD} \le 2.7$ V
	  • $2.7 \le V_{DD} \le 3.6$ V
		
		—
		—
		
		—
		—
			
			10
			5
			
			30
			16
				
				ns
				ns
				
				ns
				ns
					4

	Port rise and fall time (low drive strength) • Slew disabled				5

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7$ V	—	10	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	5	ns	
	• Slew enabled	—	30	ns	
	• $1.71 \le V_{DD} \le 2.7$ V	—	16	ns	
	• $2.7 \le V_{DD} \le 3.6$ V				

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 25 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

2.4.2 Thermal attributes

Board type	Symbol	Description	121 XFBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	33.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	21.1	°C/W	1

Table continues on the next page...

Board type	Symbol	Description	121 XFBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	26.2	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	17.8	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.3	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	12	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	4

NOTES:

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 JTAG electricals

Table 13. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	33	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	15	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.0	—	ns
J7	TCLK low to boundary scan output data valid	—	32.8	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	26.5	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG limited voltage electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	33	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns

Table continues on the next page...

Table 14. JTAG limited voltage electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• JTAG and CJTAG • Serial Wire Debug	25 15	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

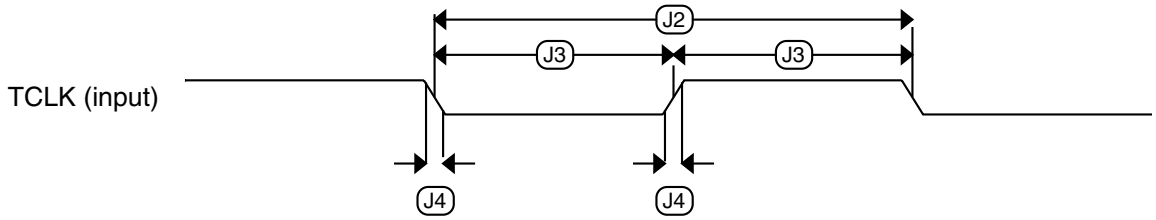


Figure 5. Test clock input timing

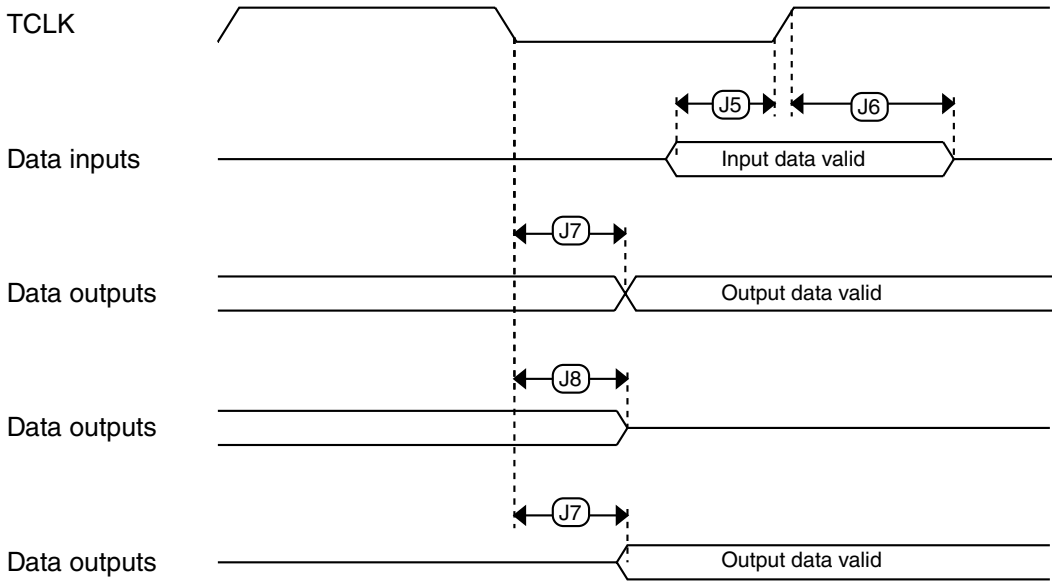


Figure 6. Boundary scan (JTAG) timing

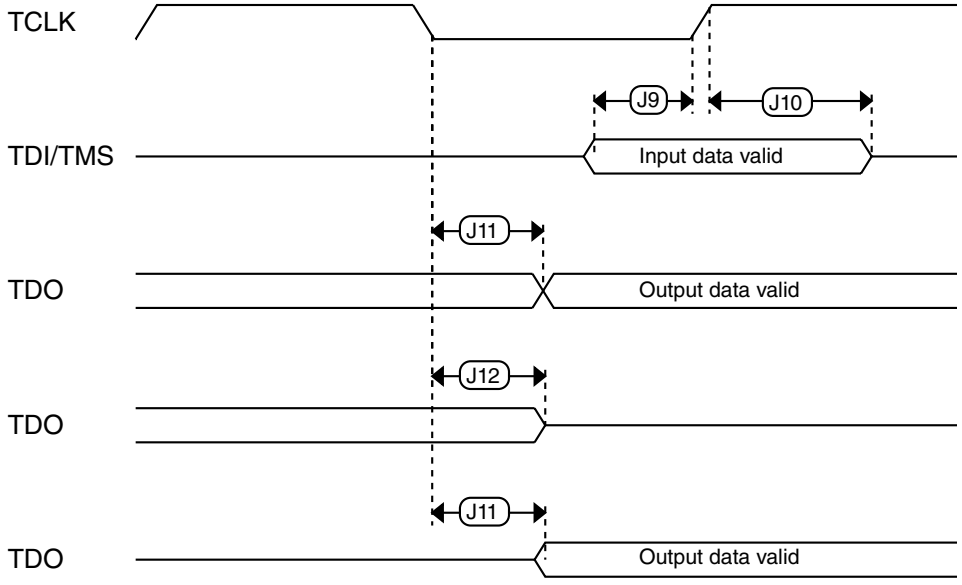


Figure 7. Test Access Port timing

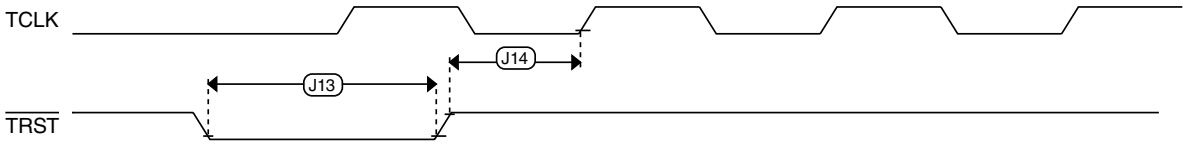


Figure 8. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	µA	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	$\%f_{dco}$	1 ,
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	25	—	µA	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	120	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	120	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)						8

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz • f_{vco} = 120 MHz	— —	1350 600	— —	ps ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 16. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature • Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	± 0.5 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	1

Table continues on the next page...