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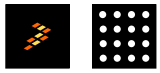
Kinetis K28F MCU Sub-Family

High performance ARM® Cortex®-M4 MCU with 2 MB Flash, 1 MB SRAM, 2 USB Controllers (High-Speed and Full-Speed), SDRAM controller, QuadSPI interface and Power Management Controller with Core Voltage Bypass.

MK28FN2M0CAU15R
MK28FN2M0VMI15

169 MAPBGA (MI)
9 x 9 x 1.28 mm Pitch 0.65 mm



210 WLCSP (AU)
6.9 mm x 6.9 x 0.6 mm Pitch 0.4 mm

K28F extends the Kinetis Micontroller portfolio with large embedded memory, advanced external memory interfaces, performance, and peripheral integration while maintaining a high level of software compatibility with previous Kinetis devices:

- The extended memory resources include a total of 2 MB of programmable flash and 1 MB of embedded SRAM which can be used to support application needs for data logging and rich human to machine interfaces with displays
- The Power Management Controller with Core Voltage Bypass enables the use of an external PMIC to maximize the power efficiency of the system
- K28F enables memory expansion leveraging the SDRAM controller and QuadSPI interface for eXecution-In-Place (XIP) from an external Serial NOR flash
- Both the USB High-Speed and Crystal-less Full-Speed Controllers integrate a PHY to reduce BOM cost
- The integrated smart peripherals such as Low-power UARTs and Timers operate in very low-power modes to optimize battery life of the system

Performance

- Up to 150 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit (FPU)

Memories and memory expansion

- 2 MB dual bank program flash and 1 MB SRAM
- 8 KB I/D + 8 KB System cache
- 32-bit external bus interface (FlexBus)
- 32-bit SDRAM controller
- Dual QuadSPI interface with eXecution-In-Place (XIP)
  - supports SDR and DDR serial flash and octal configurations
- 32 KB Boot ROM with built-in bootloader

System and Clocks

- 32-ch Asynchronous DMA
- Multiple low-power modes
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference
- Hardware and Software Watchdogs

Human-machine interface

- Up to 120 General-purpose input/output (GPIOs)

Analog modules

- Power Management Control (PMC) with Core Voltage Bypass
- One 16-bit SAR ADCs, two 6-bit DAC and one 12-bit DAC
- Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- 1.2 V Voltage reference

Timers

- One 4-ch 32-bit Periodic interrupt timer
- Two 16-bit low-power timer PWM modules
- Two 8-ch motor control/general purpose/PWM timers
- Two 2-ch quadrature decoder/general purpose timers
- Real-time clock with independent 3.6 V power domain
- Programmable delay block

Operating Characteristics

- Temperature range (ambient): -40 to 105°C (BGA)
  Temperature range (ambient):-40 to 85°C (WLCSP)

Security

- Hardware random-number generator
- Memory Mapped Crypto Acceleration Unit(MMCAU): DES, 3-DES, AES, SHA-1, SHA-256 and MD5 accelerator
- Cyclic Redundancy Check (CRC)

Target Applications

- Wearables
- Low-end graphic display system
- Cost-optimized multi-standard wireless smart home hubs
- Home Automation devices
- Consumer accessories

- Main V_{DD} Voltage and Flash write voltage range:1.71 V–3.6 V
- V_{DD_CORE}: 1.17 V–1.47 V
- Independent V_{DDIO_E} (QuadSPI):1.71 V–3.6 V
- Independent V_{BAT} (RTC): 1.71 V–3.6 V
- I/O Voltage range (V_{DD}): 1.71 V–3.6 V

Communication interfaces

- Two USB controllers:Crystal-less Full-/low-speed + transceiver Host and Device; High-/Full-/low-speed + PHY Host and Device
- Secure Digital Host Controller (SDHC)
- Two I2S modules, four I2C modules and five Low-Power UART modules
- Four SPI modules (SPI3 supports more than 40 Mbps)
- 32-ch Programmable module (FlexIO) to emulate various serial, parallel or custom interfaces

Ordering Information 1

Part Number	Embedded Memory		Package Type	Maximum number of I\O's
	Flash	SRAM		
MK28FN2M0VMI15	2 MB	1 MB	169 MAPBGA	120
MK28FN2M0CAU15R	2 MB	1 MB	210 WLCSP	120

1. To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Device Revision Number

Device Mask Set Number	SIM_SDID[REVID]	JTAG ID Register[PRN]
2N96T	0010	0010

Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	K2x Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K28P210M150SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_2N96T[1]
Package drawing	Package dimensions are provided in package drawings.	• MAPBGA 169-pin: 98ASA00628D[1] • WLCSP 210-pin: 98ASA01002D [1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

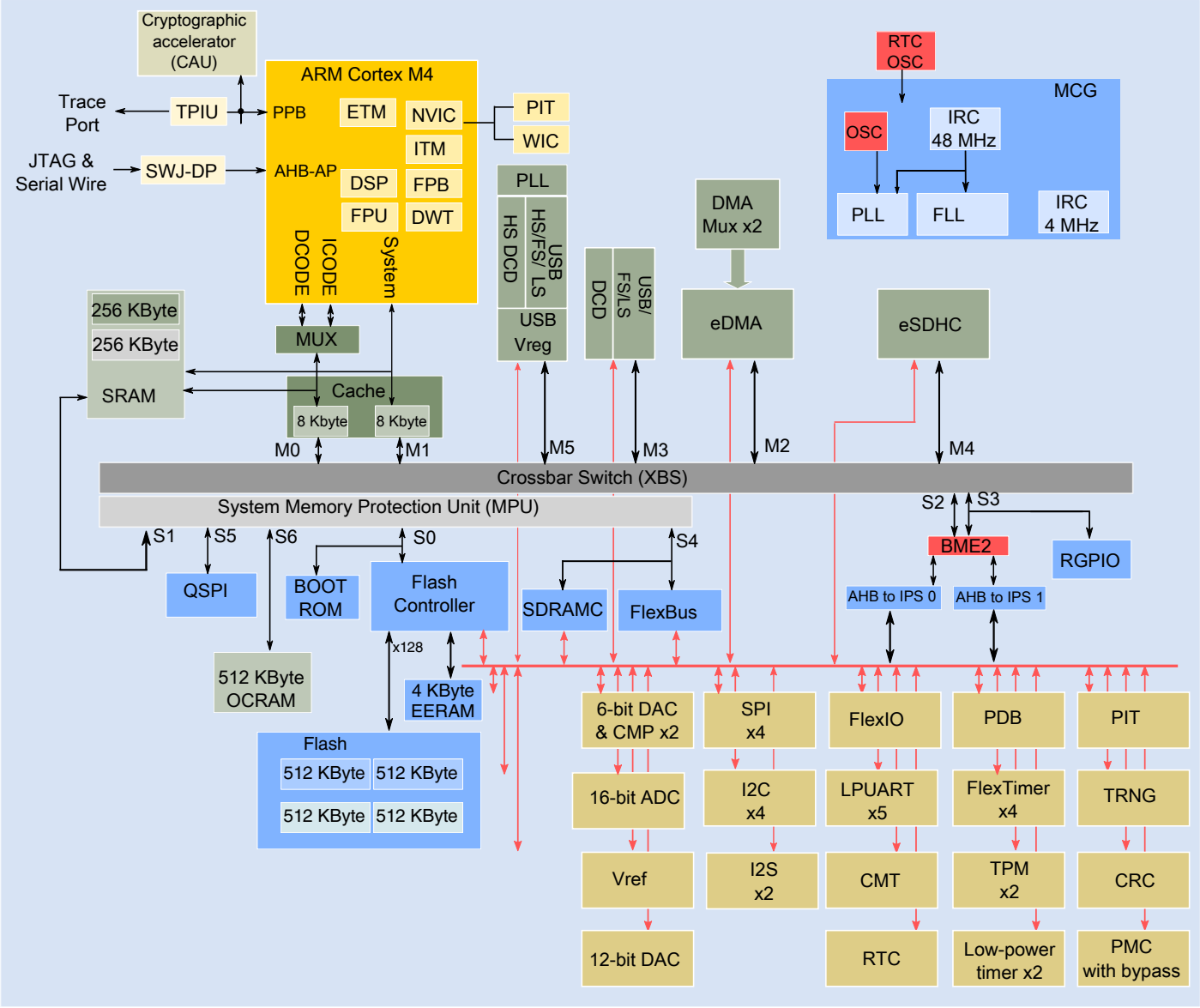


Figure 1. K28F Block Diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level (for V-temp variant)	—	3	—	1
MSL	Moisture sensitivity level (for C-temp variant)	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{DD_CORE}[1]	Internal digital logic supply voltage	– 0.3	1.47	V
V_{DD}	Digital supply voltage for Ports A, B,C,D	–0.3	3.8	V
V_{DDA}	Analog supply voltage	– 0.3	3.8	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [2]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V
V_{USB1_DPx}	USB1_DP and USB1_DM input voltage	–0.3	3.63	V

1. V_{DD_CORE} must not exceed V_{DD} on power up or power down
2. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}.

1.4.1 Recommended Power-On-Reset (POR) Sequencing

- V_{DD}/V_{DDIO_E} and V_{DD_CORE}

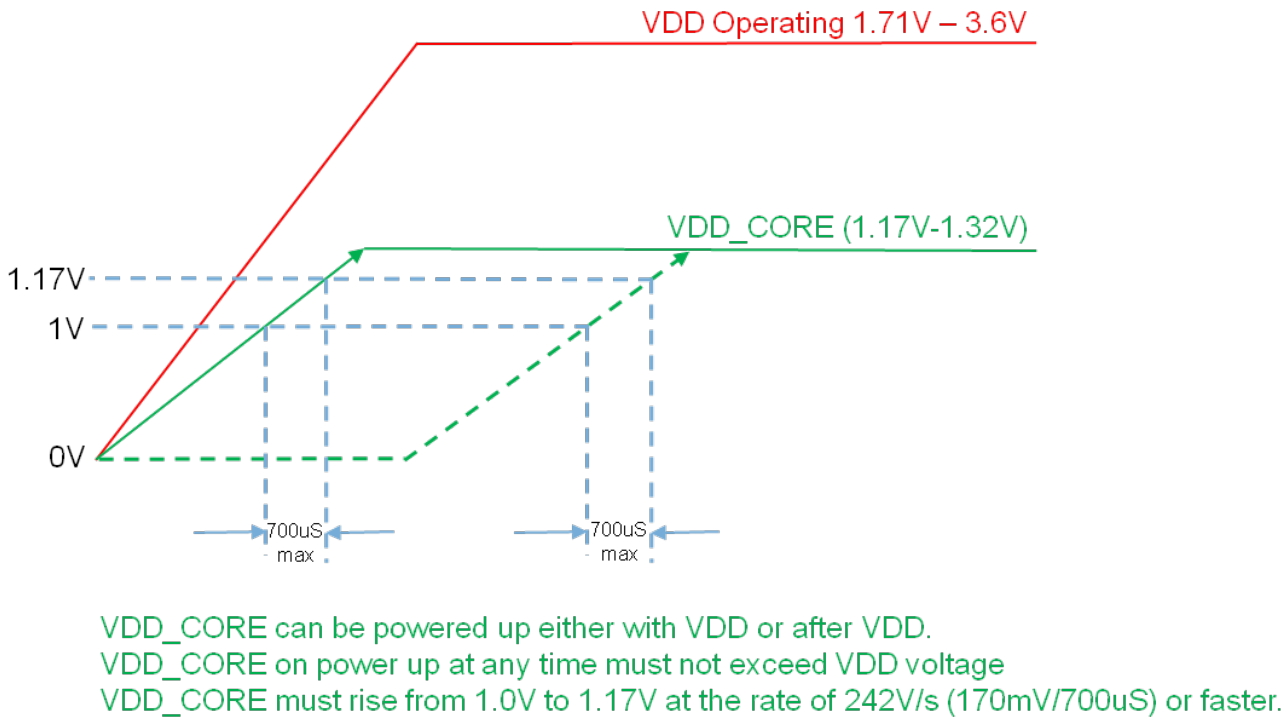

Figure 2. V_{DD_CORE}/ V_{DD} Powering sequence

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

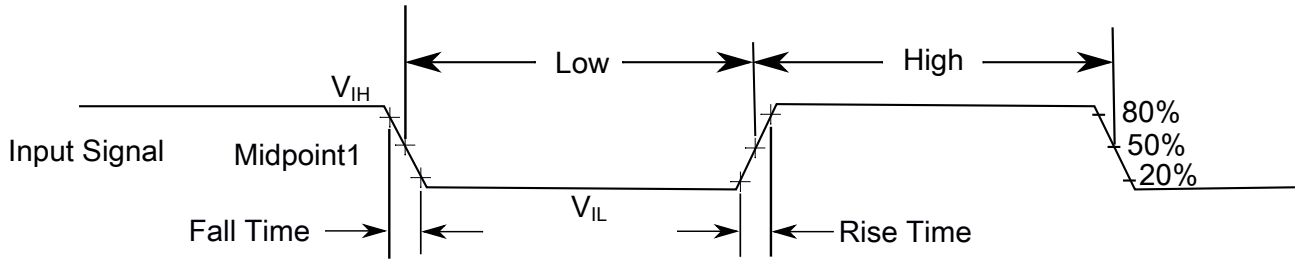

Figure 3. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
   - have C_L=15 pF loads,
   - are slew rate disabled, and
   - are normal drive strength
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD_CORE} (RUN)	Core and digital logic supply voltage for RUN mode	1.17	1.32	V	
V_{DD_CORE} (HSRUN)	Core and digital logic supply voltage for HSRUN	1.33	1.47	V	

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Digital supply voltage for Ports A, B, C,D	1.71	3.6	V	
V_{DDIO_E}	Digital Supply voltage for Port E	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{IH_E}	Input high voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	0.7 × V_{DDIO_E} 0.75 × V_{DDIO_E}	— —	V V	
V_{IL_E}	Input low voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	— —	0.35 × V_{DDIO_E} 0.3 × V_{DDIO_E}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
V_{HYS_E}	Input hysteresis	0.06 × V_{DDIO_E}	—	V	
I_{ICIO}	I/O pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Pseudo Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD_CORE} voltage required to retain RAM	1.14	1.47	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} or V_{DDIO_E}. If V_{IN} is less than -0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(-0.3-V_{IN})/|I_{ICIO}|$. The actual resistor value should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to VDD.

2.2.2 HVD, LVD and POR operating requirements

Table 2. V_{DD} supply HVD, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVDH}	High Voltage Detect (High Trip Point)	—	3.72	—	V	
V_{HVDL}	High Voltage Detect (Low Trip Point)	—	3.46	—	V	
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H} V_{LVW2H} V_{LVW3H} V_{LVW4H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L} V_{LVW2L} V_{LVW3L} V_{LVW4L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	1.74 1.84 1.94 2.04	1.80 1.90 2.00 2.10	1.86 1.96 2.06 2.16	V V V V	1
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

NOTE

There is no LVD circuit for V_{DDIO_E} and V_{DD_CORE} domain.

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive strength					2, 3
	IO Group 1					
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5 mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{BAT} – 0.5	—	—	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -5 mA	V_{DD} – 0.5	—	—	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -5 mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{DDIO_E} – 0.5	—	—	V	
	Output high voltage — High drive strength					2
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	V_{DD} – 0.5	—	—	V	
	IO Group 4	V_{DDIO_E} – 0.5	—	—	V	
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -15 mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -7.5 mA					
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — normal drive strength					2, 4, 5
	IO Group 1					
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = -5 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = -2.5 mA	—	—	0.5	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -10 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -5 mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -5 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -2.5 mA	—	—	0.5	V	
	Output low voltage — High drive strength					2, 4
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -20 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -10 mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -15 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -7.5 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current					6, 7, 8

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	V_{DD} domain pins • $V_{SS} \le V_{IN} \le V_{DD}$	— —	0.002 0.002	0.5 0.5	µA µA	
	PORTE pins • $V_{SS} \le V_{IN} \le V_{DDIO\_E}$	—	0.002	0.5	µA	
	V_{BAT} domain pins • $V_{SS} \le V_{IN} \le V_{BAT}$					
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	kΩ	9
R_{PD}	Internal pulldown resistors (except RTC_WAKEUP pins)	20	—	50	kΩ	10

1. Typical values characterized at 25°C and V_{DD} = 3.6V unless otherwise noted.
2. IO Group 1 includes V_{BAT} domain pins: RTC_WAKEUP_b. IO Group 2 includes V_{DD} domain pins: PORTA, PORTB, PORTC, and PORTD, except PTA4. IO Group 3 includes V_{DD} domain pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. IO Group 4 includes V_{DDIO_E} domain pins: PORTE.
3. PTA4 has lower drive strength: I_{OH} = -5 mA for high V_{DD} range; I_{OH} = -2.5 mA for low V_{DD} range.
4. Open drain outputs must be pulled to V_{DD}.
5. PTA4 has lower drive strength: I_{OL} = 5mA for high V_{DD} range; I_{OL} = 2.5mA for low V_{DD} range.
6. V_{DD} domain pins include ADC, CMP, and RESET_b inputs. Measured at V_{DD} = 3.6V.
7. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when $V_{DD} \ge V_{DDIO\_E}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{DD} < V_{DDIO\_E}$.
8. V_{BAT} domain pins include EXTAL32, XTAL32, and RTC_WAKEUP_b pins.
9. Measured at minimum supply voltage and $V_{IN} = V_{SS}$
10. Measured at minimum supply voltage and $V_{IN} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V and VDD_CORE reaches 1.17 V to execution of the first instruction across the operating temperature range of the chip.	—	1200	µs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• VLLS2 –> RUN	—	103	µs	
	• VLLS3 –> RUN	—	103	µs	
	• LLS2 –> RUN	—	6.3	µs	
	• LLS3 –> RUN	—	6.3	µs	
	• VLPS –> RUN	—	5.4	µs	
	• STOP –> RUN	—	5.4	µs	

2.2.5 Power consumption operating behaviors

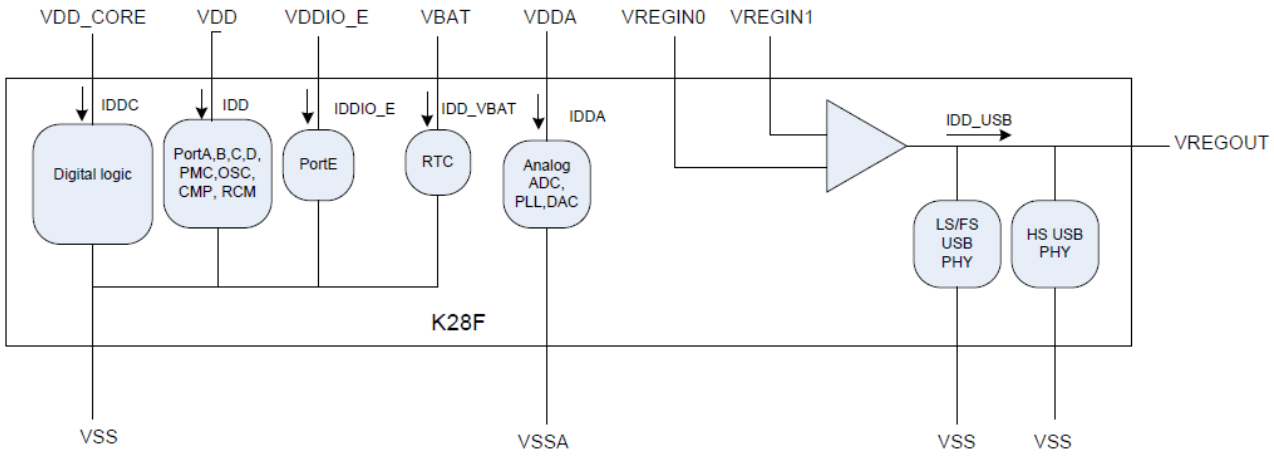

Figure 4. Power Supplies of K28F

The K28F device has several power supplies and the total current consumption of the device is the accumulative result of each individual power supplies' current consumption, dependent on the power mode of operation. (RUN, HSRUN, VLPR, Stop, VLLS3 etc.).

IDD_MCU_total = IDDC + IDD + IDDIO_E + IDD_VBAT + IDDA + IDD_USB

When calculating the total MCU current consumption considerations to external loads on the following should be made:

- On top of the device's IDD current consumption, external loads applied to Ports A,B,C and D need to be considered

- IDDIO_E current consumption is significantly dependent on external loads applied to Port E pins, and the internal current consumption in the device is negligible compared to IDD.
- The USB_VREG provides a 3.3 V output which can drive loads of upto 150 mA need to be considered.

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma). Table 6 details the IDDC values observed through the VDD_CORE supply and Table 7 details the IDD values observed through the VDD supply.

Table 6. Power consumption operating behaviors (through VDD_CORE)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DDC_RUN}	Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash at 1.2 V				mA	2
	• @ 25°C	—	31.0	35.1		
	• @ 70°C	—	37.9	51.6		
	• @ 85°C	—	42.7	63.6		
	• @ 105°C	—	51.9	85.7		
I_{DDC_RUN}	Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash at 1.2 V				mA	2
	• @ 25°C	—	41.6	47.1		
	• @ 70°C	—	48.0	65.5		
	• @ 85°C	—	52.6	78.4		
	• @ 105°C	—	61.1	100.9		
I_{DDC_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 1.2 V				mA	3
	• @ 25°C	—	28.5	32.4		
	• @ 70°C	—	35.5	48.4		
	• @ 85°C	—	40.3	60.1		
	• @ 105°C	—	49.5	81.6		
I_{DDC_HSRUN}	High-speed Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash at 1.4 V				mA	4
	• @ 25°C	—	42.6	49.6		
	• @ 70°C	—	53.5	74.9		

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD_CORE) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	59.7	91.3		
	• @ 105°C	—	71.7	121.0		
I_{DDC_HSRUN}	High-speed Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash at 1.4 V	—	54.3	63.3	mA	4
	• @ 25°C	—	65.7	91.9		
	• @ 70°C	—	71.5	109.8		
	• @ 85°C	—	82.6	139.0		
	• @ 105°C					
$I_{DDC\_HSRUNCO}$	High-speed Run mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 1.4 V	—	40.5	47.2	mA	3
	• @ 25°C	—	50.7	70.9		
	• @ 70°C	—	57.1	87.2		
	• @ 85°C	—	68.7	115.7		
	• @ 105°C					
I_{DDC_WAIT}	Wait mode high frequency current at 1.2 V— all peripheral clocks disabled	—	15.6	17.7	mA	2
	• @ 25°C	—	23.2	31.6		
	• @ 70°C	—	28.3	42.2		
	• @ 85°C	—	38.1	62.8		
	• @ 105°C					
I_{DDC_WAIT}	Wait mode reduced frequency current at 1.2 V— all peripheral clocks disabled	—	7.0	7.9	mA	5
	• @ 25°C	—	15.0	20.4		
	• @ 70°C	—	20.3	30.3		
	• @ 85°C	—	30.5	50.4		
	• @ 105°C					
I_{DDC_VLPR}	Very-low-power run mode current at 1.2 V — all peripheral clocks disabled, code of while(1) loop executing out of internal flash	—	1.2	3.9	mA	6
	• @ 25°C	—	2.6	7.1		
	• @ 70°C	—	3.8	9.7		
	• @ 85°C	—	6.2	15.0		
	• @ 105°C					

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD_CORE) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDC_VLPR}	Very-low-power run mode current at 1.2 V — all peripheral clocks enabled, code of while(1) loop executing out of internal flash				mA	6
	• @ 25°C	—	1.7	5.5		
	• @ 70°C	—	3.1	8.5		
	• @ 85°C	—	4.3	11.0		
	• @ 105°C	—	6.7	16.2		
I_{DDC_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 1 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 1.2 V				mA	7
	• @ 25°C	—	1.1	3.6		
	• @ 70°C	—	2.5	6.9		
	• @ 85°C	—	3.7	9.5		
	• @ 105°C	—	6.1	14.8		
I_{DDC_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 1.2 V				mA	3
	• @ 25°C	—	4.4	14.2		
	• @ 70°C	—	9.8	26.5		
	• @ 85°C	—	13.0	33.4		
	• @ 105°C	—	15.7	37.9		
I_{DDC_VLPW}	Very-low-power wait mode current at 1.2 V — all peripheral clocks disabled				mA	6
	• @ 25°C	—	0.759	2.5		
	• @ 70°C	—	2.2	5.9		
	• @ 85°C	—	3.3	8.6		
	• @ 105°C	—	5.8	14.0		
I_{DDC_VLPW}	Very-low-power wait mode current at 1.2 V— all peripheral clocks enabled				mA	6
	• @ 25°C	—	1.2	4.0		
	• @ 70°C	—	2.7	7.2		
	• @ 85°C	—	3.8	9.8		
	• @ 105°C	—	6.3	15.1		
I_{DDC_STOP}	Stop mode current at 1.2 V				mA	
	• @ 25°C	—	0.749	1.9		
	• @ 70°C	—	3.4	7.5		
	• @ 85°C	—	5.4	11.3		
	• @ 105°C	—	9.1	18.7		

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD_CORE) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDC_VLPS}	Very-low-power stop mode current at 1.2 V					
	• @ 25°C	—	0.452	1.2	mA	
	• @ 70°C	—	2.2	4.9		
	• @ 85°C	—	3.4	7.4		
	• @ 105°C	—	5.8	12.4		
I_{DDC_LLS3}	Low leakage stop mode current at 1.2 V					
	• @ 25°C	—	15.6	30.3	µA	
	• @ 70°C	—	129.0	189.5		
	• @ 85°C	—	244.9	347.8		
	• @ 105°C	—	535.0	737.3		
I_{DDC_LLS2}	Low leakage stop mode current at 1.2 V					8
	• @ 25°C	—	4.3	8.7	µA	
	• @ 70°C	—	33.8	57.3		
	• @ 85°C	—	62.8	104.0		
	• @ 105°C	—	135.6	205.8		
I_{DDC_VLLS3}	Very low-leakage stop mode 3 current at 1.2 V					
	• @ 25°C	—	13.5	26.0	µA	
	• @ 70°C	—	112.1	159.7		
	• @ 85°C	—	212.5	294.7		
	• @ 105°C	—	460.2	621.6		
I_{DDC_VLLS2}	Very low-leakage stop mode 2 current at 1.2 V					8
	• @ 25°C	—	0.552	0.9	µA	
	• @ 70°C	—	6.1	8.2		
	• @ 85°C	—	10.5	14.2		
	• @ 105°C	—	24.7	32.3		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled @ 3.0 V					
	• @ 25°C	—	0.266	0.319	µA	
	• @ 70°C	—	0.595	0.750		
	• @ 85°C	—	0.933	1.3		
	• @ 105°C	—	2.2	2.8		
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8 V				µA	9

Table 6. Power consumption operating behaviors (through VDD_CORE)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 25°C	—	0.454	0.546		
	• @ 70°C	—	0.724	0.897		
	• @ 85°C	—	1.1	1.4		
	• @ 105°C	—	2.0	2.6		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode.
3. MCG configured for PEE mode.
4. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode.
5. 25 MHz core and system clock, 25 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for FEI mode
6. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. Code executing from flash.
7. MCG configured for BLPE mode.
8. By default, this mode only has 32 K of SRAM enabled.
9. Includes 32 kHz oscillator current and RTC operation.

Table 7. Power consumption operating behaviors (through VDD)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V				mA	2
	• @ 25°C	—	1.5	1.6		
	• @ 70°C	—	1.5	1.7		

Table continues on the next page...

Table 7. Power consumption operating behaviors (through VDD) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	1.6	1.7		
	• @ 105°C	—	1.6	1.7		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	3
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V	—	2.0	2.1	mA	3
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V				mA	2
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	2.0	2.1	mA	1
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	2.0	2.1	mA	4
	• @ 25°C	—	2.0	2.1		
	• @ 70°C	—	2.0	2.1		
	• @ 85°C	—	2.0	2.1		
	• @ 105°C					

Table continues on the next page...

Table 7. Power consumption operating behaviors (through VDD) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled					5
	• @ 25°C	—	24.9	48.0	µA	
	• @ 70°C	—	31.2	70.1		
	• @ 85°C	—	39.6	84.5		
	• @ 105°C	—	63.9	157.5		
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled					5
	• @ 25°C	—	25.2	48.6	µA	
	• @ 70°C	—	31.5	70.6		
	• @ 85°C	—	40.0	85.0		
	• @ 105°C	—	64.3	158.4		
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, while(1) code executing from internal flash at 3.0 V					6
	• @ 25°C	—	8.3	16.0	µA	
	• @ 70°C	—	14.4	32.3		
	• @ 85°C	—	22.7	48.5		
	• @ 105°C	—	47.0	115.8		
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V					2
	• @ 25°C	—	1.8	3.5	mA	
	• @ 70°C	—	1.8	4.1		
	• @ 85°C	—	1.9	3.9		
	• @ 105°C	—	1.9	4.6		
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled					5
	• @ 25°C	—	24.9	47.8	µA	
	• @ 70°C	—	31.0	69.5		
	• @ 85°C	—	39.2	83.6		
	• @ 105°C	—	63.7	157.0		
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks enabled					5
	• @ 25°C	—	25.0	48.1	µA	
	• @ 70°C	—	31.2	70.0		

Table continues on the next page...

Table 7. Power consumption operating behaviors (through VDD) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	39.6	84.3		
	• @ 105°C	—	63.9	157.5		
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ 25°C	—	159.3	279.3	μA	
	• @ 70°C	—	173.8	341.8		
	• @ 85°C	—	181.4	358.4		
	• @ 105°C	—	251.2	735.0		
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ 25°C	—	3.1	5.6	μA	
	• @ 70°C	—	8.5	12.0		
	• @ 85°C	—	15.2	19.4		
	• @ 105°C	—	36.9	43.9		
I_{DD_LLS3}	Low leakage stop mode current at 3.0 V					
	• @ 25°C	—	2.9	4.7	μA	
	• @ 70°C	—	7.2	9.2		
	• @ 85°C	—	13.2	16.1		
	• @ 105°C	—	33.4	39.4		
I_{DD_LLS2}	Low leakage stop mode current at 3.0 V					7
	• @ 25°C	—	2.9	4.7	μA	
	• @ 70°C	—	7.2	9.2		
	• @ 85°C	—	13.2	16.1		
	• @ 105°C	—	33.4	39.4		
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ 25°C	—	2.2	3.4	μA	
	• @ 70°C	—	4.7	6.4		
	• @ 85°C	—	8.1	10.6		
	• @ 105°C	—	18.8	23.8		
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					7
	• @ 25°C	—	2.2	3.3	μA	
	• @ 70°C	—	4.5	6.1		

Table 7. Power consumption operating behaviors (through VDD)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 85°C	—	7.7	10.0		
	• @ 105°C	—	17.5	22.0		

1. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode.
2. MCG configured for PEE mode.
3. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode.
4. 25 MHz core and system clock, 25 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for FEI mode.
5. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. Code executing from flash.
6. MCG configured for BLPE mode.
7. By default, this mode has only 32K of SRAM enabled.

Below table list the current consumption adders for different SRAM configurations from the LLS2/VLLS2 (TYP) IDD values using a 32 KB SRAM retention referenced in Table 6.

Table 8. LLS2/VLLS2 additional Typical IDDC current consumption Adders

RAM array retained		@ 25°C	@ 85°C	@ 105°C	Unit
LLS2	RAM2: 32 KB	0.5	10.8	21.3	µA
	RAM3: 32 KB	0.5	11.0	21.5	µA
	RAM4: 32 KB	0.4	10.7	21.0	µA
	RAM5: 128 KB	1.4	28.1	57.6	µA
	RAM6: 64 KB	0.6	15.2	30.5	µA
	RAM7: 192 KB	2.1	41.1	85.1	µA
	RAM8: 256 KB	2.8	53.0	109.9	µA
	RAM9: 256 KB	2.3	53.5	110.9	µA
VLLS2	RAM2: 32 KB	0.5	9.1	19.7	µA
	RAM3: 32 KB	0.5	8.5	18.0	µA
	RAM4: 32 KB	0.5	8.1	16.8	µA
	RAM5: 128 KB	1.5	26.6	57.1	µA
	RAM6: 64 KB	0.8	12.9	27.1	µA
	RAM7: 192 KB	2.3	40.2	86.6	µA
	RAM8: 256 KB	3.0	52.9	114.3	µA
	RAM9: 256 KB	3.0	53.1	114.8	µA

Table 9. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS3	440	490	540	560	570	580	
	LLS2	490	490	540	560	570	680	
	LLS3	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{LPUART}	LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

2.2.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to nxp.com
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 10. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 11. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	150	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	100	—	MHz	
f_{BUS}	Bus clock	—	75	MHz	
f_{B_CLK}	FlexBus clock	—	75	MHz	
f_{FLASH}	Flash clock	—	28	MHz	

Table continues on the next page...

Table 11. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{B_CLK}	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, LPUART, CMT, timers, and I^2C signals.

Table 12. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7$ V • $2.7 \le V_{DD} \le 3.6$ V	 — — — —	 34 16 10 8	 ns ns ns ns	4, 5
	Port rise and fall time (low drive strength) • Slew enabled	 —	 34	 ns	6, 7

Table continues on the next page...

Table 12. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7$ V • $2.7 \le V_{DD} \le 3.6$ V	— —	16 7	ns ns	
	• Slew disabled • $1.71 \le V_{DD} \le 2.7$ V • $2.7 \le V_{DD} \le 3.6$ V	— —	5	ns	
	Port rise and fall time (high drive strength) • Slew enabled • $1.71 \le V_{DDIO\_E} \le 2.7$ V • $2.7 \le V_{DDIO\_E} \le 3.6$ V • Slew disabled • $1.71 \le V_{DDIO\_E} \le 2.7$ V • $2.7 \le V_{DDIO\_E} \le 3.6$ V	— — — —	34 16 7 5	ns ns ns ns	5, 8
	Port rise and fall time (low drive strength) • Slew enabled • $1.71 \le V_{DDIO\_E} \le 2.7$ V • $2.7 \le V_{DDIO\_E} \le 3.6$ V • Slew disabled • $1.71 \le V_{DDIO\_E} \le 2.7$ V • $2.7 \le V_{DDIO\_E} \le 3.6$ V	— — — —	34 16 7 5	ns ns ns ns	7, 8

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.
5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications