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Freescale Semiconductor
Data Sheet: Technical Data

Document Number K61P256M150SF3
Rev. 6, 09/2015

K61P256M150SF3

K61 Sub-Family

Supports the following:
MK61FX512VMJ15,
MK61FN1M0VMJ15

Key features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 150 MHz ARM® Cortex®-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 1024 KB program flash memory on non-FlexMemory devices
  - Up to 512 KB program flash memory on FlexMemory devices
  - Up to 512 KB FlexNVM on FlexMemory devices
  - 16 KB FlexRAM on FlexMemory devices
  - Up to 128 KB RAM
  - Serial programming interface (EzPort)
  - FlexBus external bus interface
  - DDR controller interface
  - NAND flash controller interface
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 32-channel DMA controller, supporting up to 128 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - Tamper detect and secure storage
  - Hardware random-number generator
  - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - Four 16-bit SAR ADCs
  - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
  - Two 12-bit DACs
  - Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Two 8-channel motor control/general purpose/PWM timers
  - Two 2-channel quadrature decoder/general purpose timers
  - IEEE 1588 timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect (USBDCD)
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital Host Controller (SDHC)
  - Two I2S modules

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK61 and MK61

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K61
A	Key attribute	• F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 512 = 512 KB • 1M0 = 1 MB

Table continues on the next page...

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK61FN1M0VMJ15

3 Terminology and guidelines

3.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

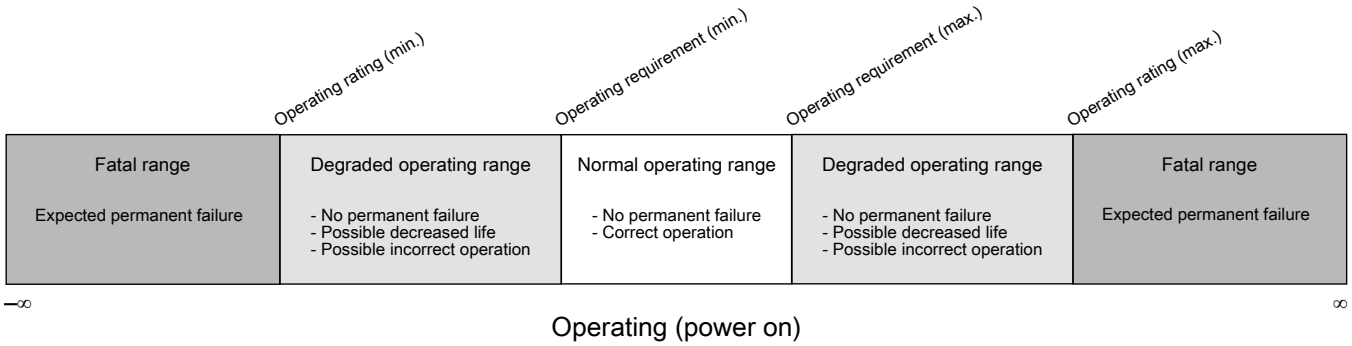
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

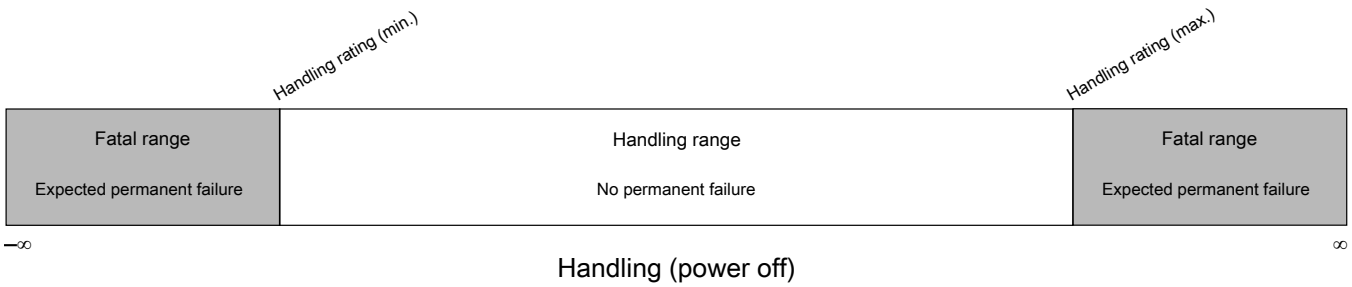
3.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

3.4 Relationship between ratings and operating requirements





3.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage[1]	–0.3	3.8	V
V_{DD_INT}	Core supply voltage	–0.3	3.8	V
V_{DD_DDR}	DDR I/O supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
I_{DD_INT}	Core supply current	—	185	mA
I_{DD_DDR}	DDR supply current	—	220	mA
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL0/XTAL0, and EXTAL1/XTAL1) [2]	–0.3	5.5	V
V_{DDDR}	DDR input voltage	–0.3	V_{DD_DDR} + 0.3	V
V_{AIO}	Analog[3], $\overline{RESET}$, EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. It applies for all port pins except Tamper pins.
2. It covers digital pins except Tamper pins and DDR pins.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

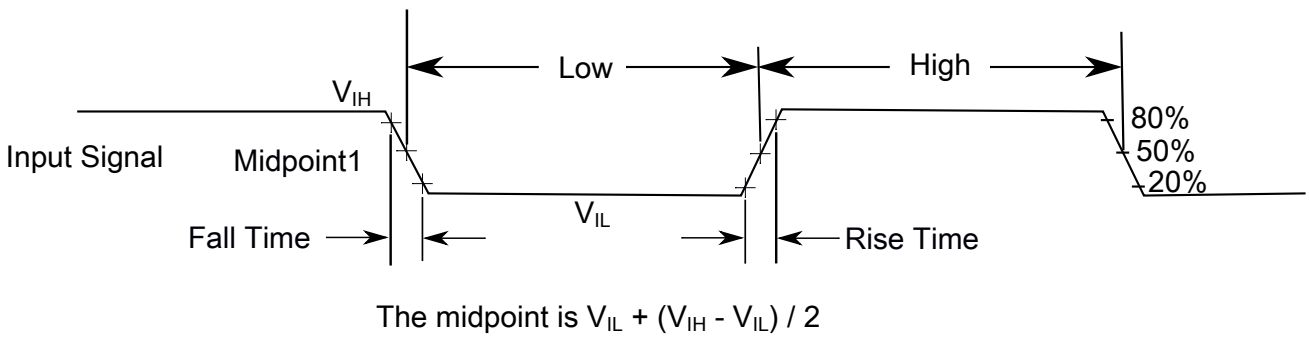


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
   - have C_L=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	max [V_{DD_DDR}, 1.71 V]	3.6	V	
V_{DD_INT}	Core supply voltage	1.71	V_{DD}	V	
V_{DD_DDR}	DDR voltage — memory I/O buffers • DDR1 • DDR2/LPDDR1	 2.3 1.71	 2.7 1.9	 V V	
V_{REF_DDR}	Input reference voltage (DDR1/DDR2/ LPDDR1)	0.49 × V_{DD_DDR}	V_{DD_DDR}	V	1
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage (digital pins except Tamper pins and DDR pins) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage (digital pins except Tamper pins and DDR pins) • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{IH_DDR}	Input high voltage (DDR pins) • DDR1 • DDR2 • LPDDR1	 V_{REF_DDR} + 0.15 V_{REF_DDR} + 0.125 0.7 × V_{DD_DDR}	 — — —	 V V V	
V_{IL_DDR}	Input low voltage (DDR pins) • DDR1 • DDR2 • LPDDR1	 — — —	 V_{REF_DDR} – 0.15 V_{REF_DDR} – 0.125 0.3 × V_{DD_DDR}	 V V V	
V_{HYS}	Input hysteresis (digital pins except Tamper pins and DDR pins)	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin (except Tamper pins) negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	2
I_{ICAIO}	Analog[3], EXTAL0/XTAL0, and EXTAL1/ XTAL1 pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -5 —	 — +5	mA	4

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	-25 —	— +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	5
V_{RAM}	V_{DD} (V_{DD_INT}) voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. For DDR1/DDR2, connect V_{REF_DDR} to the same reference voltage used for the memory. For LPDDR1, connect V_{REF_DDR} to the V_{DD_DDR} voltage.
2. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than V_{DIO_MIN}, a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO\_MIN}-V_{IN})/|I_{ICDIO}|$.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
4. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
5. Open drain outputs must be pulled to VDD.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H} V_{LVW2H} V_{LVW3H} V_{LVW4H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00) • Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	2.62 2.72 2.82 2.92	2.70 2.80 2.90 3.00	2.78 2.88 2.98 3.08	V V V V	1
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L} V_{LVW2L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00)	1.74 1.84	1.80 1.90	1.86 1.96	V V	1

Table continues on the next page...

Table 2. LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW3L} V_{LVW4L}	• Level 2 falling (LVWV=01) • Level 3 falling (LVWV=10) • Level 4 falling (LVWV=11)	1.94 2.04	2.00 2.10	2.06 2.16	V V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	— — 	 V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	— — 	 V V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{OHT_io60}	Output high current total for fast digital ports	—	—	100	mA	
V_{OH_DDR}	Output high voltage for DDR pins • DDR1 (I_{OH} = -16.2 mA) • DDR2 half strength (I_{OH} = -5.36 mA) • DDR2 full strength (I_{OH} = -13.4 mA) • LPDDR1 half strength (I_{OH} = -0.1 mA) • LPDDR1 full strength (I_{OH} = -0.1 mA)	V_{DD_DDR} - 0.36 V_{DD_DDR} - 0.28 V_{DD_DDR} - 0.28 0.9 x V_{DD_DDR} 0.9 x V_{DD_DDR}	— — — — —	— — — — —	V V V V V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OHT_DDR}	Output high current total for DDR pins • DDR1 • DDR2 • LPDDR1	— — —	— — —	100 56 39	mA mA mA	
V_{OH_Tamper}	Output high voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	— —	— —	0.5 0.5	V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	— —	— —	0.5 0.5	V V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
V_{OL_DDR}	Output low voltage for DDR pins • DDR1 (I_{OL} = 16.2 mA) • DDR2 half strength (I_{OL} = 5.36 mA) • DDR2 full strength (I_{OL} = 13.4 mA) • LPDDR1 half strength (I_{OL} = 0.1 mA) • LPDDR1 full strength (I_{OL} = 0.1 mA)	— — — — —	— — — — —	0.37 0.28 0.28 0.1 x V_{DD_DDR} 0.1 x V_{DD_DDR}	V V V V V	
I_{OLT_DDR}	Output low current total for DDR pins • DDR1 • DDR2 • LPDDR1	—	—	100 56 39	mA mA mA	
V_{OL_Tamper}	Output low voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA	— —	— —	0.5 0.5	V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA	— —	— —	0.5 0.5	V V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs • $V_{SS} \leq V_{IN} \leq V_{DD}$ • All pins except EXTAL32, XTAL32, EXTAL, XTAL • EXTAL (PTA18) and XTAL (PTA19) • EXTAL32, XTAL32	 — — —	 0.002 0.004 0.075	 0.5 1.5 10	 μA μA μA	1, 2
I_{IND}	Input leakage current, digital pins • $V_{SS} \leq V_{IN} \leq V_{IL}$ • All digital pins • $V_{IN} = V_{DD}$ • All digital pins except PTD7 • PTD7	 — — —	 0.002 0.002 0.004	 0.5 0.5 1	 μA μA μA	2, 3
I_{IND}	Input leakage current, digital pins • $V_{IL} < V_{IN} < V_{DD}$ • $V_{DD} = 3.6$ V • $V_{DD} = 3.0$ V • $V_{DD} = 2.5$ V • $V_{DD} = 1.7$ V	 — — — —	 18 12 8 3	 26 19 13 6	 μA μA μA μA	2, 3, 4
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	 —	 1	 50	 μA	2, 3
Z_{IND}	Input impedance examples, digital pins • $V_{DD} = 3.6$ V • $V_{DD} = 3.0$ V • $V_{DD} = 2.5$ V • $V_{DD} = 1.7$ V	 — — — —	 — — — —	 48 55 57 85	 kΩ kΩ kΩ kΩ	2, 5
I_{IN_DDR}	Input leakage current (per DDR pin) for full temperature range	—	—	1	μA	
I_{IN_DDR}	Input leakage current (per DDR pin) at 25°C	—	—	0.025	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	μA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	—	50	kΩ	6
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	—	50	kΩ	7
R_{ODT}	On-die termination (ODT) resistance for DDR2 • $R_{tt1(eff)}$ - 75 Ω • $R_{tt2(eff)}$ - 150 Ω	60 120	— —	90 180	Ω Ω	

General

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
7. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

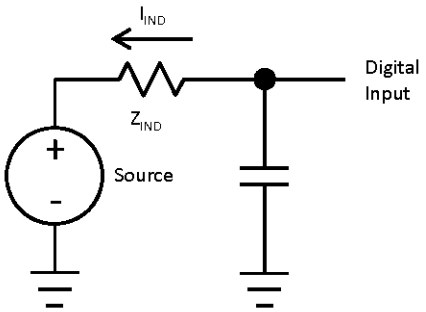


Figure 2. 5 V Tolerant Input IIND Parameter

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s	— —	300 1.7 V / (V_{DD} slew rate)	µs	1
	• VLLS1 → RUN	—	160	µs	
	• VLLS2 → RUN	—	114	µs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• VLLS3 → RUN	—	114	μs	
	• LLS → RUN	—	5.0	μs	
	• VLPS → RUN	—	5	μs	
	• STOP → RUN	—	4.8	μs	

1. Normal boot (FTFE_FOPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	58.01	83.95	mA	
	• @ 3.0V	—	57.93	84.14	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3
	• @ 1.8V	—	89.26	116.53	mA	
	• @ 3.0V	—	89.23	117.26	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	40.18	65.25	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	18.08	42.96	mA	4
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	1.25	1.62	mA	
	• @ 70°C	—	2.93	4.39	mA	
	• @ 105°C	—	7.08	10.74	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.03	4.48	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.58	4.96	mA	5
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	0.64	4.29	mA	5
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.22	0.38	mA	
		—	0.78	1.33	mA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 70°C • @ 105°C	— —	2.18 —	3.56 —	mA —	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 0.22 0.78 2.16	 0.37 1.33 3.52	 mA mA mA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 4.09 20.98 84.95	 5.58 28.93 111.15	 μA μA μA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 2.68 8.8 37.28	 4.22 10.74 43.61	 μA μA μA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 2.46 7.04 30.68	 4.02 8.99 37.04	 μA μA μA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 0.89 1.28 3.10	 1.10 1.85 4.30	 μA μA μA	6

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 150 MHz core and system clock, 75 MHz bus, 50 MHz FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 150 MHz core and system clock, 75 MHz bus, 50 MHz FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.
5. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
6. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode at greater than 100 MHz frequencies.

- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

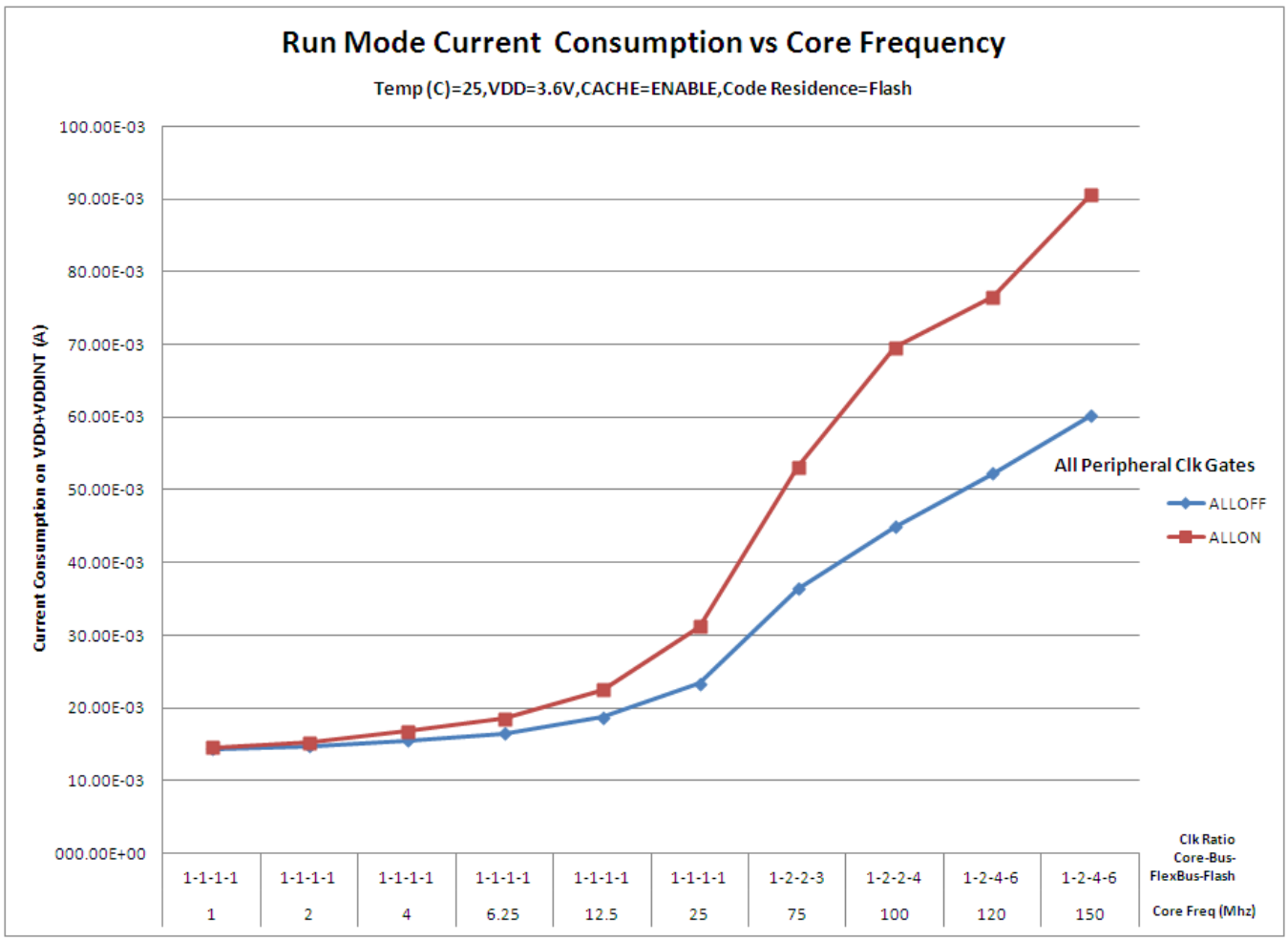


Figure 3. Run mode supply current vs. core frequency

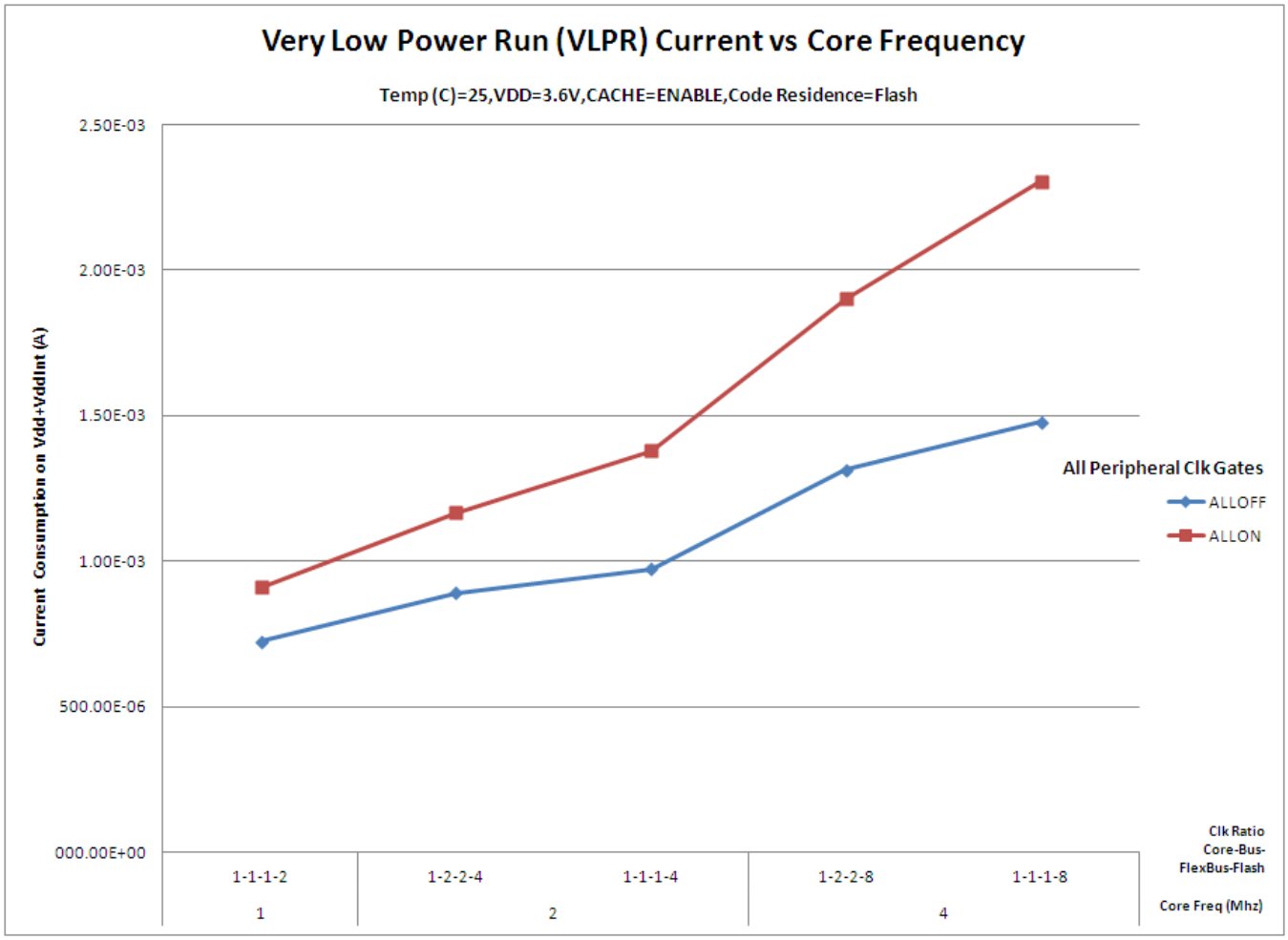


Figure 4. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 256MAPBGA

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	21	dBμV	1, 2, 3
V_{RE2}	Radiated emissions voltage, band 2	50–150	24	dBμV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	29	dBμV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	28	dBμV	

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 72 MHz, f_{BUS} = 72 MHz
3. Determined according to IEC Standard JESD78, *IC Latch-Up Test*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	150	MHz	
f_{SYS_USBFS}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	60	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	
f_{BUS}	Bus clock	—	75	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{DDR}	DDR clock	—	150	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	0.5	MHz	
f_{LPTMR}	LPTMR clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength)				4
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	14	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	8	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	
	Port rise and fall time (low drive strength)				5
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	14	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	8	ns	
	• Slew enabled				
		—	36	ns	

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	—	24	ns	
t_{io50}	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 7 3 28 14	 ns ns ns ns	6 — — — —
t_{io50}	Port rise and fall time (low drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 18 9 48 24	 ns ns ns ns	7 — — — —
t_{io60}	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 6 3 28 14	 ns ns ns ns	6 — — — —
t_{io60}	Port rise and fall time (low drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 18 6 48 24	 ns ns ns ns	7 — — — —

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load
6. 25 pF load

7. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

5.4.2 Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	25	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center	2	°C/W	6

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
		(natural convection)			

NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

5.5 Power sequencing

Voltage supplies must be sequenced in the proper order to avoid damaging internal diodes. There is no limit on how long after one supply powers up before the next supply must power up. Note that V_{DD} and V_{DD_INT} can use the same power source.

The power-up sequence is:

1. V_{DD}/V_{DDA}
2. V_{DD_INT}
3. V_{DD_DDR}

The power-down sequence is the reverse:

1. V_{DD_DDR}
2. V_{DD_INT}
3. V_{DD}/V_{DDA}