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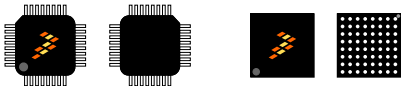
Kinetis K63F Sub-Family Data Sheet

120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

MK63FN1M0VLQ12
MK63FN1M0VMD12



144 LQFP
20 x 20 x 1.6 mm Pitch
0.5 mm

144 MAPBGA
13 x 13 x 1.46 mm
Pitch 1 mm

The K63 product family members are optimized for cost-sensitive applications requiring low-power, USB/Ethernet connectivity, up to 256 KB of embedded SRAM and the need for extensive tamper protection, such as Electronic Point of Sales. These devices share the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- Run power consumption down to 250 µA/MHz. Static power consumption down to 5.8 µA with full state retention and 5 µs wakeup. Lowest Static mode down to 339 nA
- DryIce Tamper Detection with active/passive pin, temperature, clock, supply voltage monitoring
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO Vreg, with USB device crystal-less operation
- 10/100 Mbit/s Ethernet MAC with MII and RMII interfaces

Performance

- Up to 120 MHz ARM® Cortex®-M4 core with DSP instructions and floating point unit

Memories and memory interfaces

- Up to 1 MB program flash memory and 256 KB RAM
- FlexBus external bus interface

System peripherals

- Multiple low-power modes, low-leakage wake-up unit
- Memory protection unit with multi-master protection
- 16-channel DMA controller
- External watchdog monitor and software watchdog

Security and integrity modules

- Hardware CRC module
- Tamper detect and secure storage
- Hardware random-number generator
- Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- 128-bit unique identification (ID) number per chip

Analog modules

- Two 16-bit SAR ADCs
- Two 12-bit DACs
- Three analog comparators (CMP)
- Voltage reference

Communication interfaces

- Ethernet controller with MII and RMII interface
- USB full-/low-speed On-the-Go controller
- Controller Area Network (CAN) module
- Three SPI modules
- Three I2C modules. Support for up to 1 Mbit/s
- Six UART modules
- Secure Digital Host Controller (SDHC)
- I2S module

Timers

- Two 8-channel Flex-Timers (PWM/Motor control)
- Two 2-channel FlexTimers (PWM/Quad decoder)
- IEEE 1588 timers
- 32-bit PITs and 16-bit low-power timers
- Real-time clock
- Programmable delay block

Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- PLL, FLL, and multiple internal oscillators
- 48 MHz Internal Reference Clock (IRC48M)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): –40 to 105°C

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM (KB)	
MK63FN1M0VLQ12	1 MB	256	100
MK63FN1M0VMD12	1 MB	256	95

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K60PB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K63P144M120SF5RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K63P144M120SF5[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 144-pin: 98ASS23177W[1] • MAPBGA 144-pin: 98ASA00222D[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

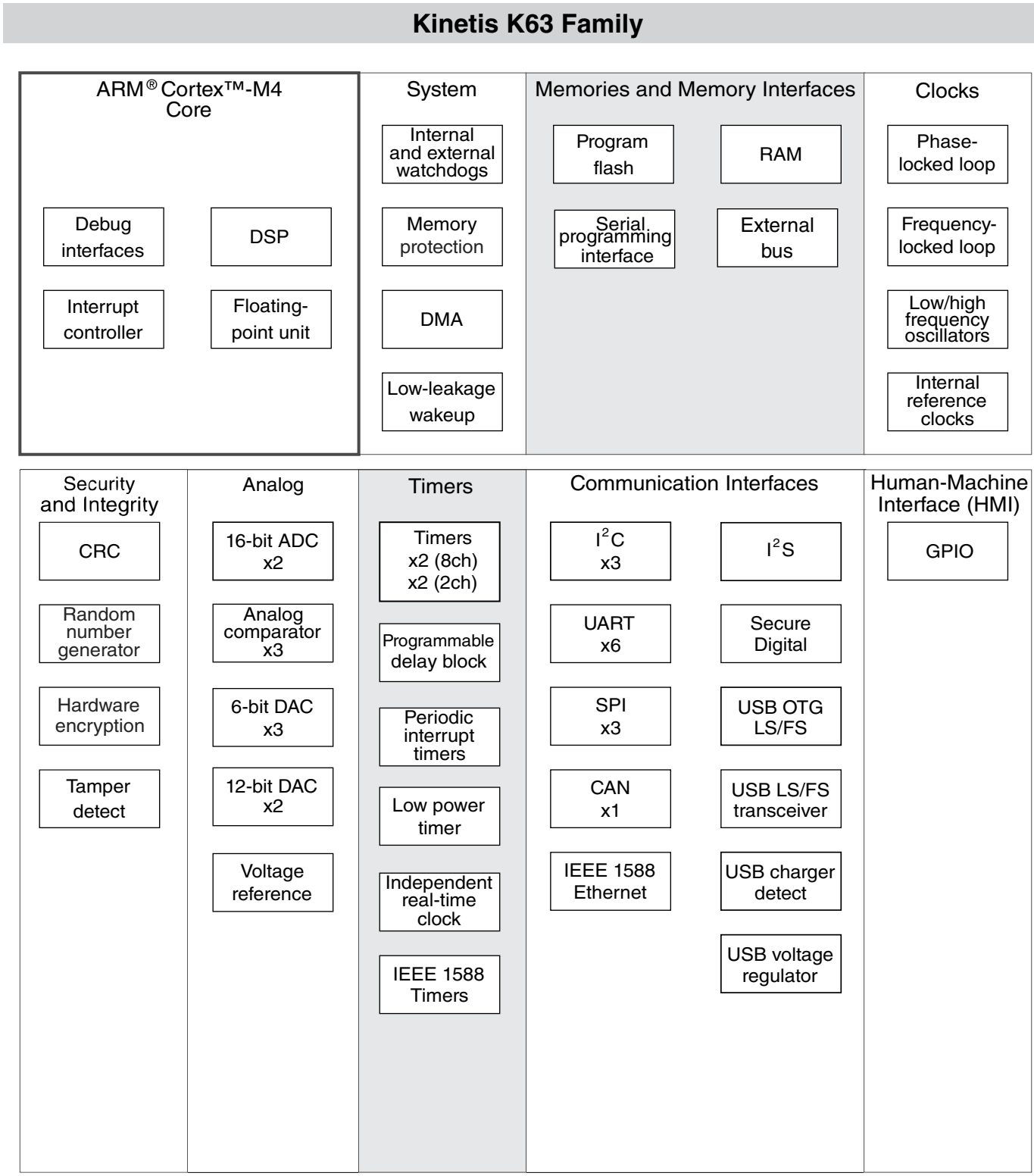


Figure 1. K63 block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

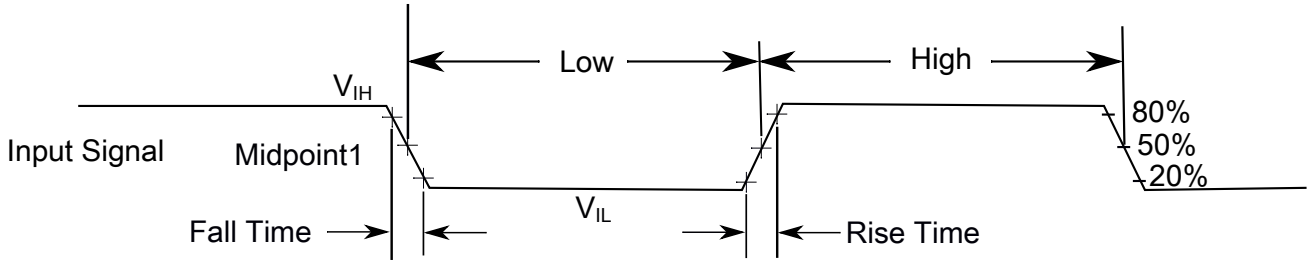
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	5.5	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin (except Tamper pins) negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -5 —	 — +5	mA	3
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	4
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than V_{DIO_MIN}, a current limiting resistor is required. If V_{IN} greater than V_{DIO_MIN} (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO\_MIN}-V_{IN})/|I_{ICDIO}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
4. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -8mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OH_Tamper}	Output high voltage — high drive strength	V_{BAT} – 0.5	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA	V_{BAT} – 0.5	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA				
	Output high voltage — low drive strength	V_{BAT} – 0.5	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA	V_{BAT} – 0.5	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA				
I_{OH_Tamper}	Output high current total for Tamper pins	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
V_{OL_Tamper}	Output low voltage — high drive strength	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA				
	Output low voltage — low drive strength	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA				
I_{OL_Tamper}	Output low current total for Tamper pins	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	1
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	µA	1
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	1	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	0.025	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	0.25	µA	
I_{OZ_Tamper}	Hi-Z (off-state) leakage current (per Tamper pin)	—	0.25	µA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
R_{PU}	Internal pullup resistors (except Tamper pins)	20	50	kΩ	2
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	50	kΩ	3

1. Measured at VDD=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 → RUN	—	156	µs	
	• VLLS1 → RUN	—	156	µs	
	• VLLS2 → RUN	—	78	µs	
	• VLLS3 → RUN	—	78	µs	
	• LLS → RUN	—	4.8	µs	
	• VLPS → RUN	—	4.5	µs	
	• STOP → RUN	—	4.5	µs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	31.1	36.65	mA	
	• @ 3.0V	—	31	36.75	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	42.7	48.35	mA	
	• @ 3.0V					
	• @ 25°C	—	40	41.60	mA	
	• @ 105°C	—	48.33	51.50	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	17.9	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	6.9	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.0	—	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.7	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.678	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.49	1.24	mA	
	• @ 70°C	—	1.18	4.3	mA	
	• @ 105°C	—	3.0	12.5	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	57	139.31	µA	
	• @ 70°C	—	291	679.33	µA	
	• @ 105°C	—	927.3	1869.85	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	5.8	10.48	µA	
		—	26.7	47.99	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 70°C • @ 105°C	— —	114.9 —	196.49 —	µA µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 4.4 21 90.2	 5.54 36.46 150.17	 µA µA µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 2.1 6.84 29.4	 2.34 10.36 46.74	 µA µA µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 0.817 3.97 21.3	 0.86 5.77 33.99	 µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 0.52 3.67 21.20	 0.62 5.7 34.9	 µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ –40 to 25°C • @ 70°C • @ 105°C	 — — —	 0.339 3.36 20.3	 0.412 4.2 29.9	 µA µA µA	

I_{DD_VBAT}	Average current with RTC and 32 kHz disabled
	• @ 1.8 V
	  • @ –40 to 25°C
	  • @ 70°C
	  • @ 105°C
	• @ 3.0 V
	  • @ –40 to 25°C
	  • @ 70°C
	  • @ 105°C
		
		—
		—
		—
		
		—
		—
		—
			
			0.16
			0.55
			2.5
			
			0.18
			0.66
			2.92
				
				0.19
				0.72
				3.68
				
				0.21
				0.86
				4.30
					
					µA
					µA
					µA
					
					µA
					µA
					µA	

I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					10

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 1.8 V					
	• @ –40 to 25°C	—	0.59	0.70	µA	
	• @ 70°C	—	1.0	1.30	µA	
	• @ 105°C	—	3.0	4.42	µA	
	• @ 3.0 V					
	• @ –40 to 25°C	—	0.71	0.84	µA	
	• @ 70°C	—	1.22	1.59	µA	
	• @ 105°C	—	3.5	5.15	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, 30 Mhz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus clock, 30 MHz Flexbus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 256 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	VLLS3	440	490	540	560	570	580	nA
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

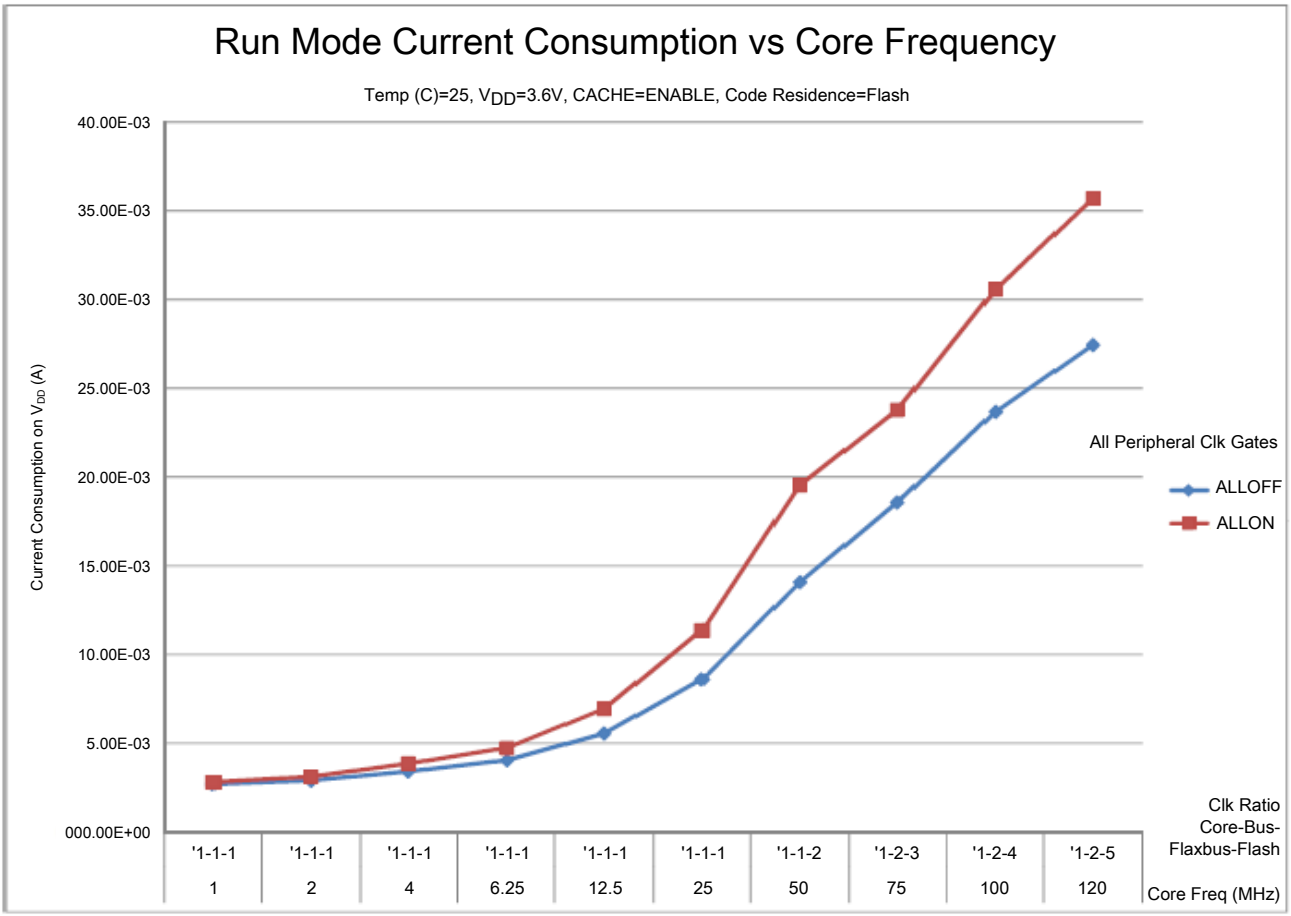


Figure 3. Run mode supply current vs. core frequency

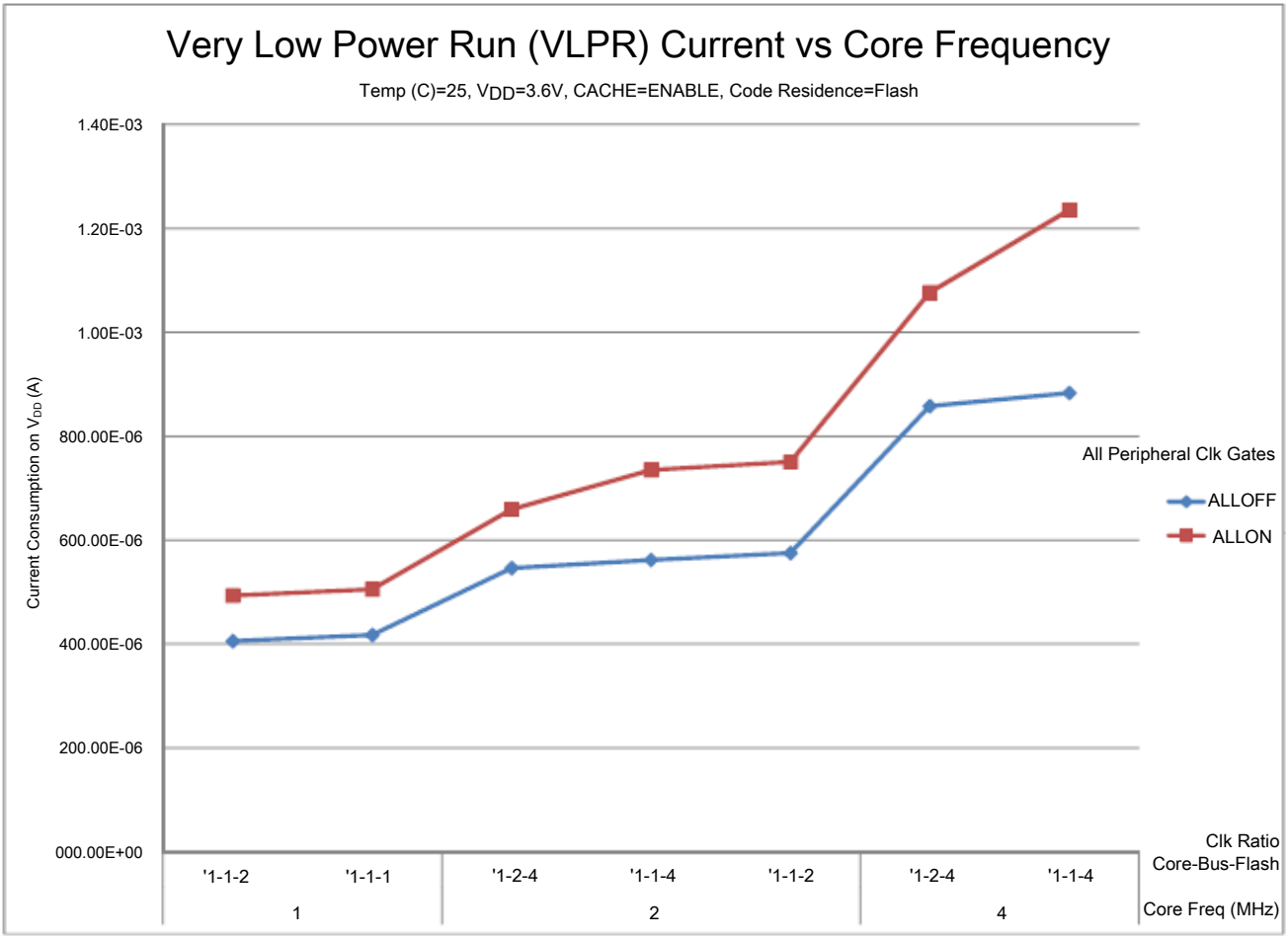


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
			144 LQFP		
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	16	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	22	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	21	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and*

Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 96 MHz, f_{BUS} = 48MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	0.8	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{FlexCAN\_ERCLK}$	FlexCAN external reference clock	—	8	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, IEEE 1588 timer, timers, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - 3 V				4
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	• Slew enabled				
		—	18	ns	

Table continues on the next page...

Table 11. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	—	12	ns	
	Port rise and fall time (high drive strength) - 5 V				4
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	6	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	4	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	24	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	14	ns	
	Port rise and fall time (low drive strength) - 3 V				5
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	24	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	16	ns	
	Port rise and fall time (low drive strength) - 5 V				5
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	17	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	10	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	20	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 25 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	51	38.1	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43	21.6	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	42	30.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	18	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	30	16.5	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	8.9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	2	0.9	°C/W	4

Table 13. Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
		outside center (natural convection)				

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 14. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1	—	ns

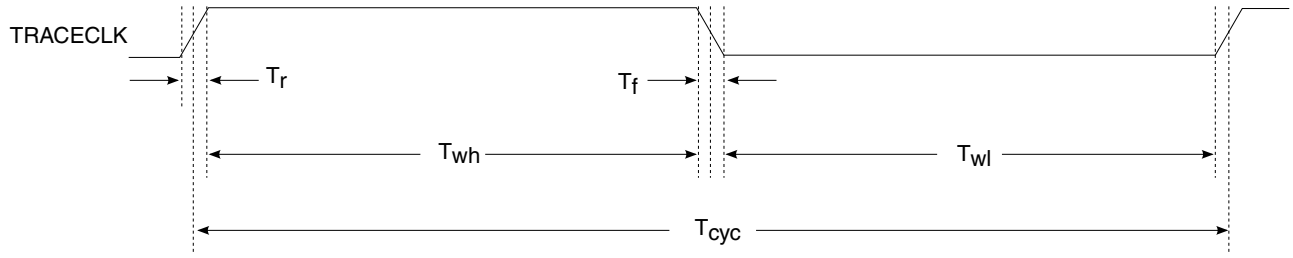


Figure 5. TRACE_CLKOUT specifications

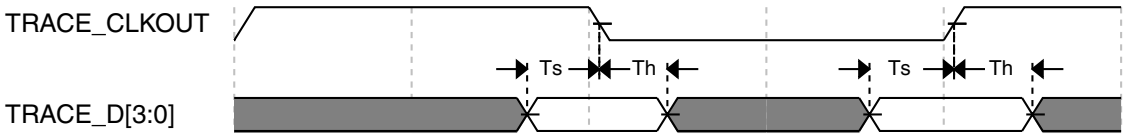


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 15. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 16. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.9	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

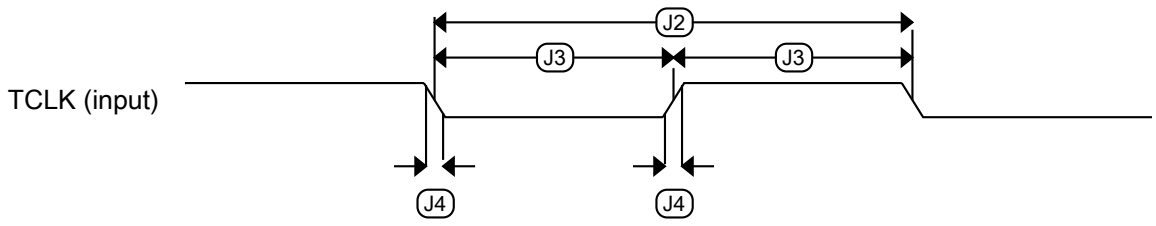


Figure 7. Test clock input timing

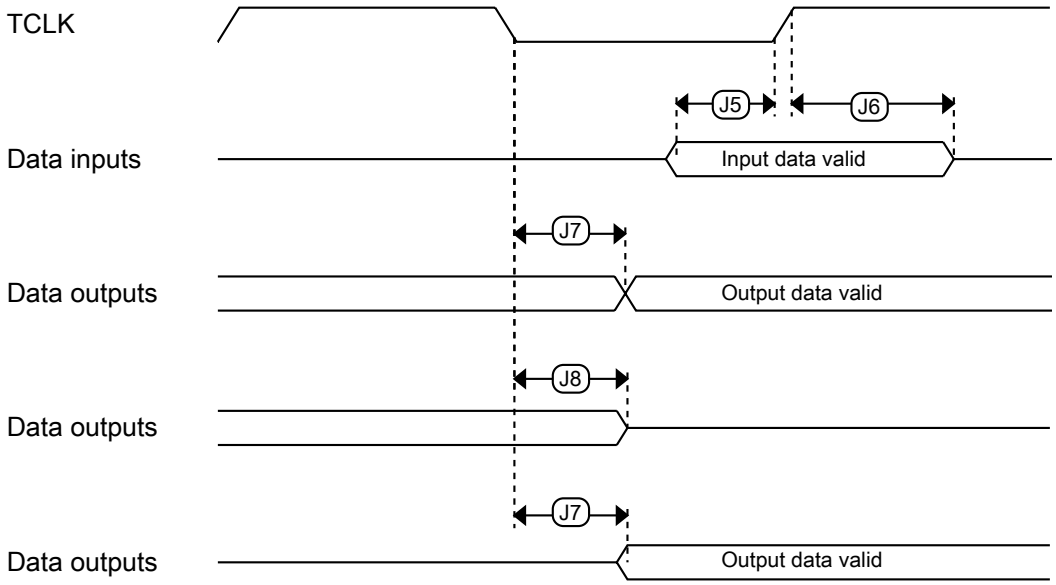


Figure 8. Boundary scan (JTAG) timing

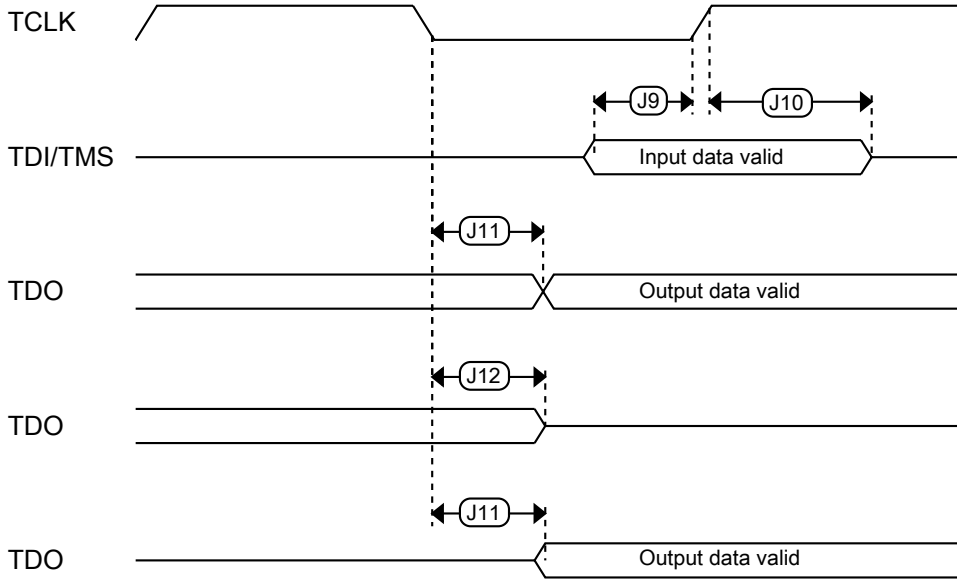


Figure 9. Test Access Port timing

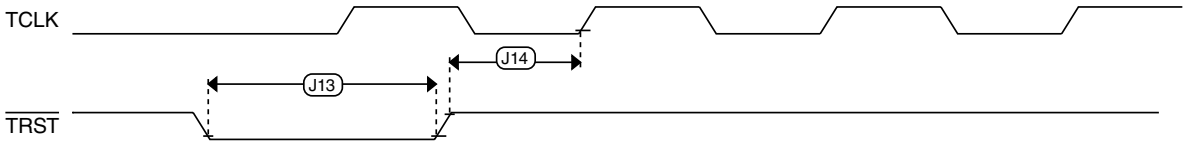


Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 17. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	µA	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current	—	25	—	µA	

Table continues on the next page...