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# Kinetis K64F Sub-Family Data Sheet

## 120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K64 product family members are optimized for cost-sensitive applications requiring low-power, USB/Ethernet connectivity, and up to 256 KB of embedded SRAM. These devices share the comprehensive enablement and scalability of the Kinetis family.

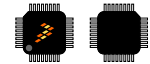
This product offers:

- Run power consumption down to 250  $\mu$ A/MHz. Static power consumption down to 5.8  $\mu$ A with full state retention and 5  $\mu$ s wakeup. Lowest Static mode down to 339 nA
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO Vreg, with USB device crystal-less operation
- 10/100 Mbit/s Ethernet MAC with MII and RMII interfaces

MK64FN1M0Vxx12  
MK64FX512Vxx12



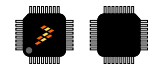
121 XFBGA  
8 x 8 x 0.5 mm Pitch  
0.65 mm



144 LQFP  
20 x 20 x 1.6 mm Pitch  
0.5 mm



144 MAPBGA  
13 x 13 x 1.46 mm  
Pitch 1 mm



100 QFP  
14 x 14 x 1.7 mm Pitch  
0.5 mm

### Performance

- Up to 120 MHz ARM® Cortex®-M4 core with DSP instructions and floating point unit

### Memories and memory interfaces

- Up to 1 MB program flash memory and 256 KB RAM
- Upto 128 KB FlexNVM and 4 KB FlexRAM on devices with FlexMemory
- FlexBus external bus interface

### System peripherals

- Multiple low-power modes, low-leakage wake-up unit
- Memory protection unit with multi-master protection
- 16-channel DMA controller
- External watchdog monitor and software watchdog

### Security and integrity modules

- Hardware CRC module
- Hardware random-number generator
- Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- 128-bit unique identification (ID) number per chip

### Analog modules

- Two 16-bit SAR ADCs
- Two 12-bit DACs
- Three analog comparators (CMP)
- Voltage reference

### Communication interfaces

- Ethernet controller with MII and RMII interface
- USB full-/low-speed On-the-Go controller
- Controller Area Network (CAN) module
- Three SPI modules
- Three I2C modules. Support for up to 1 Mbit/s
- Six UART modules
- Secure Digital Host Controller (SDHC)
- I2S module

### Timers

- Two 8-channel Flex-Timers (PWM/Motor control)
- Two 2-channel FlexTimers (PWM/Quad decoder)
- IEEE 1588 timers
- 32-bit PITs and 16-bit low-power timers
- Real-time clock
- Programmable delay block

### Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- PLL, FLL, and multiple internal oscillators
- 48 MHz Internal Reference Clock (IRC48M)

### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C



### Ordering Information<sup>1</sup>

Part Number	Memory		Maximum number of I/O's
	Flash	SRAM (KB)	
MK64FX512VLL12	512 KB	256	66
MK64FN1M0VLL12	1 MB	256	66
MK64FX512VDC12	512 KB	256	83
MK64FN1M0VDC12	1 MB	256	83
MK64FX512VLQ12	512 KB	256	100
MK64FN1M0VLQ12	1 MB	256	100
MK64FX512VMD12	512 KB	256	100
MK64FN1M0VMD12	1 MB	256	100

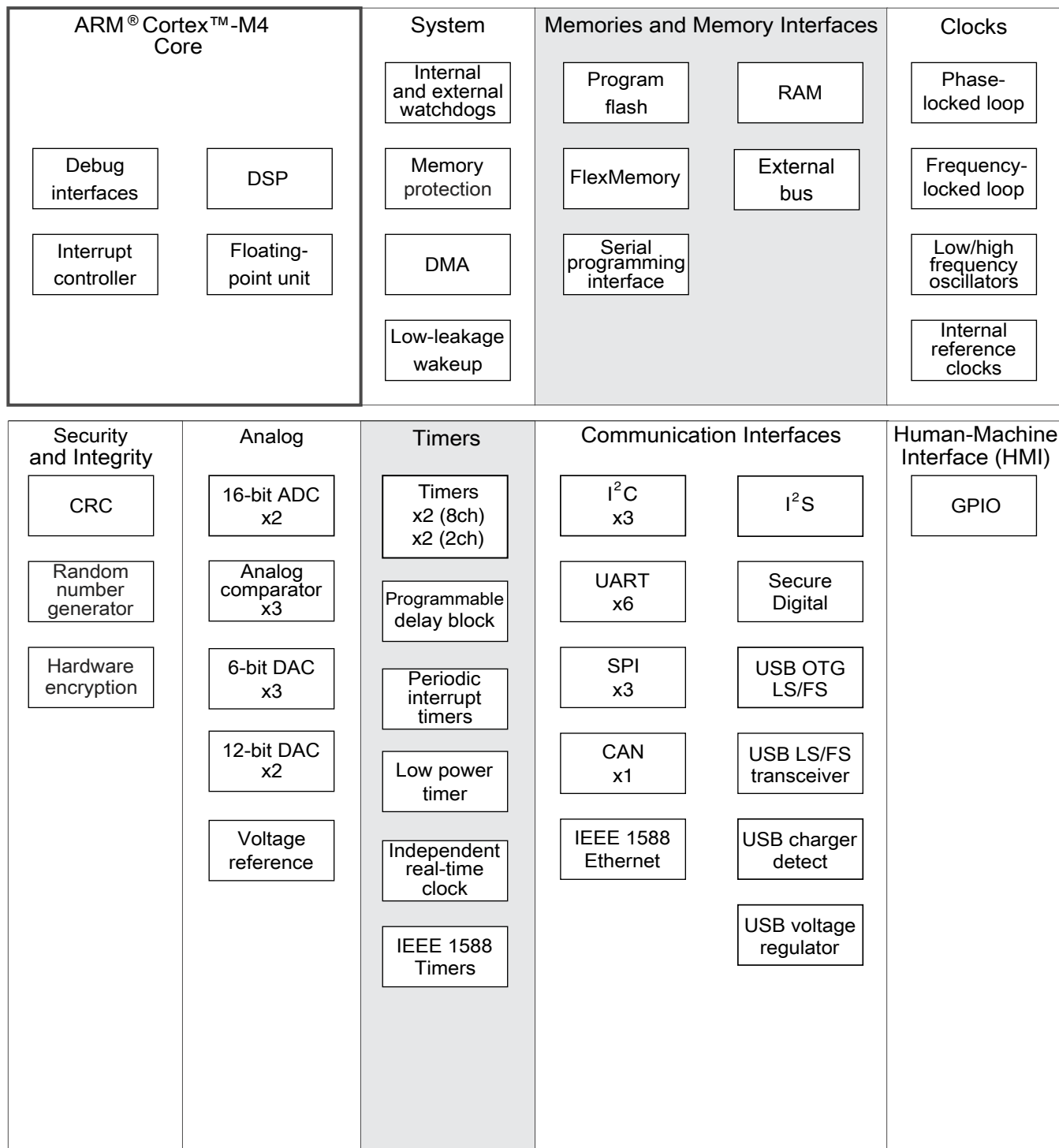
1. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.

### Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Solution Advisor</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K60PB <sup>1</sup>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K64P144M120SF5RM <sup>1</sup>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K64P144M120SF5 <sup>1</sup>
Package drawing	Package dimensions are provided in package drawings.	<ul style="list-style-type: none"> <li>• MAPBGA 144-pin: 98ASA00222D<sup>1</sup></li> <li>• LQFP 144-pin: 98ASS23177W<sup>1</sup></li> <li>• LQFP 100-pin: 98ASS23308W<sup>1</sup></li> <li>• XFBGA 121-pin: 98ASA00595D<sup>1</sup></li> </ul>

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.

## Kinetis K64 Family



**Figure 1. K64 block diagram**

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# 1 Ratings

## 1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

## General

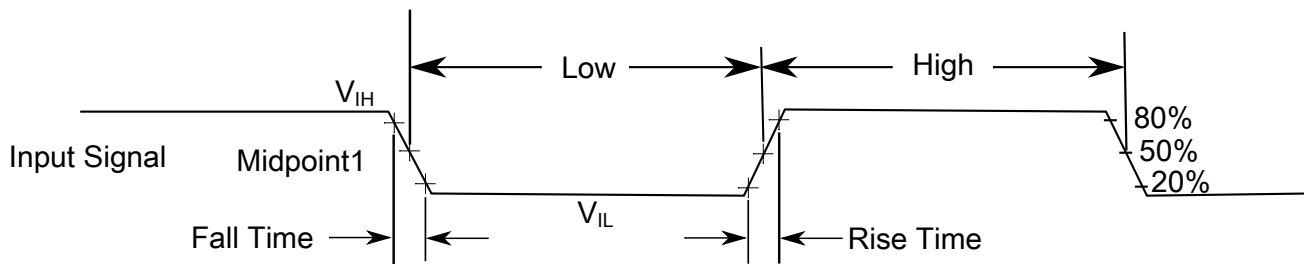
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	185	mA
$V_{DIO}$	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
$V_{DRTC\_WAKEUP}$	RTC Wakeup input voltage	-0.3	$V_{BAT} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB0\_DP}$	USB0_DP input voltage	-0.3	3.63	V
$V_{USB0\_DM}$	USB0_DM input voltage	-0.3	3.63	V
$V_{REGIN}$	USB regulator input	-0.3	6.0	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

### 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	3.6	V	
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> – V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	–0.1	0.1	V	
V <sub>SS</sub> – V <sub>SSA</sub>	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	–0.1	0.1	V	
V <sub>BAT</sub>	RTC battery supply voltage	1.71	3.6	V	
V <sub>IH</sub>	Input high voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub> 0.75 × V <sub>DD</sub>	— —	V V	
V <sub>IL</sub>	Input low voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	— —	0.35 × V <sub>DD</sub> 0.3 × V <sub>DD</sub>	V V	
V <sub>HYS</sub>	Input hysteresis	0.06 × V <sub>DD</sub>	—	V	
I <sub>CDIO</sub>	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V</li> </ul>	-5	—	mA	1
I <sub>CAIO</sub>	Analog <sup>2</sup> , EXTAL, and XTAL pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> <li>• V<sub>IN</sub> &gt; V<sub>DD</sub>+0.3V (Positive current injection)</li> </ul>	-5 —	— +5	mA	3
I <sub>Ccont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> <li>• Positive current injection</li> </ul>	-25 —	— +25	mA	
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	4
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	
V <sub>RFVBAT</sub>	V <sub>BAT</sub> voltage required to retain the VBAT register file	V <sub>POR_VBAT</sub>	—	V	

- All 5 V tolerant digital I/O pins are internally clamped to V<sub>SS</sub> through an ESD protection diode. There is no diode connection to V<sub>DD</sub>. If V<sub>IN</sub> is less than V<sub>DIO\_MIN</sub>, a current limiting resistor is required. If V<sub>IN</sub> greater than V<sub>DIO\_MIN</sub> (=V<sub>SS</sub>-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. The negative DC injection current limiting resistor is calculated as  $R=(V_{DIO\_MIN}-V_{IN})/|I_{CDIO}|$ .
- Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
- All analog pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>AIO\_MIN</sub> or greater than V<sub>AIO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{CAIO}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{CAIO}|$ . Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
- Open drain outputs must be pulled to V<sub>DD</sub>.



## 2.2.2 LVD and POR operating requirements

Table 2.  $V_{DD}$  supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
$V_{LVW1H}$	Low-voltage warning thresholds — high range					1
	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
$V_{LVW2H}$	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
$V_{LVW3H}$	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
$V_{LVW4H}$	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
$V_{LVW1L}$	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
$V_{LVW2L}$	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
$V_{LVW3L}$	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
$V_{LVW4L}$	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
$V_{BG}$	Bandgap voltage reference	0.97	1.00	1.03	V	
$t_{LPO}$	Internal low power oscillator period — factory trimmed	900	1000	1100	$\mu$ s	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR\_VBAT}$	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

## 2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — high drive strength				

Table continues on the next page...

**Table 4. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -8\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -2\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage — high drive strength	$V_{BAT} - 0.5$	—	V	
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$ , $I_{OH} = -10\text{ mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$ , $I_{OH} = -3\text{ mA}$	$V_{BAT} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$ , $I_{OH} = -2\text{ mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$ , $I_{OH} = -0.6\text{ mA}$	$V_{BAT} - 0.5$ $V_{BAT} - 0.5$	— —	V V	
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	100	mA	
$V_{OL}$	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 9\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 3\text{ mA}$	— —	0.5 0.5	V V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 2\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 0.6\text{ mA}$	— —	0.5 0.5	V V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage — high drive strength	—	0.5	V	
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$ , $I_{OL} = 10\text{ mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$ , $I_{OL} = 3\text{ mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$ , $I_{OL} = 2\text{ mA}$ • $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$ , $I_{OL} = 0.6\text{ mA}$	— —	0.5 0.5	V V	
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUP pins	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range	—	1	$\mu\text{A}$	1
$I_{IN}$	Input leakage current (per pin) at 25°C	—	0.025	$\mu\text{A}$	1
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) for full temperature range	—	1	$\mu\text{A}$	
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) at 25°C	—	0.025	$\mu\text{A}$	

Table continues on the next page...

**Table 4. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	0.25	μA	
I <sub>OZ_RTC_WAK EUP</sub>	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)	—	0.25	μA	
R <sub>PU</sub>	Internal pullup resistors (except RTC_WAKEUP pins)	20	50	kΩ	2
R <sub>PD</sub>	Internal pulldown resistors (except RTC_WAKEUP pins)	20	50	kΩ	3

1. Measured at V<sub>DD</sub>=3.6V
2. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>
3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>DD</sub>

## 2.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub>, and VLLS<sub>x</sub>→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
t <sub>POR</sub>	After a POR event, amount of time from the point V <sub>DD</sub> reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	
	• VLLS0 → RUN	—	156	μs	
	• VLLS1 → RUN	—	156	μs	
	• VLLS2 → RUN	—	78	μs	
	• VLLS3 → RUN	—	78	μs	
	• LLS → RUN	—	4.8	μs	
	• VLPS → RUN	—	4.5	μs	
	• STOP → RUN	—	4.5	μs	

## 2.2.5 Power consumption operating behaviors

### NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks disabled, code executing from flash	—	31.1	36.65	mA	2
		—	31	36.75	mA	
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks enabled, code executing from flash	—	42.7	48.35	mA	3, 4
		—	40	41.60	mA	
		—	48.33	51.50	mA	
I <sub>DD_WAIT</sub>	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	17.9	—	mA	2
I <sub>DD_WAIT</sub>	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	6.9	—	mA	5
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.0	—	mA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.7	—	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.678	—	mA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V	—	0.49	1.24	mA	
		—	1.18	4.3	mA	
		—	3.0	12.5	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V	—	57	139.31	μA	
		—	291	679.33	μA	
		—	927.3	1869.85	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V					9

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	5.8	10.48	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	4.4	5.54	μA	
		—	21	36.46	μA	
		—	90.2	150.17	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	2.1	2.34	μA	
		—	6.84	10.36	μA	
		—	29.4	46.74	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.817	0.86	μA	
		—	3.97	5.77	μA	
		—	21.3	33.99	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.52	0.62	μA	
		—	3.67	5.7	μA	
		—	21.20	34.9	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.339	0.412	μA	
		—	3.36	4.2	μA	
		—	20.3	29.9	μA	
I <sub>DD_VBAT</sub>	Average current with RTC and 32 kHz disabled <ul style="list-style-type: none"> <li>• @ 1.8 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul> </li> <li>• @ 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul> </li> </ul>	—	0.16	0.19	μA	
		—	0.55	0.72	μA	
		—	2.5	3.68	μA	
		—	0.18	0.21	μA	
		—	0.66	0.86	μA	
		—	2.92	4.30	μA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers					10
	• @ 1.8 V					
	• @ -40 to 25°C	—	0.59	0.70	μA	
	• @ 70°C	—	1.0	1.30	μA	
	• @ 105°C	—	3.0	4.42	μA	
	• @ 3.0 V					
	• @ -40 to 25°C	—	0.71	0.84	μA	
• @ 70°C	—	1.22	1.59	μA		
• @ 105°C	—	3.5	5.15	μA		

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
- 120 MHz core and system clock, 60 MHz bus clock, 30 MHz Flexbus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
- Max values are measured with CPU executing DSP instructions.
- 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz FlexBus and flash clock. MCG configured for FEI mode.
- 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- Data reflects devices with 256 KB of RAM.
- Includes 32kHz oscillator current and RTC operation.

**Table 7. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHZ</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHZ</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>EREFSTEN4MHZ</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I <sub>EREFSTEN32KHZ</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by							

Table continues on the next page...

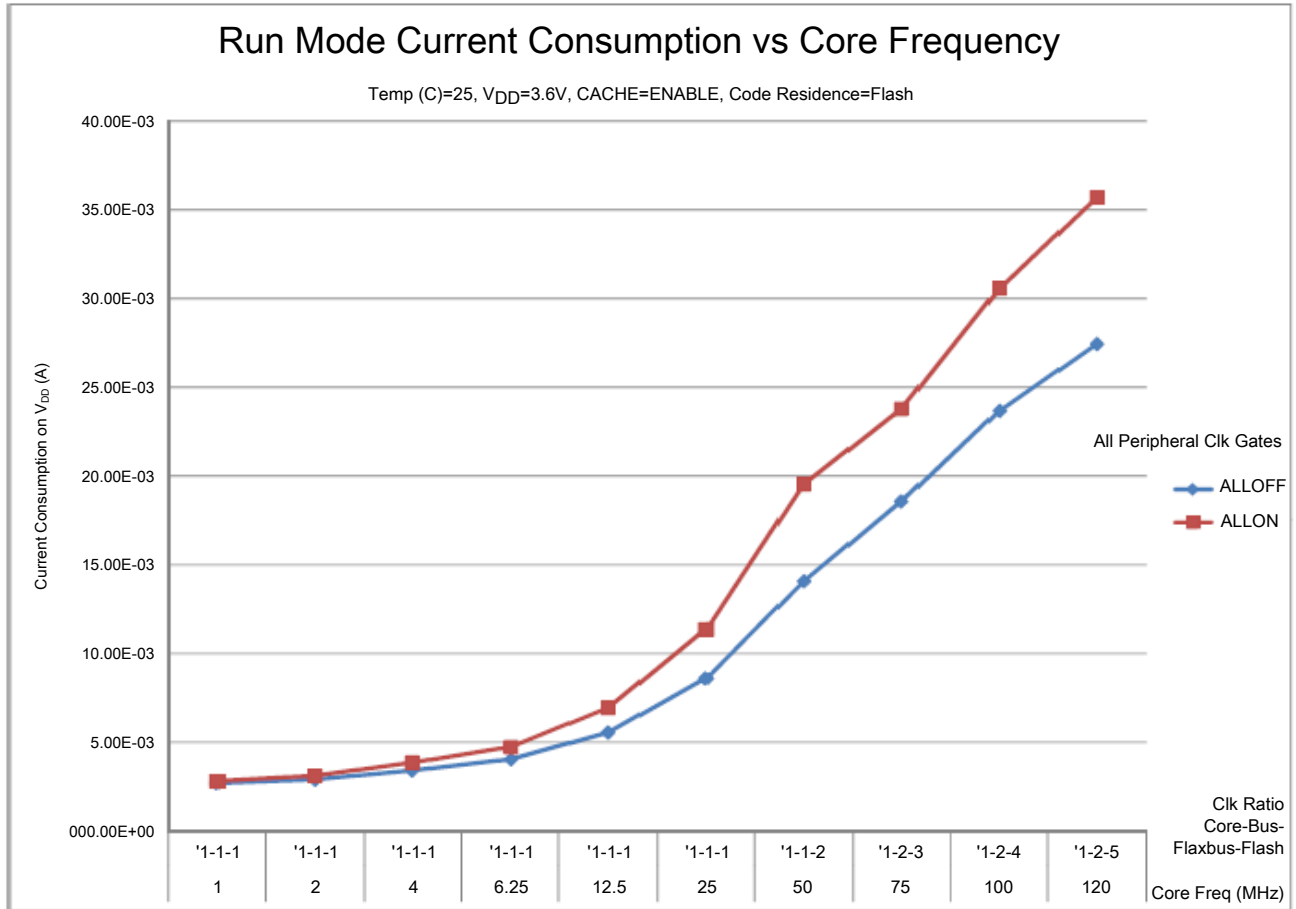
**Table 7. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	490	490	540	560	570	680	
	LLS	510	560	560	560	610	680	
	VLPS	510	560	560	560	610	680	
	STOP							
I <sub>48MIRC</sub>	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>RTC</sub>	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE



**Figure 3. Run mode supply current vs. core frequency**



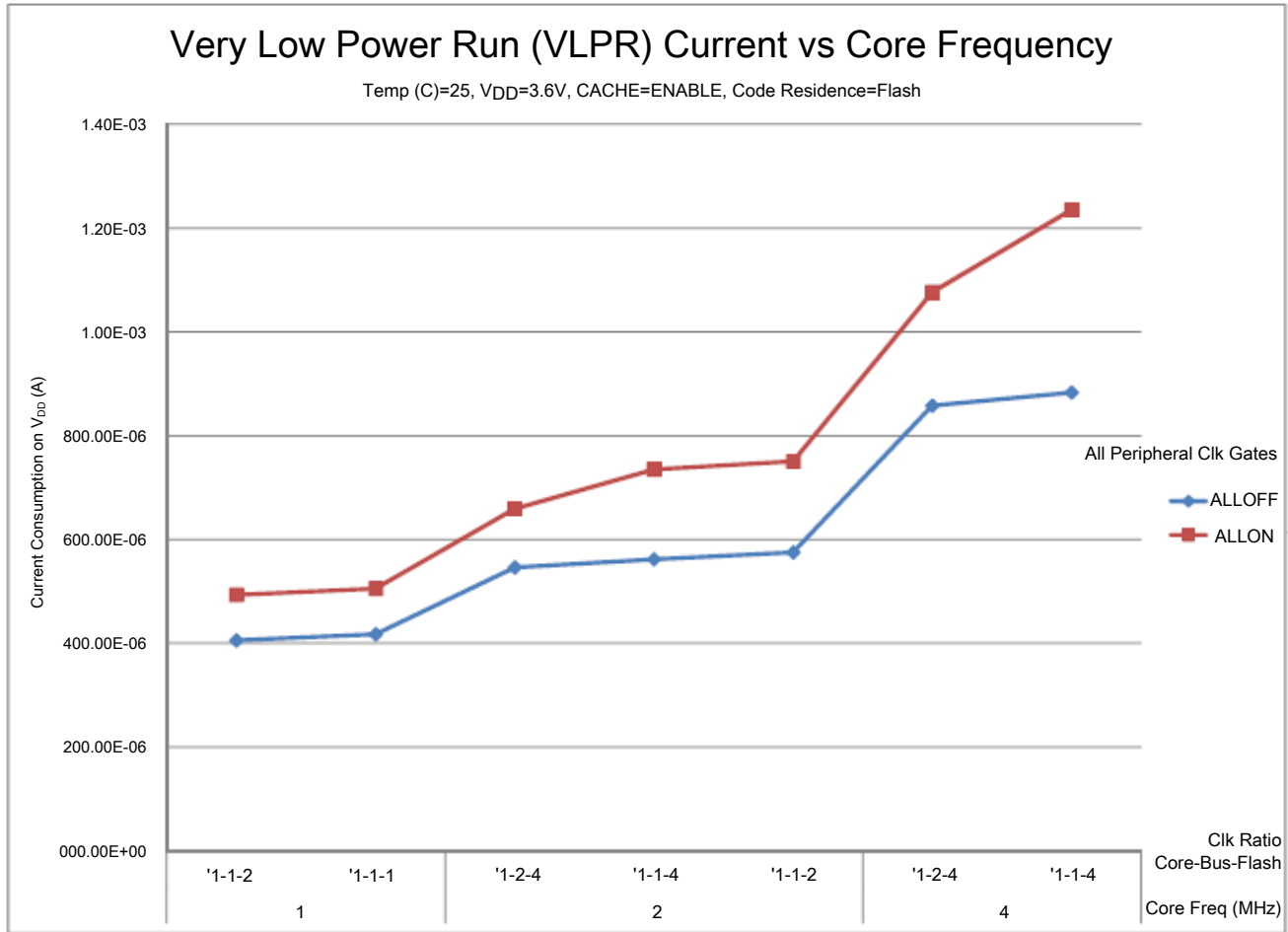


Figure 4. VLPR mode supply current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
			144 LQFP		
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	16	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	22	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	21	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	16	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and*

*Wideband TEM Cell Method.* Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ ,  $f_{OSC} = 12\text{ MHz}$  (crystal),  $f_{SYS} = 96\text{ MHz}$ ,  $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.nxp.com](http://www.nxp.com).
2. Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
$f_{ENET}$	System and core clock when ethernet in operation			MHz	
	• 10 Mbps	5	—		
	• 100 Mbps	50	—		
$f_{BUS}$	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	

Table continues on the next page...

**Table 10. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
f <sub>LPTMR</sub>	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	—	4	MHz	
f <sub>BUS</sub>	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f <sub>FLASH</sub>	Flash clock	—	0.8	MHz	
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	
f <sub>LPTMR_pin</sub>	LPTMR clock	—	25	MHz	
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	
f <sub>FlexCAN_ERCLK</sub>	FlexCAN external reference clock	—	8	MHz	
f <sub>I2S_MCLK</sub>	I2S master clock	—	12.5	MHz	
f <sub>I2S_BCLK</sub>	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, IEEE 1588 timer, timers, and I<sup>2</sup>C signals.

**Table 11. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ( $\overline{\text{EZP\_CS}}$ ) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - 3 V				4
	<ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled</li> </ul>	—	8	ns	
		—	6	ns	
		—	18	ns	

Table continues on the next page...

**Table 11. General switching specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul>	—	12	ns	
	Port rise and fall time (high drive strength) - 5 V <ul style="list-style-type: none"> <li>• Slew disabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	6	ns	4
		—	4	ns	
		—	24	ns	
		—	14	ns	
	Port rise and fall time (low drive strength) - 3 V <ul style="list-style-type: none"> <li>• Slew disabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	12	ns	5
		—	6	ns	
		—	24	ns	
		—	16	ns	
	Port rise and fall time (low drive strength) - 5 V <ul style="list-style-type: none"> <li>• Slew disabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled               <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	17	ns	5
		—	10	ns	
		—	36	ns	
		—	20	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 25 pF load
5. 15 pF load

## 2.4 Thermal specifications

## 2.4.1 Thermal operating requirements

**Table 12. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
T <sub>J</sub>	Die junction temperature	-40	125	°C
T <sub>A</sub>	Ambient temperature <sup>1</sup>	-40	105	°C

1. Maximum T<sub>A</sub> can be exceeded only if the user ensures that T<sub>J</sub> does not exceed maximum T<sub>J</sub>. The simplest method to determine T<sub>J</sub> is:

$$T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$$

## 2.4.2 Thermal attributes

**Table 13. Thermal attributes**

Board type	Symbol	Description	144 LQFP	144 MAPBGA	121 XFBGA	100 LQFP	Unit	Notes
Single-layer (1s)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	51	38.1	33.3	51	°C/W	1
Four-layer (2s2p)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	43	21.6	21.1	39	°C/W	1
Single-layer (1s)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	30.8	26.2	41	°C/W	1
Four-layer (2s2p)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	18	17.8	32	°C/W	1
—	R <sub>θJB</sub>	Thermal resistance, junction to board	30	16.5	16.3	24	°C/W	2
—	R <sub>θJC</sub>	Thermal resistance,	11	8.9	12	11	°C/W	3

Table continues on the next page...

**Table 13. Thermal attributes (continued)**

Board type	Symbol	Description	144 LQFP	144 MAPBGA	121 XFBGA	100 LQFP	Unit	Notes
		junction to case						
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	0.9	0.2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

#### 3.1.1 Debug trace timing specifications

**Table 14. Debug trace operating behaviors**

Symbol	Description	Min.	Max.	Unit
$T_{cyc}$	Clock period	Frequency dependent		MHz
$T_{wl}$	Low pulse width	2	—	ns
$T_{wh}$	High pulse width	2	—	ns
$T_r$	Clock and data rise time	—	3	ns
$T_f$	Clock and data fall time	—	3	ns
$T_s$	Data setup	1.5	—	ns
$T_h$	Data hold	1	—	ns

## Peripheral operating requirements and behaviors

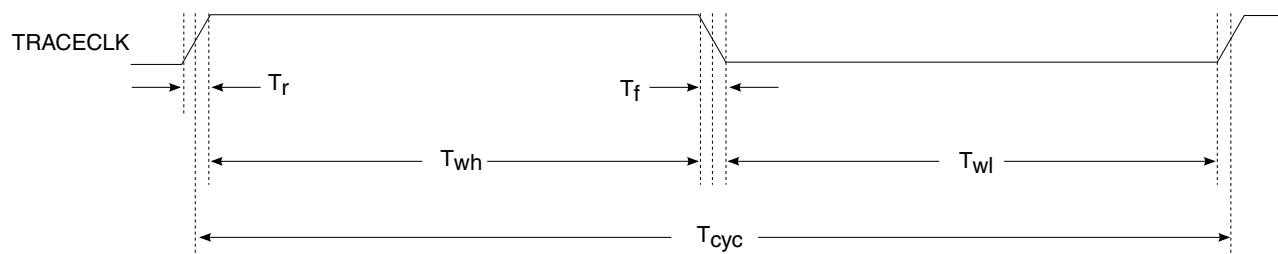


Figure 5. TRACE\_CLKOUT specifications

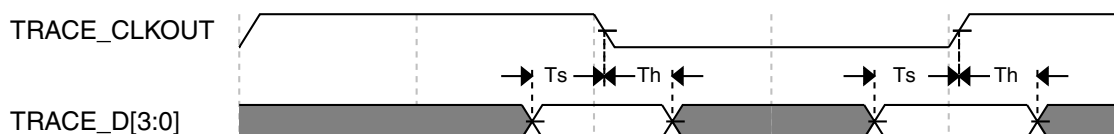


Figure 6. Trace data specifications

### 3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	0	10	MHz
		0	25	
		0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	50	—	ns
		20	—	ns
		10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

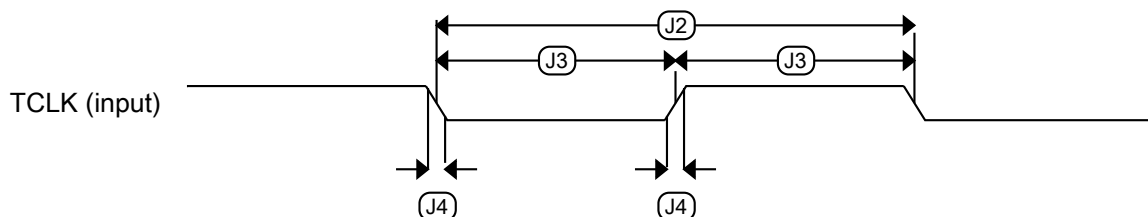
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**Table 15. JTAG limited voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

**Table 16. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.9	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

**Figure 7. Test clock input timing**



Peripheral operating requirements and behaviors

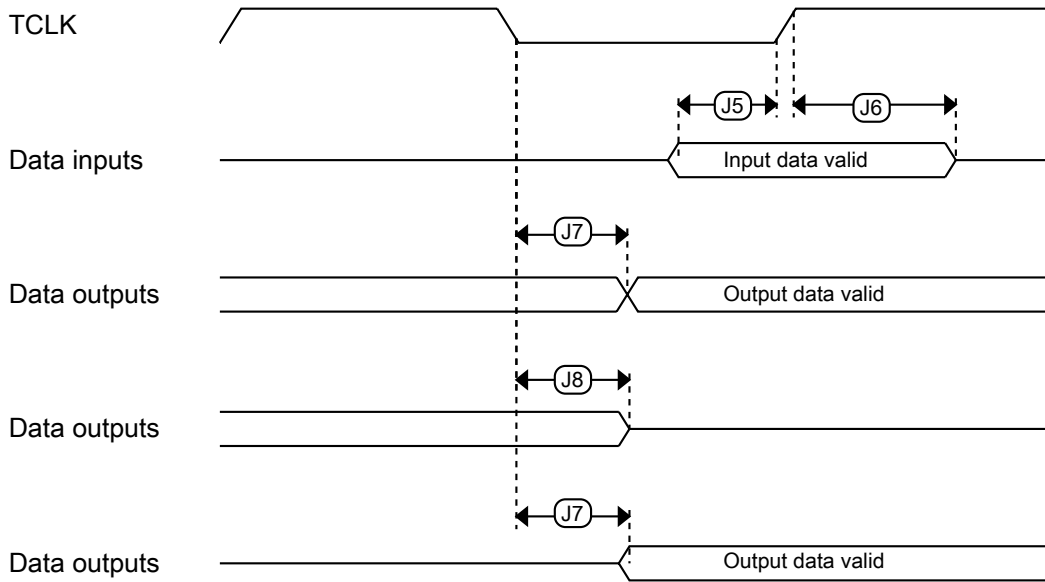


Figure 8. Boundary scan (JTAG) timing

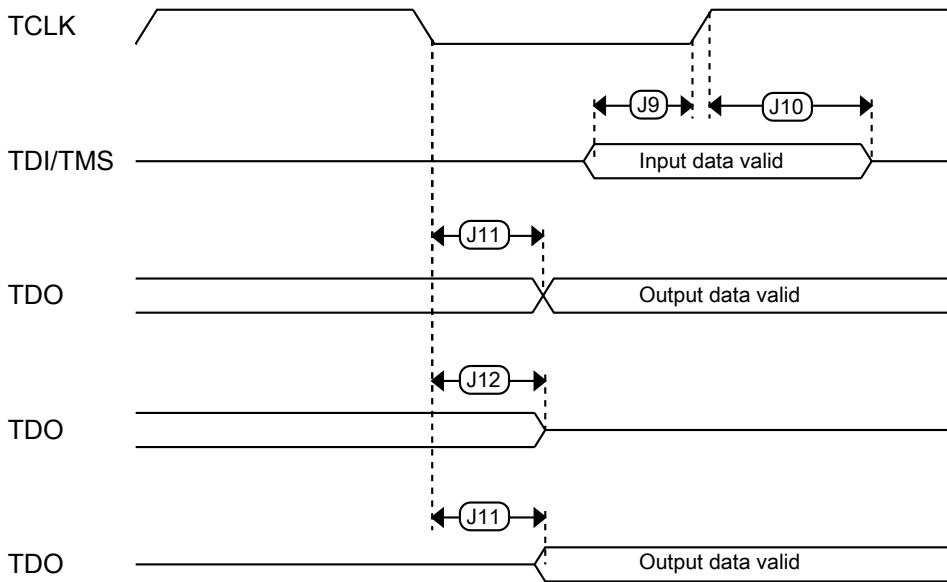


Figure 9. Test Access Port timing

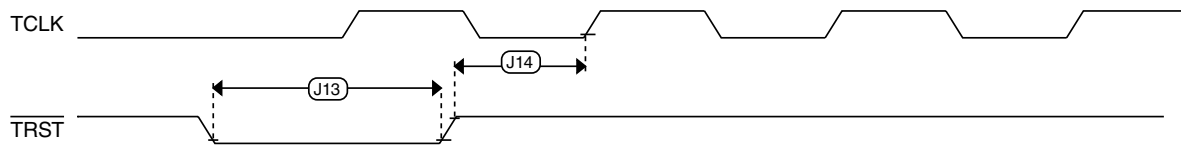


Figure 10. TRST timing

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

Table 17. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints\_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints\_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$I_{\text{ints}}$	Internal reference (slow clock) current	—	20	—	μA	
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{\text{dco}}$	1
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% $f_{\text{dco}}$	1
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	% $f_{\text{dco}}$	1, 2
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1	% $f_{\text{dco}}$	1
$f_{\text{intf\_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf\_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$I_{\text{intf}}$	Internal reference (fast clock) current	—	25	—	μA	

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