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Kinetis K66 Sub-Family

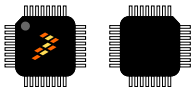
180 MHz ARM® Cortex®-M4F Microcontroller.

MK66FN2M0VMD18
MK66FX1M0VMD18
MK66FN2M0VLQ18
MK66FX1M0VLQ18

The K66 sub-family members provide greater performance, memory options up to 2 MB total flash and 256 KB of SRAM, as well as higher peripheral integration with features such as Dual USB and a 10/100 Mbit/s Ethernet MAC. These devices maintain hardware and software compatibility with the existing Kinetis family. This product also offers:

- Integration of a High Speed USB Physical Transceiver
- Greater performance flexibility with a High Speed Run mode
- Smarter peripherals with operation in Stop modes

144 MAPBGA (MD)
13 mm x 13 mm Pitch 1 mm



144 LQFP (LQ)
20 mm x 20 mm Pitch 0.5 mm

Performance

- Up to 180 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit

System and Clocks

- Multiple low-power modes to provide power optimization based on application requirements
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference

Security

- Hardware random-number generator
- Supports DES, AES, SHA accelerator (CAU)
- Multiple levels of embedded flash security

Timers

- Four Periodic interrupt timers
- 16-bit low-power timer
- Two 16-bit low-power timer PWM modules
- Two 8-channel motor control/general purpose/PWM timers
- Two 2-ch quad decoder/general purpose timers
- Real-time clock

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- General-purpose input/output

Memories and memory expansion

- Up to 2 MB program flash memory on non-FlexMemory devices with 256 KB RAM
- Up to 1 MB program flash memory and 256 KB of FlexNVM on FlexMemory devices
- 4 KB FlexRAM on FlexMemory devices
- FlexBus external bus interface and SDRAM controller

Analog modules

- Two 16-bit SAR ADCs and two 12-bit DAC
- Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Voltage reference 1.2V

Communication interfaces

- Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
- USB high-/full-/low-speed On-the-Go with on-chip high speed transceiver
- USB full-/low-speed OTG with on-chip transceiver
- Two CAN, three SPI and four I2C modules
- Low Power Universal Asynchronous Receiver/ Transmitter 0 (LPUART0) and five standard UARTs
- Secure Digital Host Controller (SDHC)
- I2S module

Operating Characteristics

- Voltage/Flash write voltage range:1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM	
MK66FN2M0VMD18	2 MB	256 KB	100
MK66FX1M0VMD18	1.25 MB	256 KB	100
MK66FN2M0VLQ18	2 MB	256 KB	100
MK66FX1M0VLQ18	1.25 MB	256 KB	100

1. To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K66P144M180SF5RMV2[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_0N65N [1]
Package drawing	Package dimensions are provided in package drawings.	• MAPBGA 144-pin : 98ASA00222D[1] • LQFP 144-pin: 98ASS23177W[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

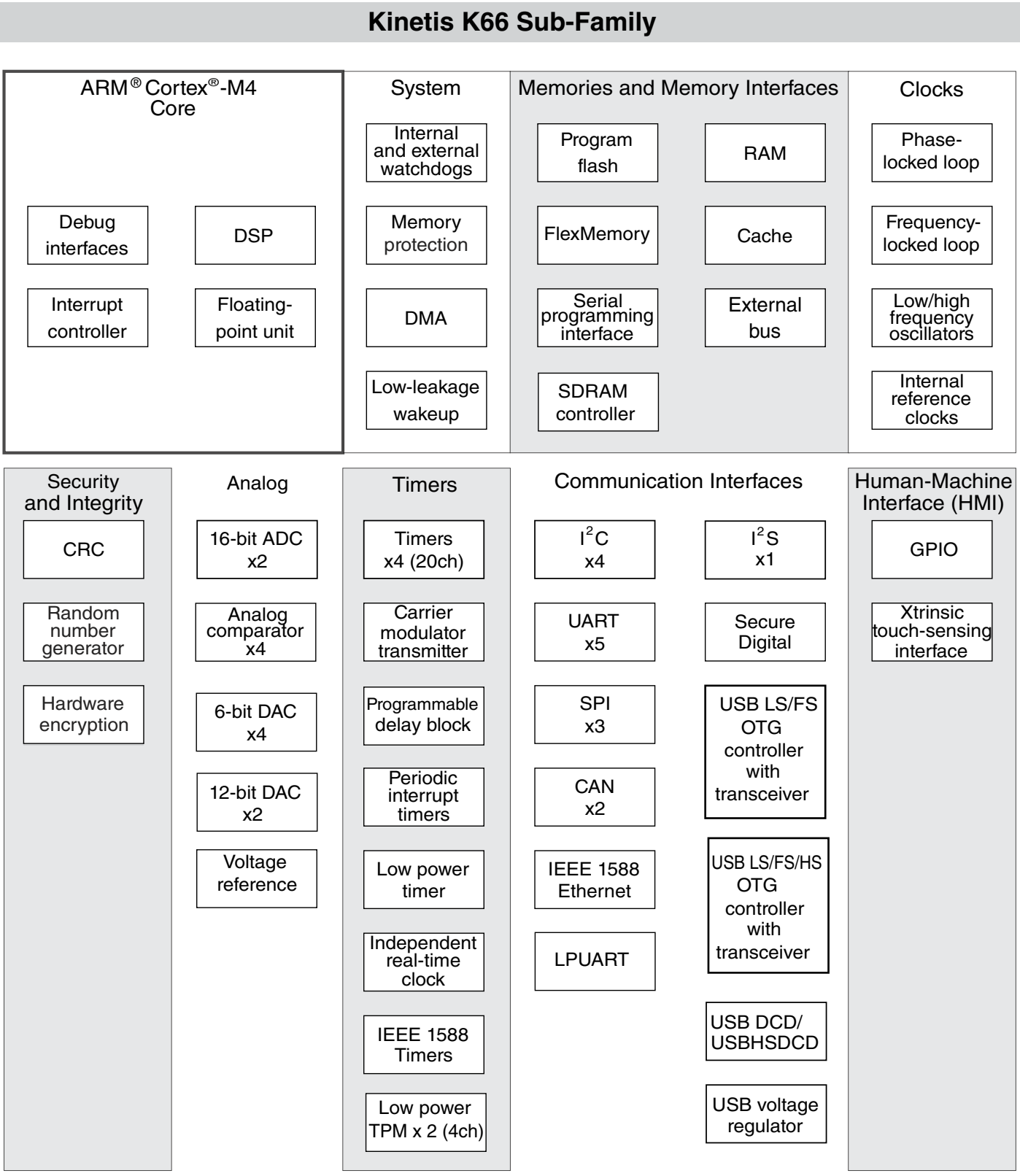


Figure 1. K66 Block Diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

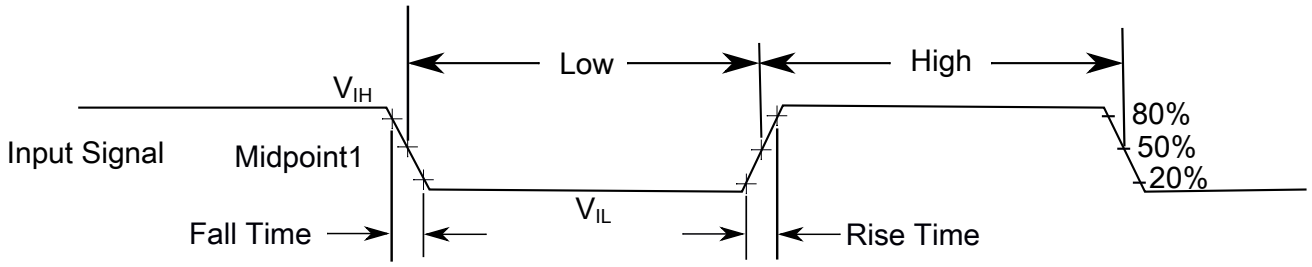
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital[1] input voltage,including RESET_b	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1] input voltage, including EXTAL32 and XTAL32	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB1_DP}	USB1_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{USB1_DM}	USB1_DM input voltage	–0.3	3.63	V
V_{USB1_VBUS}	USB1_VBUS detect voltage	–0.3	6.0	V
VREG_IN0, VREG_IN1	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Digital pins have a general purpose I/O port assigned (e.g. PTA0). Analog pins do not have an associated general purpose I/O port.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

- have C_L=30pF loads,
- are slew rate disabled, and
- are normal drive strength

2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital[1] input pin negative DC injection current (except RTC_WAKEUP pins) — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	2
I_{ICAIO}	Analog[1] input pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection)	 -5	 —	 mA	2
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pin • Negative current injection	-25	—	mA	
V_{ODPU}	Pseudo Open drain pullup voltage level	V_{DD}	V_{DD}	V	3
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. Digital pins have a general purpose I/O port assigned (e.g. PTA0). Analog pins do not have an associated general purpose I/O port.
2. All digital and analog I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} is less than VSS-0.3V, a current limiting resistor is required. The minimum negative DC injection current limiting resistor value is calculated as $R=(-0.3-V_{IN})/|I_{ICDIO}|$ or $R=(-0.3-V_{IN})/|I_{ICAIO}|$. The actual resistor should be an order of magnitude higher to tolerate transient voltages.
3. Open drain outputs must be pulled to VDD.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤V_{DD} ≤ 2.7 V, I_{OH} = -5mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 — —	 V V	
	Output high voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage— normal drive pad • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5 mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —		V V	
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	—	100	mA	
V_{OL}	Output low voltage — normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	— —	— —	0.5 0.5	V V	
	Output low voltage — high drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	— —	— —	0.5 0.5	V V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage— normal drive pad • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 2.5mA	— —		0.5 0.5	V V	
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUPpins	—	—	100	mA	
I_{IN}	Input leakage current, analog and digital pins • V_{SS} ≤ V_{IN} ≤ V_{DD}	—	0.002	0.5	µA	1
$I_{OZ\_RTC\_WAKEUP}$	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)	—	—	0.25	µA	
R_{PU}	Internal pullup resistors	20	—	50	kΩ	2
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	3

1. Measured at VDD=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100MHz
- Bus clock = 50MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 –> RUN	—	172	µs	
	• VLLS1 –> RUN	—	172	µs	
	• VLLS2 –> RUN	—	94	µs	
	• VLLS3 –> RUN	—	94	µs	
	• LLS2 –> RUN	—	5.8	µs	
	• LLS3 –> RUN	—	5.8	µs	
	• VLPS –> RUN	—	5.4	µs	
	• STOP –> RUN	—	5.4	µs	

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	440	490	540	560	570	580	
	LLS2	490	490	540	560	570	680	
	LLS3	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{48MIRC}	48MHz IRC	511	520	545	556	563	576	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma)

Table 7. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	32.3	71.03	mA	
	• @ 3.0V	—	32.4	71.81	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	50.5	89.58	mA	
	• @ 3.0V					
	• @ 25°C	—	50.6	55.95	mA	
	• @ 105°C	—	69.7	99.85	mA	
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash	—	28.5	67.74	mA	5
	• at 3.0 V					
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash					6
	• @ 1.8V	—	47.2	91.25	mA	
	• @ 3.0V	—	47.3	91.62	mA	
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash					7, 4
	• @ 1.8V	—	71.4	103.58	mA	
	• @ 3.0V					
	• @ 25°C	—	71.5	79.13	mA	
	• @ 105°C	—	93.3	115.08	mA	
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 168 MHz core/ 28 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0V	—	42.9	91.97	mA	5
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	16.9	45.2	mA	8

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks enabled	—	35	62.81	mA	8
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.1	9.56	mA	9
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	2	9.88	mA	10
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 1 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock • at 3.0 V	—	986	9.47	µA	11
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.690	9.25	mA	12
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks enabled	—	1.5	10.00	mA	
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.791	2.39	mA	
	• @ 70°C	—	3.8	6.91	mA	
	• @ 105°C	—	13.2	18.91	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	202	353.77	µA	
	• @ 70°C	—	1400	2464.54	µA	
	• @ 105°C	—	5100	8949.06	µA	
I_{DD_LLS3}	Low leakage stop mode current at 3.0 V					
	• @ –40 to 25°C	—	9.0	16.5	µA	
	• @ 70°C	—	76.3	88.63	µA	
	• @ 105°C	—	402	656.08	µA	
I_{DD_LLS2}	Low leakage stop mode current at 3.0 V					
	• @ –40 to 25°C	—	5.7	9.7	µA	
	• @ 70°C	—	41.3	55.80	µA	
	• @ 105°C	—	229	276.81	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	5.5	7.31	µA	
	• @ 70°C	—	46.3	58.33	µA	
	• @ 105°C	—	249	380.77	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.7	3.24	µA	
	• @ 70°C	—	13.1	18.72	µA	
	• @ 105°C	—	76.6	84.77	µA	

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	0.847	1.48	µA	
	• @ 70°C	—	6.5	11.31	µA	
	• @ 105°C	—	46.7	81.78	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	0.551	.65	µA	
	• @ 70°C	—	6.3	7.12	µA	
	• @ 105°C	—	49.6	53.68	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.254	0.445	µA	
	• @ 70°C	—	6.3	10.99	µA	
	• @ 105°C	—	48.7	85.27	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	µA	
	• @ 70°C	—	0.49	0.64	µA	
	• @ 105°C	—	2.2	3.2	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					13
	• @ 1.8V					
	– @ –40 to 25°C	—	0.68	0.8	µA	
	– @ 70°C	—	1.2	1.56	µA	
	– @ 105°C	—	3.6	5.3	µA	
	• @ 3.0V					
	– @ –40 to 25°C	—	0.81	0.96	µA	
	– @ 70°C	—	1.45	1.89	µA	
	– @ 105°C	—	4.3	6.33	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. MCG configured for PEE mode.
6. 168 MHz core and system clock, 56 MHz bus and FlexBus clock, and 28 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
7. 168 MHz core and system clock, 56 MHz bus and FlexBus clock, and 28 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.

8. 120 MHz core and system clock, 60MHz bus clock, and FlexBus. MCG configured for PEE mode.
9. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
10. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
11. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
12. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
13. Includes 32kHz oscillator current and RTC operation.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

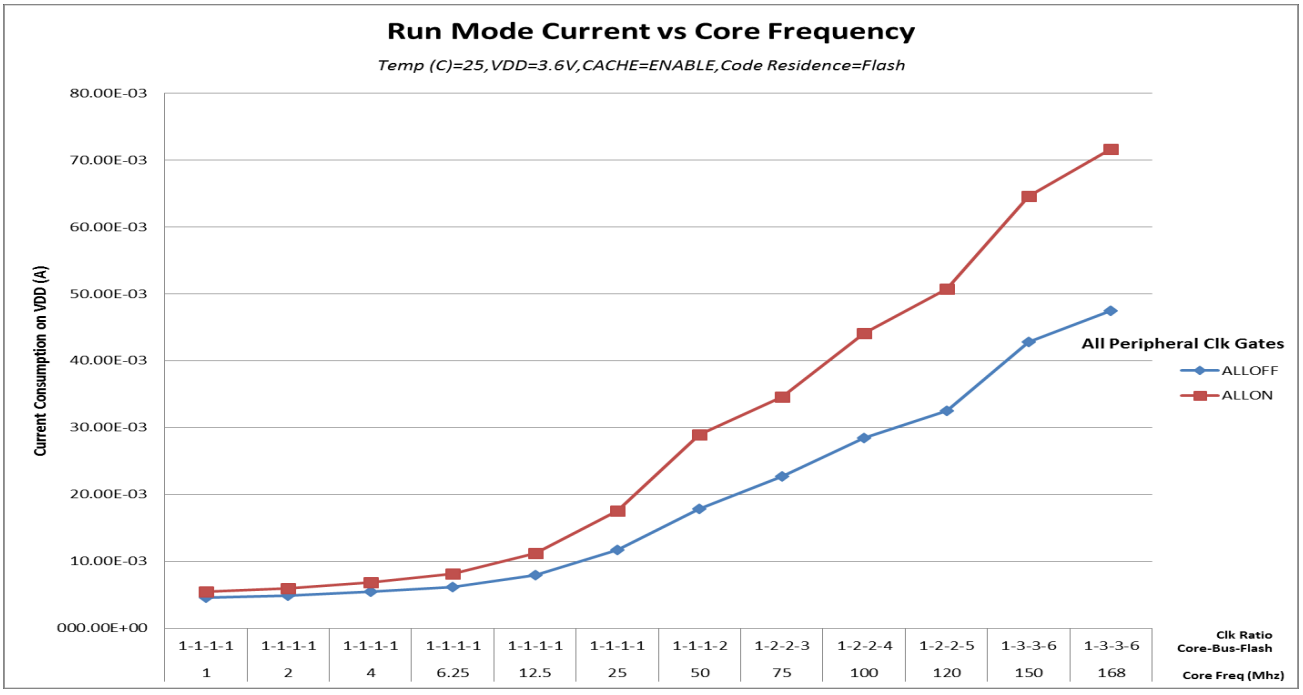


Figure 3. Run mode supply current vs. core frequency

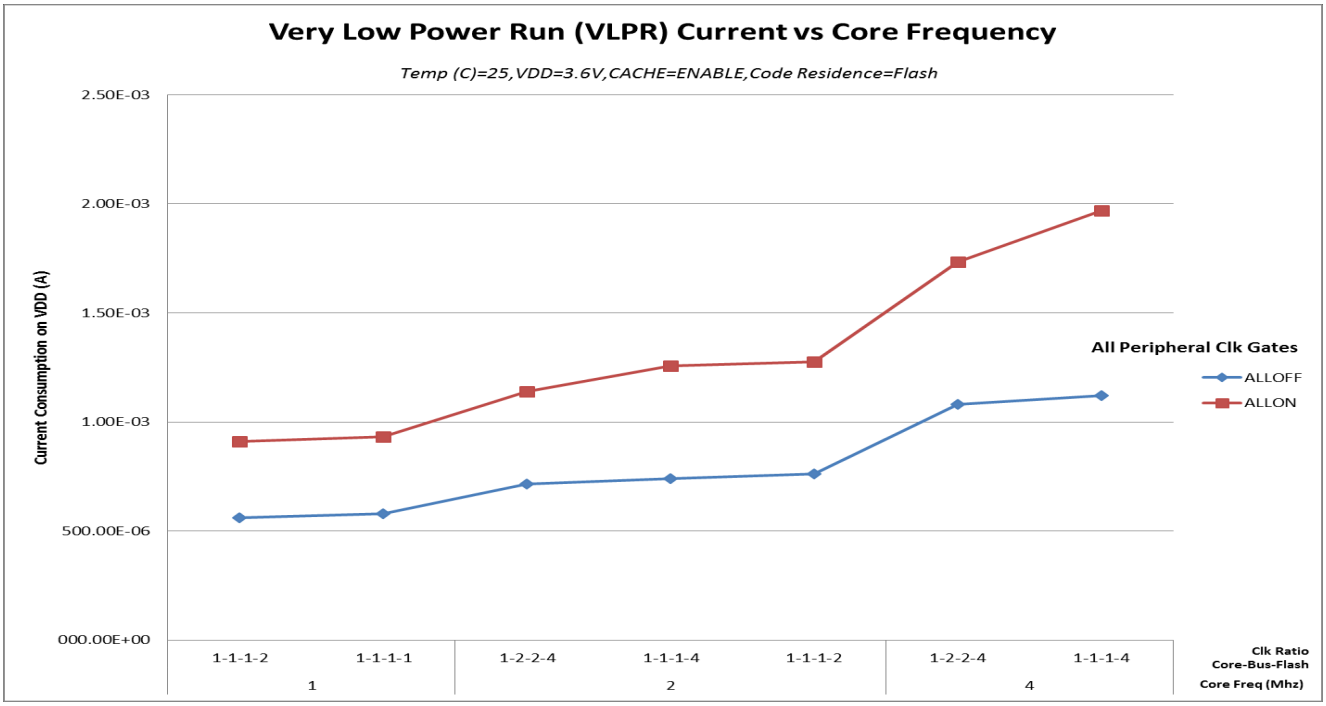


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	23	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	27	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	28	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	14	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = MHz, f_{BUS} = MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to nxp.com
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	180	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{SYS_USBHS}	System and core clock when High Speed USB in operation	100	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{BUS}	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	60	MHz	
f_{FLASH}	Flash clock	—	28	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
$f_{FlexCAN\_ERCLK}$	FlexCAN external reference clock	—	8	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, IEEE 1588 timer, timers, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) • Slew enabled	 —	 25	 ns	4
		—	15	ns	

Table continues on the next page...

Table 11. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	— —	7 7	ns ns	
	Port rise and fall time (low drive strength) • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	 — — — —	 25 15 7 7	 ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ x chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 13. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

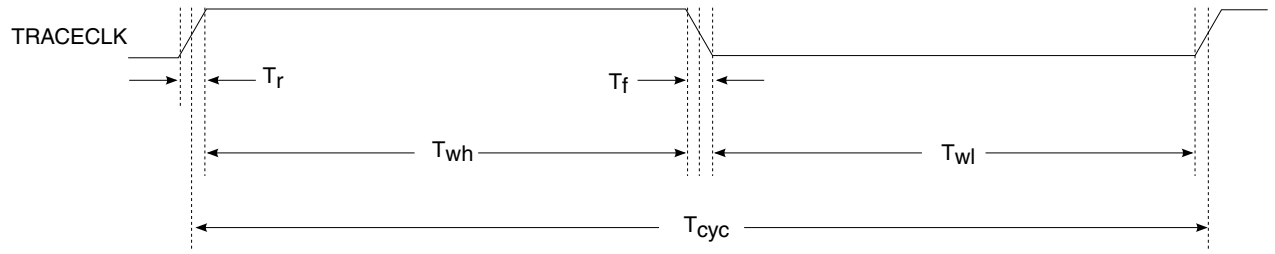


Figure 5. TRACE_CLKOUT specifications

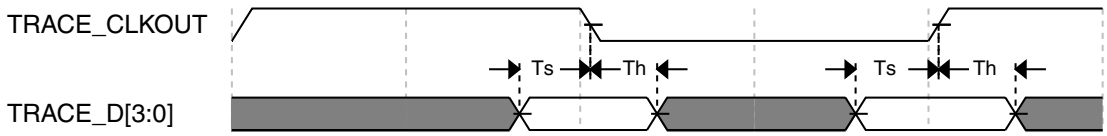


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns

Table continues on the next page...

Table 15. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

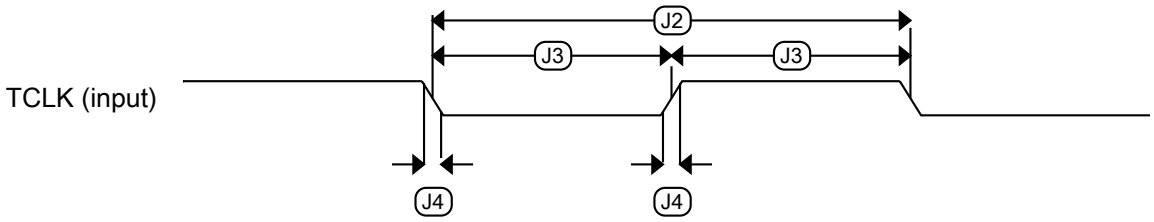


Figure 7. Test clock input timing

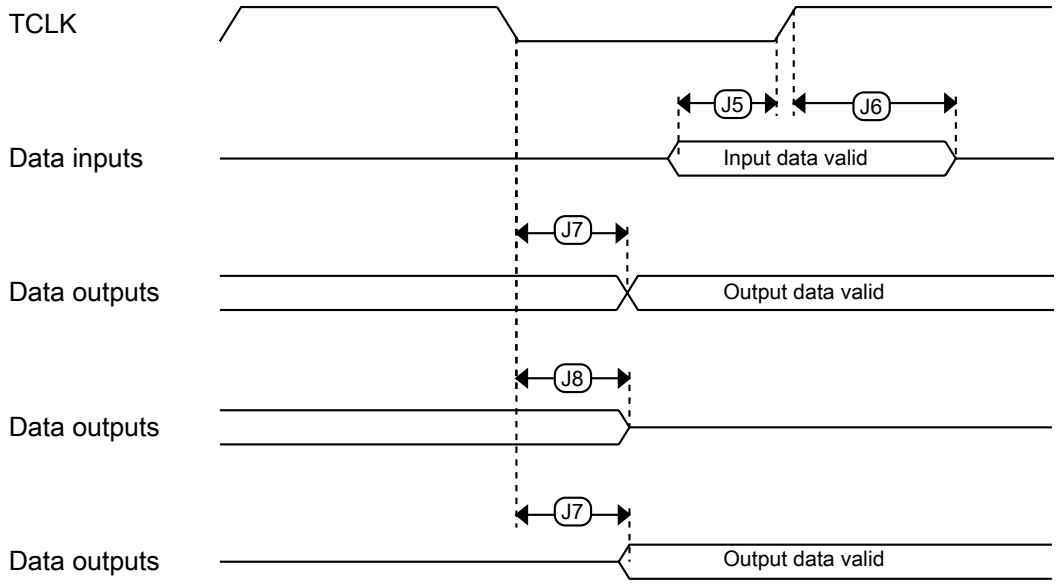


Figure 8. Boundary scan (JTAG) timing

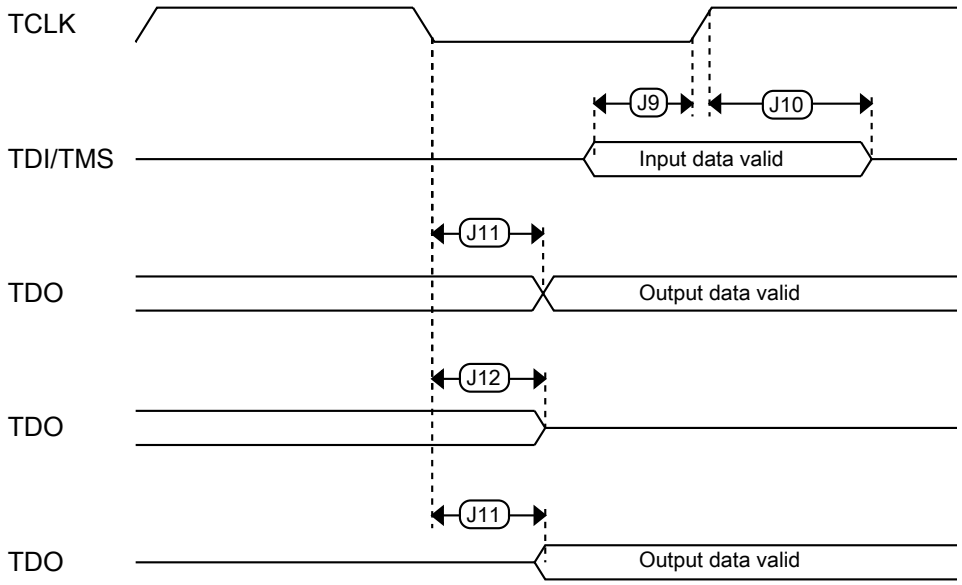


Figure 9. Test Access Port timing

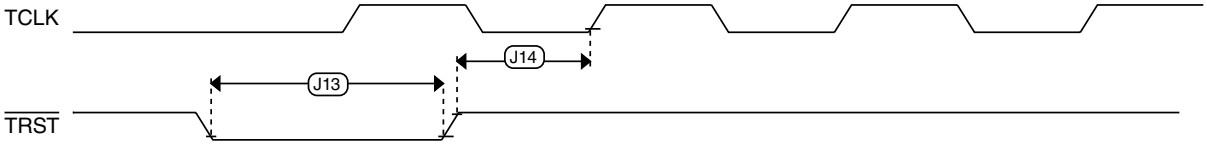


Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 16. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current		—	20	—	µA	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 0.5	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	1.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current		—	25	—	µA	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above (3/5)f_{int} never reset ext clk freq: between (2/5)fint and (3/5)f_{int} maybe reset (phase dependency) ext clk freq: below (2/5)f_{int} always reset		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11 ext clk freq: above (16/5)f_{int} never reset ext clk freq: between (15/5)f_{int} and (16/5)f_{int} maybe reset (phase dependency) ext clk freq: below (15/5)f_{int} always reset		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco_ut}	DCO output frequency range — untrimmed	Low range (DRS=00, DMX32=0) 640 × f_{ints_ut}	16.0	23.04	26.66	MHz	2
		Mid range (DRS=01, DMX32=0) 1280 × f_{ints_ut}	32.0	46.08	53.32		

Table continues on the next page...