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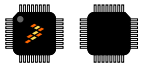
Kinetis K82 Sub-Family

High performance ARM® Cortex®-M4F MCU with up to 256KB of Flash, 256KB of SRAM, Full Speed USB connectivity, enhanced Security, and QuadSPI for interfacing to Serial NOR flash

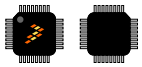
The K82 sub-family extends Kinetis products with new hardware security mechanisms including decryption from serial NOR flash memory, AES128, AES256 with side band attack protection, and Elliptical Curve Cryptography acceleration. These advancements are done while maintaining a high level of compatibility with previous Kinetis devices. The MCUs range in total flash space upto 256KB and have 256KB of SRAM. The QuadSPI interface supports connections to Non-Volatile Memory for data or code. The extended memory resources and new security features allow developers to enhance their embedded applications with greater capability.

MK82FN256VDC15
MK82FN256VLL15
MK82FN256VLQ15
MK82FN256CAx15

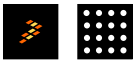
121 XFBGA (DC)
8 x 8 x 0.5 mm Pitch 0.65 mm



100 LQFP (LL)
14 x 14 x 1.7 Pitch 0.5mm



144 LQFP (LQ)
20 x 20 x 1.6 Pitch 0.5 mm



121 WLCSP (Ax)
4.64 mm x 4.53 mm

Performance

- Up to 150 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit

Memories and memory expansion

- Up to 256 KB program flash with 256 KB RAM
- FlexBus external bus interface and SDRAM controller
- Dual QuadSPI with OTF decryption and XIP
- 32 KB Boot ROM with built in bootloader
- Supports SDR and DDR serial flash and octal configurations

System and Clocks

- Multiple low-power modes
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference

Timers

- One 4 ch-Periodic interrupt timer
- Two 16-bit low-power timer PWM modules
- Two 8-ch motor control/general purpose/PWM timers
- Two 2-ch quadrature decoder/general purpose timers
- Real-time clock with independent 3.3V power domain
- Programmable delay block

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- General-purpose input/output

Analog modules

- One 16-bit SAR ADCs, two 6-bit DAC and one 12-bit DAC
- Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Voltage reference 1.2V

Operating Characteristics

- Main VDD Voltage and Flash write voltage range:1.71V–3.6 V
- Temperature range (ambient): -40 to 105°C
- Independent V_{DDIO} for PORTE (QuadSPI): 1.71V–3.6 V

Communication interfaces

- USB full-/low-speed On-the-Go controller
- Secure Digital Host Controller (SDHC) and FlexIO
- One I2S module, three SPI, four I2C modules and five LPUART modules

Security

- LP Trusted Crypto (LTC) hardware accelerators supporting AES, DES, 3DES, RSA and ECC
- Hardware random-number generator
- Supports DES, AES, SHA accelerator (CAU)
- Multiple levels of embedded flash security

Ordering Information

Part Number	Memory		Maximum number of I\O's
	Flash	SRAM	
MK82FN256VDC15	256 KB	256 KB	87
MK82FN256VLL15	256 KB	256 KB	66
MK82FN256CAx15R [1]	256 KB	256 KB	87
MK82FN256VLQ15[2]	256 KB	256 KB	102

1. The 121-pin WLCSP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.
2. The 144-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Related Resources

Type	Description	Resource
Product Selector	The Product Selector lets you find the right Kinetis part for your design.	K-Series Product Selector
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	K8x Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K82P121M150SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_K_1N03P[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 100-pin: 98ASS23308W[1] • XFBGA 121-pin: 98ASA00595D[1] • LQFP 144-pin: 98ASS23177W[2] • WLCSP 121-pin: Under development[2]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. This package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

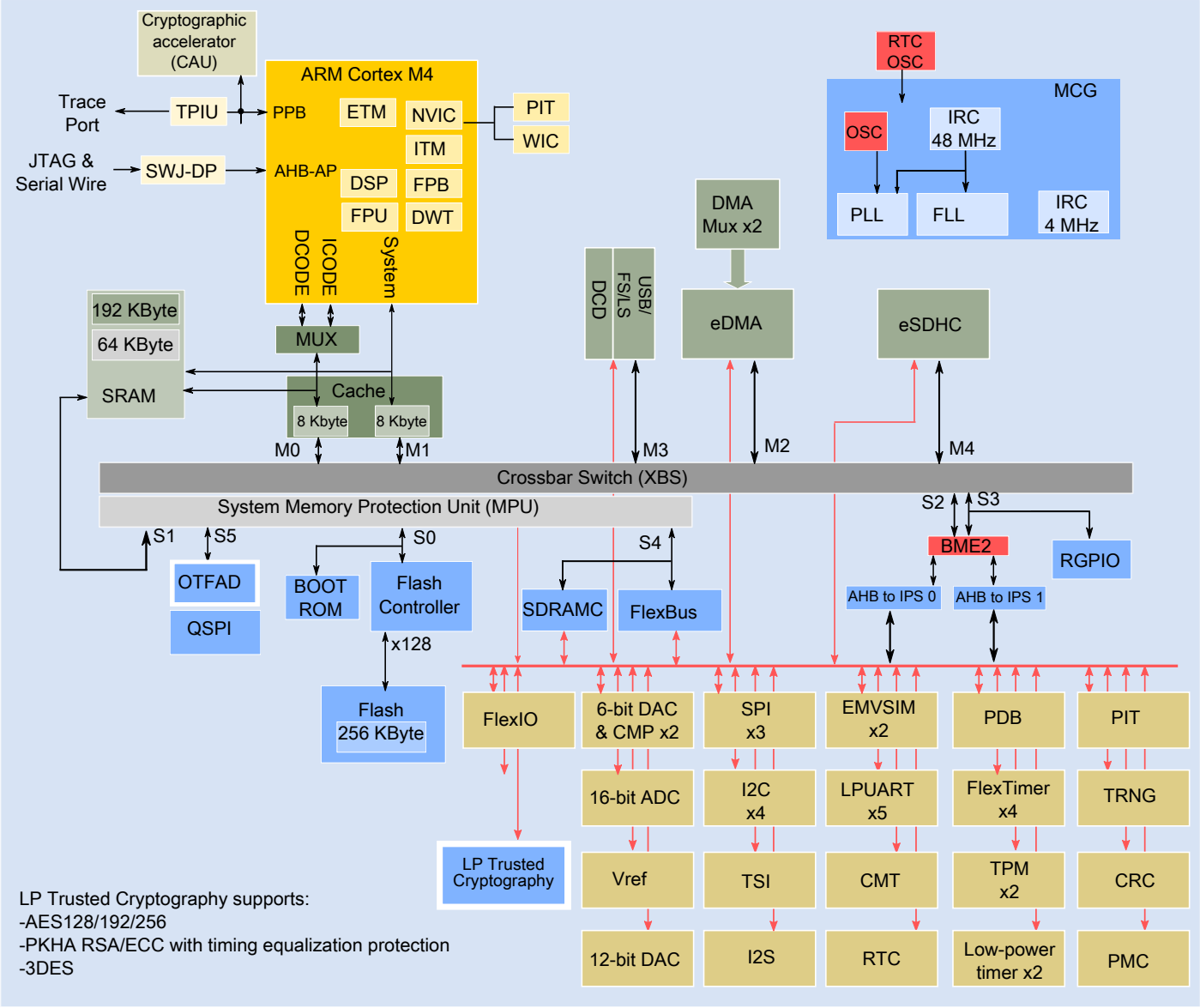


Figure 1. K82 Block Diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{DDIO_E}	V_{DDIO_E} is an independent voltage supply for PORTE [1]	–0.3	3.8	V
V_{BAT}	RTC supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{IO}	Input voltage (except PORTE, VBAT domain pins, and USB0)[2]	–0.3	V_{DD} + 0.3	V
V_{IO_E}	PORTE input voltage[3]	–0.3	V_{DDIO_E} + 0.3	V
I_D	Maximum current single pin limit (digital output pins)	–25	25	mA
VREGIN	USB regulator input	–0.3	6.0	V
V_{USB0_Dx}	USB0_DP and USB_DM input voltage	–0.3	3.63	V

1. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD}. However, it is required that the V_{DD} domain be powered up before V_{DDIO_E}. V_{DDIO_E} must never be higher than V_{DD} during power ramp up, or power down. V_{DD} and V_{DDIO_E} may ramp together if tied to the same power supply.
2. Includes ADC, CMP, and RESET_b inputs.
3. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when $V_{DD} \geq V_{DDIO\_E}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{DD} < V_{DDIO\_E}$.

1.4.1 Recommended POR Sequencing

Cases

- VDD = VDDIO_E
- VDD > VDDIO_E
- VDD < VDDIO_E

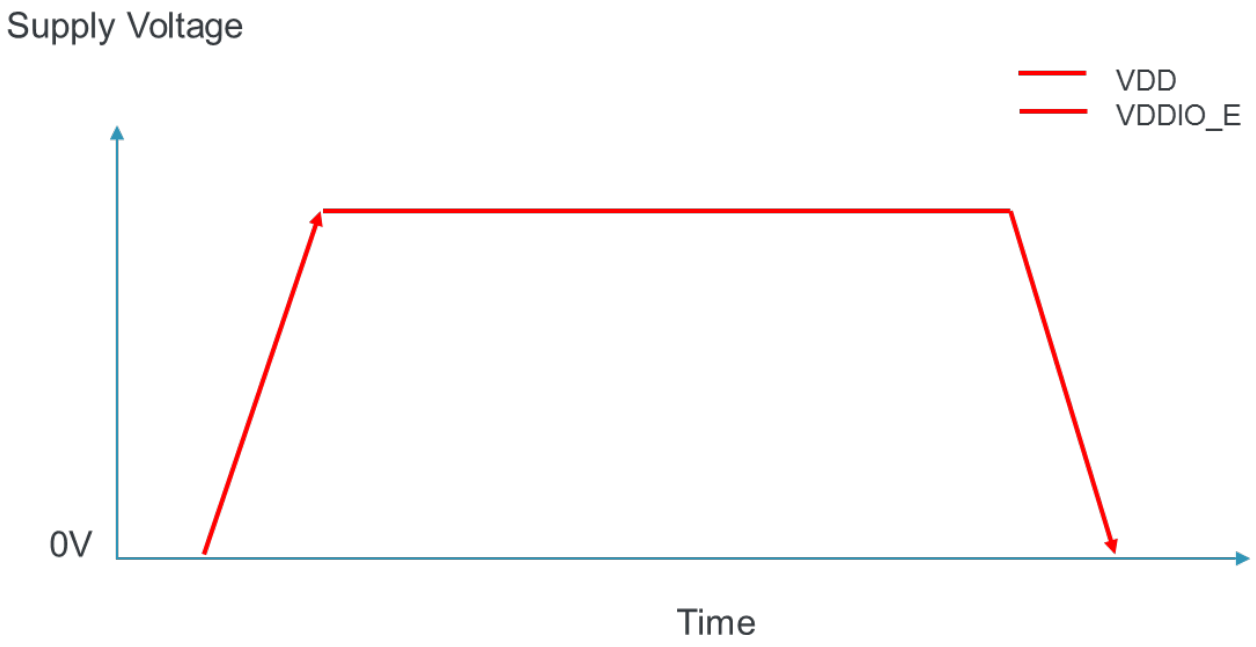


Figure 2. VDD = VDDIO_E

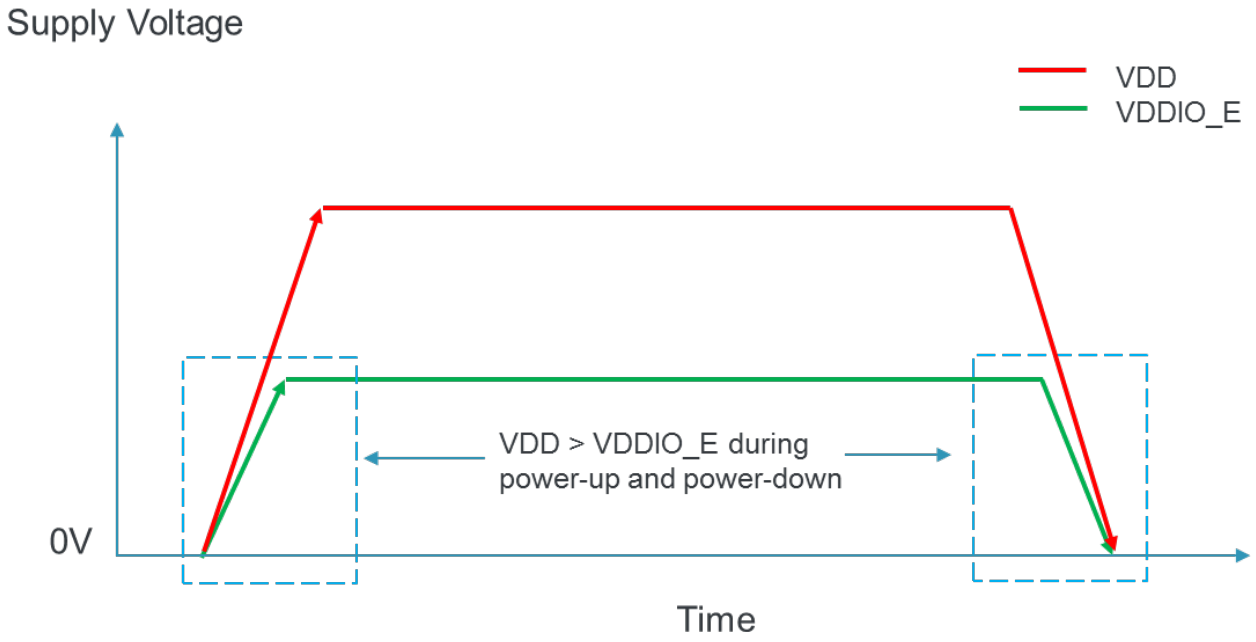


Figure 3. VDD > VDDIO_E

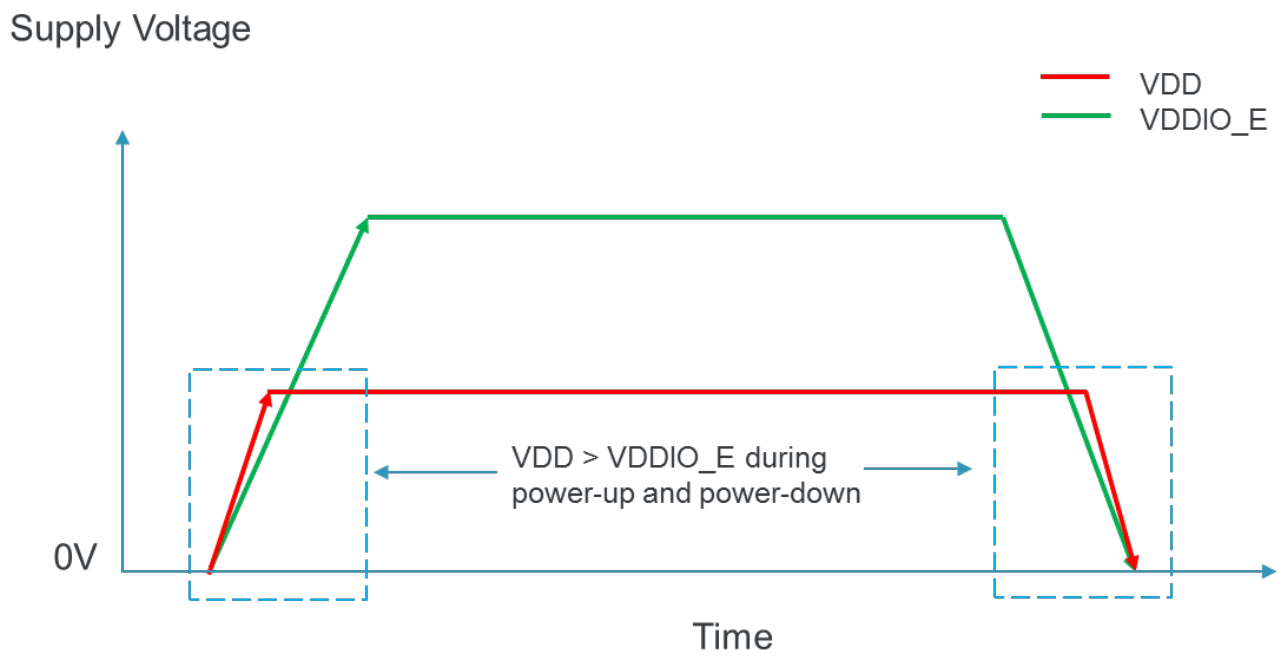


Figure 4. VDD < VDDIO_E

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

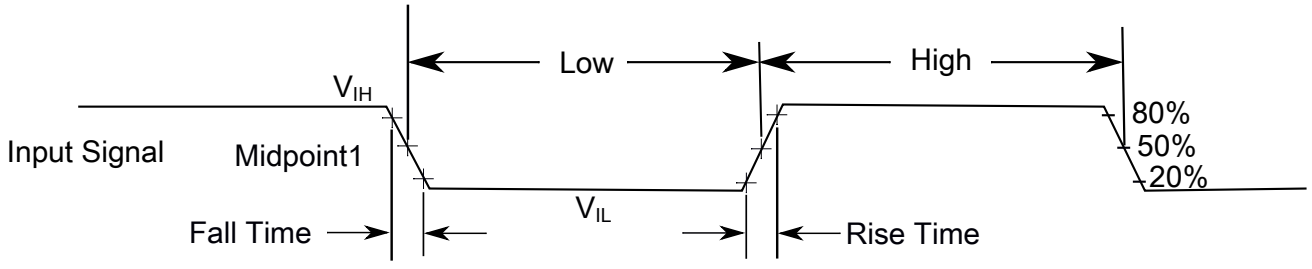


Figure 5. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins

- have C_L=15pF loads,
- are slew rate disabled, and
- are normal drive strength

2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDIO_E}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	— —	0.35 × V_{DD} 0.3 × V_{DD}	V V	
V_{IH_E}	Input high voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	0.7 × V_{DDIO_E} 0.75 × V_{DDIO_E}	— —	V V	
V_{IL_E}	Input low voltage • 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V • 1.7 V ≤ V_{DDIO_E} ≤ 2.7 V	— —	0.35 × V_{DDIO_E} 0.3 × V_{DDIO_E}	V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
V_{HYS_E}	Input hysteresis	0.06 × V_{DDIO_E}	—	V	
I_{ICIO}	I/O pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	1

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Pseudo Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} or V_{DDIO_E}. If V_{IN} is less than -0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(-0.3-V_{IN})/|I_{ICIO}|$. The actual resistor value should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to VDD.

2.2.2 HVD, LVD and POR operating requirements

Table 2. V_{DD} supply HVD, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HVDH}	High Voltage Detect (High Trip Point)	—	3.72	—	V	
V_{HVDL}	High Voltage Detect (Low Trip Point)	—	3.46	—	V	
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	40	—	mV	

Table continues on the next page...

Table 2. V_{DD} supply HVD, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

NOTE

There is no LVD circuit for VDDIO domain

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive strength					2, 3
	IO Group 1					
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5mA	V_{BAT} – 0.5	—	—	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -5mA	V_{DD} – 0.5	—	—	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -5mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -2.5mA	V_{DDIO_E} – 0.5	—	—	V	
	Output high voltage — High drive strength					2
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
	IO Group 4	V_{DDIO_E} – 0.5	—	—	V	
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OH} = -15mA	V_{DDIO_E} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OH} = -7.5mA					
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — normal drive strength					2, 4, 5
	IO Group 1					

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = -5mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = -2.5mA	—	—	0.5	V	
	IO Groups 2 and 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -10mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -5mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -5mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -2.5mA	—	—	0.5	V	
	Output low voltage — High drive strength					2, 4
	IO Group 3					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = -20mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = -10mA	—	—	0.5	V	
	IO Group 4					
	• 2.7 V ≤ V_{DDIO_E} ≤ 3.6 V, I_{OL} = -15mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DDIO_E} ≤ 2.7 V, I_{OL} = -7.5mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current					6, 7, 8
	V_{DD} domain pins	—	0.002	0.5	µA	
	• V_{SS} ≤ V_{IN} ≤ V_{DD}	—	0.002	0.5	µA	
	PORTE pins					
	• V_{SS} ≤ V_{IN} ≤ V_{DDIO_E}	—	0.002	0.5	µA	
	V_{BAT} domain pins					
	• V_{SS} ≤ V_{IN} ≤ V_{BAT}					
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	kΩ	9
R_{PD}	Internal pulldown resistors (except RTC_WAKEUP pins)	20	—	50	kΩ	10

1. Typical values characterized at 25°C and V_{DD} = 3.6V unless otherwise noted.
2. IO Group 1 includes V_{BAT} domain pins: RTC_WAKEUP_b. IO Group 2 includes V_{DD} domain pins: PORTA, PORTB, PORTC, and PORTD, except PTA4. IO Group 3 includes V_{DD} domain pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. IO Group 4 includes V_{DDIO_E} domain pins: PORTE.
3. PTA4 has lower drive strength: I_{OH} = -5mA for high V_{DD} range; I_{OH} = -2.5mA for low V_{DD} range.
4. Open drain outputs must be pulled to V_{DD}.
5. PTA4 has lower drive strength: I_{OL} = 5mA for high V_{DD} range; I_{OL} = 2.5mA for low V_{DD} range.
6. V_{DD} domain pins include ADC, CMP, and RESET_b inputs. Measured at V_{DD} = 3.6V.
7. PORTE analog input voltages cannot exceed V_{DDIO_E} supply when V_{DD} ≥ V_{DDIO_E}. PORTE analog input voltages cannot exceed V_{DD} supply when V_{DD} < V_{DDIO_E}.
8. V_{BAT} domain pins include EXTAL32, XTAL32, and RTC_WAKEUP_b pins.
9. Measured at minimum supply voltage and V_{IN} = V_{SS}
10. Measured at minimum supply voltage and V_{IN} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100MHz
- Bus clock = 50MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	
	• VLLS0 –> RUN	—	154	µs	
	• VLLS1 –> RUN	—	154	µs	
	• VLLS2 –> RUN	—	92	µs	
	• VLLS3 –> RUN	—	92	µs	
	• LLS2 –> RUN	—	6.3	µs	
	• LLS3 –> RUN	—	6.3	µs	
	• VLPS –> RUN	—	5.3	µs	
	• STOP –> RUN	—	5.3	µs	

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	440	490	540	560	570	580	
	LLS2	490	490	540	560	570	680	
	LLS3	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 7. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					2
	• @ 25°C	—	28	31.55	mA	
	• @ 105°C	—	39.6	50.10		
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					3, 4
	• @ 25°C	—	54	57.55	mA	
	• @ 105°C	—	70	80.50		
I_{DD_RUNCO}	Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V					5
	• @ 25°C	—	25.1	28.65	mA	
	• @ 105°C	—	37.8	48.30		
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from internal flash @ 3.0V					6
	• @ 25°C	—	38	40.70	mA	
	• @ 105°C	—	51.7	65.04		
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from internal flash @ 3.0V					7, 8
	• @ 25°C	—	48	50.70	mA	
	• @ 105°C	—	63.7	77.04		
$I_{DD\_HSRUNCO}$	HSRun mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0V					
	• @ 25°C	—	34.5	37.2	mA	
	• @ 105°C	—	50.3	63.64		
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled					9
	• @ 25°C	—	14.2	19.87	mA	
	• @ 105°C	—	26.2	35.66		
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks enabled					9
		—	24.4	30.07	mA	

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 25°C • @ 105°C	— —	36.6 —	46.06 —		
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled • @ 25°C • @ 105°C	— —	0.94 3.99	1.10 7.62	mA	10
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled • @ 25°C • @ 105°C	— —	1.36 4.4	1.52 8.03	mA	11
$I_{DD\_VLPRCO\_CM}$	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from internal flash at 3.0 V • @ 25°C • @ 105°C	— —	1000 3650	— —	µA	12
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V • @ 25°C • @ 105°C	— —	3.95 17.71	5.75 27.15	mA	5
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled • @ 25°C • @ 105°C	— —	0.45 3.28	0.63 6.87	mA	13
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks enabled • @ 25°C • @ 105°C	— —	0.75 3.6	0.93 7.19	mA	
I_{DD_STOP}	Stop mode current at 3.0 V • @ 25°C • @ 105°C	— —	0.55 5.67	0.85 9.59	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ 25°C • @ 105°C	— —	91.48 1798.38	240.90 3796.94	µA	
I_{DD_LLS2}	Low leakage stop mode current at 3.0 V • @ 25°C • @ 105°C	— —	4.94 73.68	7.14 121.9	µA	

Table continues on the next page...

Table 7. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_LLS3}	Low leakage stop mode current at 3.0 V • @ 25°C • @ 105°C	 — —	 7.78 160.91	 13.16 284.31	 µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ 25°C • @ 105°C	 — —	 5.63 117.89	 9.34 202.55	 µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ 25°C • @ 105°C	 — —	 3.13 29.49	 4.04 48.7	 µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ 25°C • @ 105°C	 — —	 1.05 15.31	 1.36 18.56	 µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ 25°C • @ 105°C	 — —	 0.62 13.92	 0.84 16.95	 µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ 25°C • @ 105°C	 — —	 0.33 13.42	 0.53 16.44	 µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V • @ 25°C • @ 105°C	 — —	 0.19 2.56	 0.23 3.71	 µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers @ 1.8V • @ 25°C • @ 105°C	 — —	 0.57 2.52	 0.64 5.82	 µA	14

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 150 MHz core and system clock, 75 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configure for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. MCG configured for PEE mode.
6. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.

7. 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
8. Max values are measured with CPU executing DSP instructions.
9. 120 MHz core and system clock, 60MHz bus clock, and FlexBus. MCG configured for PEE mode.
10. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
11. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
12. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
13. 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
14. Includes 32kHz oscillator current and RTC operation.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE
- V_{DD}=V_{DDA}=V_{DDIO_E}

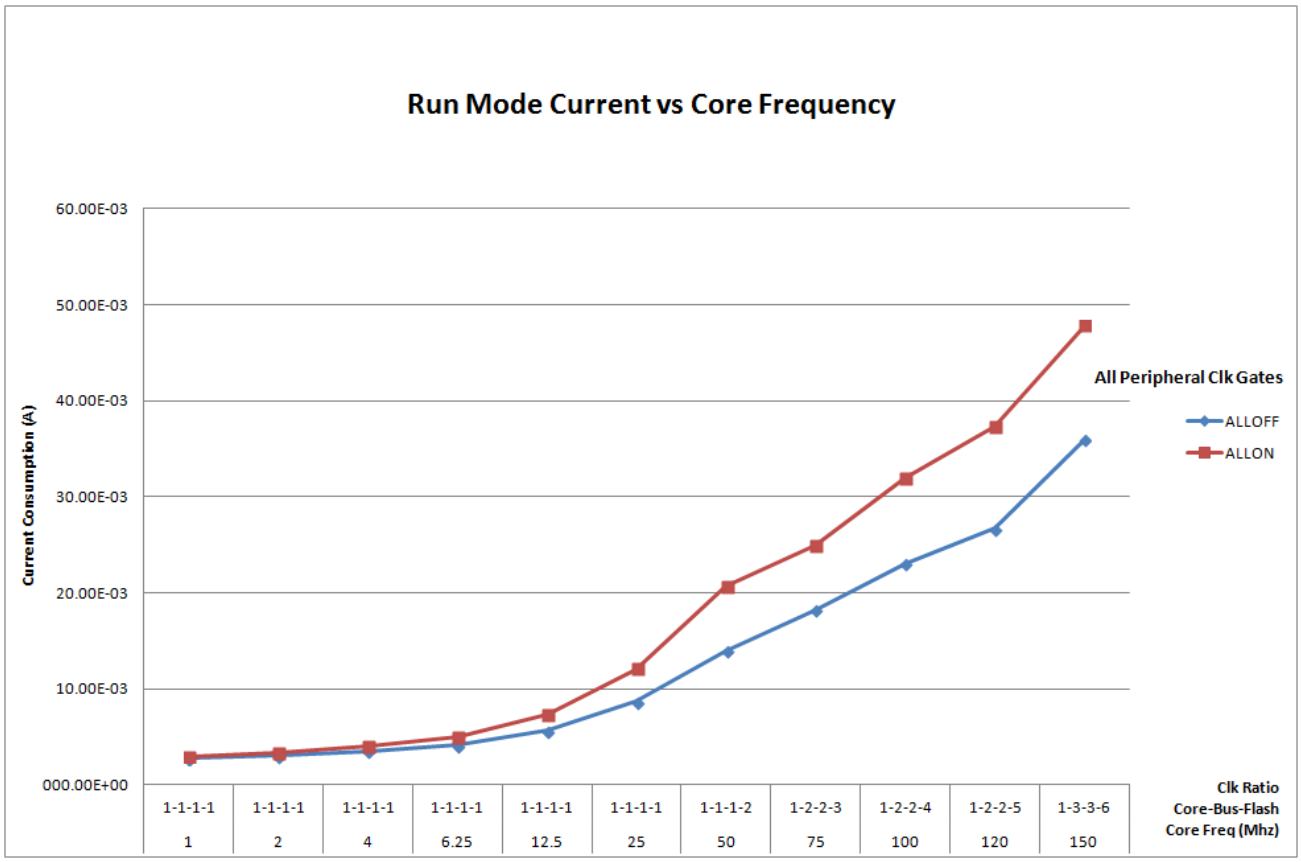


Figure 6. Run mode supply current vs. core frequency

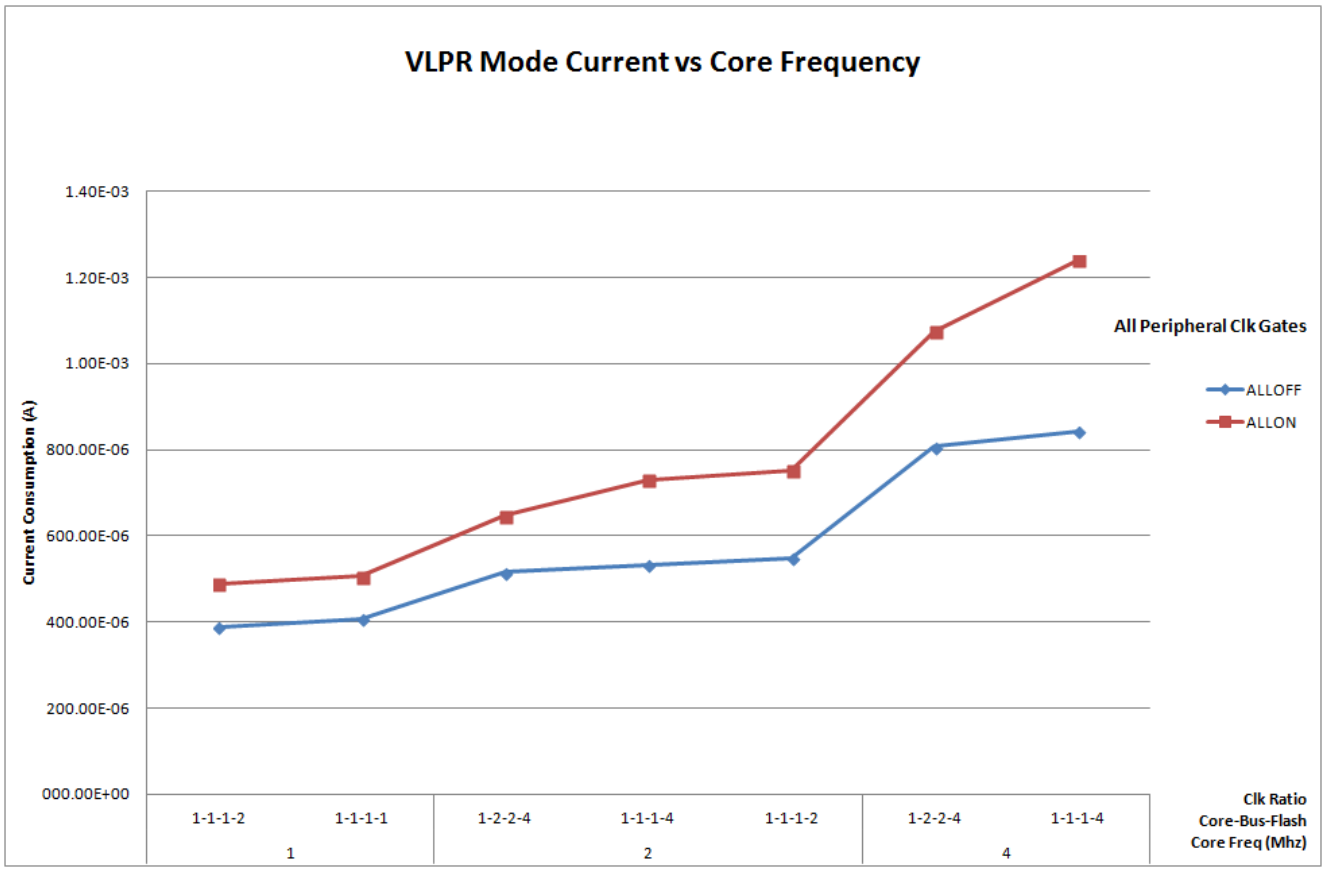


Figure 7. VLPR mode supply current vs. core frequency

2.2.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from Freescale on request.

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	150	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	75	MHz	
FB_CLK	FlexBus clock	—	75	MHz	
f_{FLASH}	Flash clock	—	28	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
$f_{FlexCAN\_ERCLK}$	FlexCAN external reference clock	—	8	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, timers, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External RESET_b input pulse width (digital glitch filter disabled)	100	—	ns	
	Port rise and fall time (high drive strength) • Slew enabled • 1.71 ≤ V_{DD} ≤ 2.7V • 2.7 ≤ V_{DD} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7V • 2.7 ≤ V_{DD} ≤ 3.6V	 — — — —	 34 16 10 8	 ns ns ns ns	4, 5
	Port rise and fall time (low drive strength) • Slew enabled • 1.71 ≤ V_{DD} ≤ 2.7V • 2.7 ≤ V_{DD} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7V • 2.7 ≤ V_{DD} ≤ 3.6V	 — — — —	 34 16 7 5	 ns ns ns ns	6, 7
	Port rise and fall time (high drive strength) • Slew enabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V	 — — — —	 34 16 7 5	 ns ns ns ns	5, 8
	Port rise and fall time (low drive strength) • Slew enabled	 — —	 34 16	 ns ns	7, 8

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V • Slew disabled • 1.71 ≤ V_{DDIO_E} ≤ 2.7V • 2.7 ≤ V_{DDIO_E} ≤ 3.6V	— —	7 5	ns ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.
5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1,

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

   $T_J = T_A + \theta_{JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	100 LQFP	121 XFBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	52	71	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	39	36.8	°C/W	1

Table continues on the next page...

Table 12. Thermal attributes (continued)

Board type	Symbol	Description	100 LQFP	121 XFBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	55	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	33	32.2	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	18	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	12.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	0.25	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 13. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

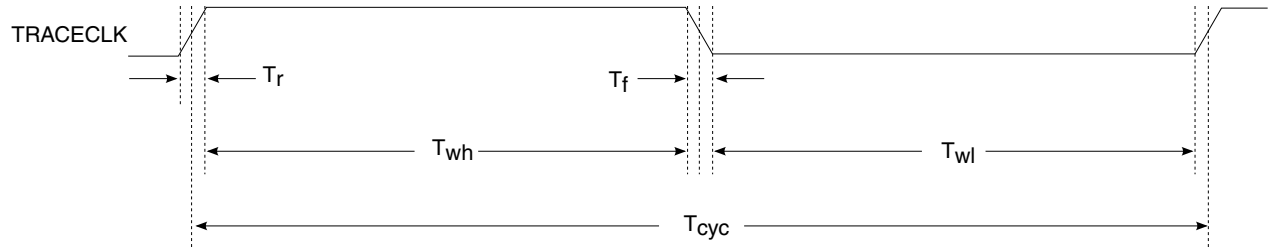


Figure 8. TRACE_CLKOUT specifications

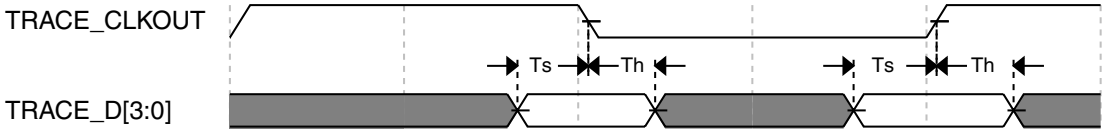


Figure 9. Trace data specifications

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...