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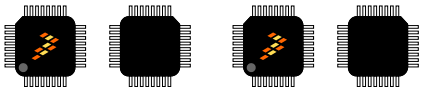
Kinetis KE1xF with up to 512 KB Flash

Up to 168 MHz ARM® Cortex®-M4 Based Microcontroller

MKE1xF512VLL16
MKE1xF512VLH16
MKE1xF256VLL16
MKE1xF256VLH16

The KE1xF microcontroller is built on the ARM® Cortex®-M4 processor with stronger performance and higher memory densities in multiple packages. This device offers up to 168 MHz performance with integrated single-precision floating point unit (FPU) and digital signal processor (DSP). Embedded flash memory sizes range from 256 KB to 512 KB.



100 LQFP (LL)
14x14x1.4 mm Pitch
0.5 mm

64 LQFP (LH)
10x10x1.4 mm Pitch
0.5 mm

Core Processor and System

- ARM® Cortex®-M4 core, supports up to 168 MHz frequency with 1.25 Dhrystone MIPS per MHz
- ARM Core based on the ARMv7 Architecture and Thumb®-2 ISA
- Integrated Digital Signal Processor (DSP)
- Configurable Nested Vectored Interrupt Controller (NVIC)
- Single-precision Floating Point Unit (FPU)
- 16-channel DMA controller extended up to 64 channels with DMAMUX

Reliability, safety and security

- Error-correcting code (ECC) on Flash and SRAM memories
- System memory protection unit (MPU) module
- Flash Access Control (FAC)
- Cyclic Redundancy Check (CRC) generator module
- 128-bit unique identification (ID) number
- Internal watchdog (WDOG) with independent clock source
- External watchdog monitor (EWM) module
- ADC self calibration feature
- On-chip clock loss monitoring

Human-machine interface (HMI)

- Supports up to 92 interrupt request (IRQ) sources
- Up to 89 GPIO pins with interrupt functionality
- 8 high drive pins
- Digital filters

Memory and memory interfaces

- Up to 512 KB program flash with ECC
- Up to 64 KB SRAM with ECC
- 64 KB FlexNVM with ECC for data flash and with EEPROM emulation
- 4 KB FlexRAM for EEPROM emulation
- 8 KB I/D cache to minimize performance impact of memory access latencies
- Boot ROM with built in bootloader

Mixed-signal analog

- 3× 12-bit analog-to-digital converter (ADC) with up to 16 channel analog inputs per module, up to 1M sps
- 3× high-speed analog comparators (CMP) with internal 8-bit digital to analog converter (DAC)
- 1× 12-bit digital to analog converter (DAC)

Timing and control

- 4× Flex Timers (FTM) for PWM generation, offering up to 32 standard channels
- 1× Low-Power Timer (LPTMR) working at Stop mode, with flexible wake up control
- 3× Programmable Delay Block (PDB) with flexible trigger system, to provide accurate delay and trigger generation for inter-module synchronization
- 1× Low-power Periodic Interrupt Timer (LPIT) with 4 independent channels, for general purpose
- Pulse Width Timer (PWT)
- Real timer clock (RTC)

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

Clock interfaces

- 3 - 40 MHz fast external oscillator (OSC)
- 32 kHz slow external oscillator (OSC32)
- 48 - 60 MHz high-accuracy (up to 1%) fast internal reference clock (FIRC) for high-speed run
- 8 MHz / 2 MHz high-accuracy (up to 3%) slow internal reference clock (SIRC) for low-speed run
- 128 kHz low power oscillator (LPO)
- Phased lock loop (PLL)
- Up to 60 MHz DC external square wave input clock
- System clock generator (SCG)
- Real time counter (RTC)

Power management

- Low-power ARM Cortex-M4 core with excellent energy efficiency
- Power management controller (PMC) with multiple power modes: HSRun, Run, Wait, Stop, VLPR, VLPW and VLPS
- Supports clock gating for unused modules, and specific peripherals remain working in low power modes
- POR, LVD/LVR

Operating Characteristics

- Voltage range: 2.7 to 5.5 V
- Ambient temperature range: –40 to 105 °C

Connectivity and communications interfaces

- TriggerMUX: for module inter-connectivity
- 3× low-power universal asynchronous receiver/ transmitter (LPUART) modules with DMA support and working at Stop mode
- 2 low-power serial peripheral interface (LPSPI) modules with DMA support and working at Stop mode
- 2× low-power inter-integrated circuit (LPI2C) modules with DMA support and working at Stop mode
- Up to 2 ×FlexCAN modules, with flexible message buffers and mailboxes
- FlexIO module for flexible and high performance serial interfaces emulation

Debug functionality

- Serial Wire JTAG Debug Port (SWJ-DP) combines
- Debug Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Test Port Interface Unit (TPIU)
- Flash Patch and Breakpoints (FPB)

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KE1xF512PB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KE1xFP100M168SF0RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KE1xFP100M168SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_E_0N79P [1]
Package drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W 64-LQFP: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

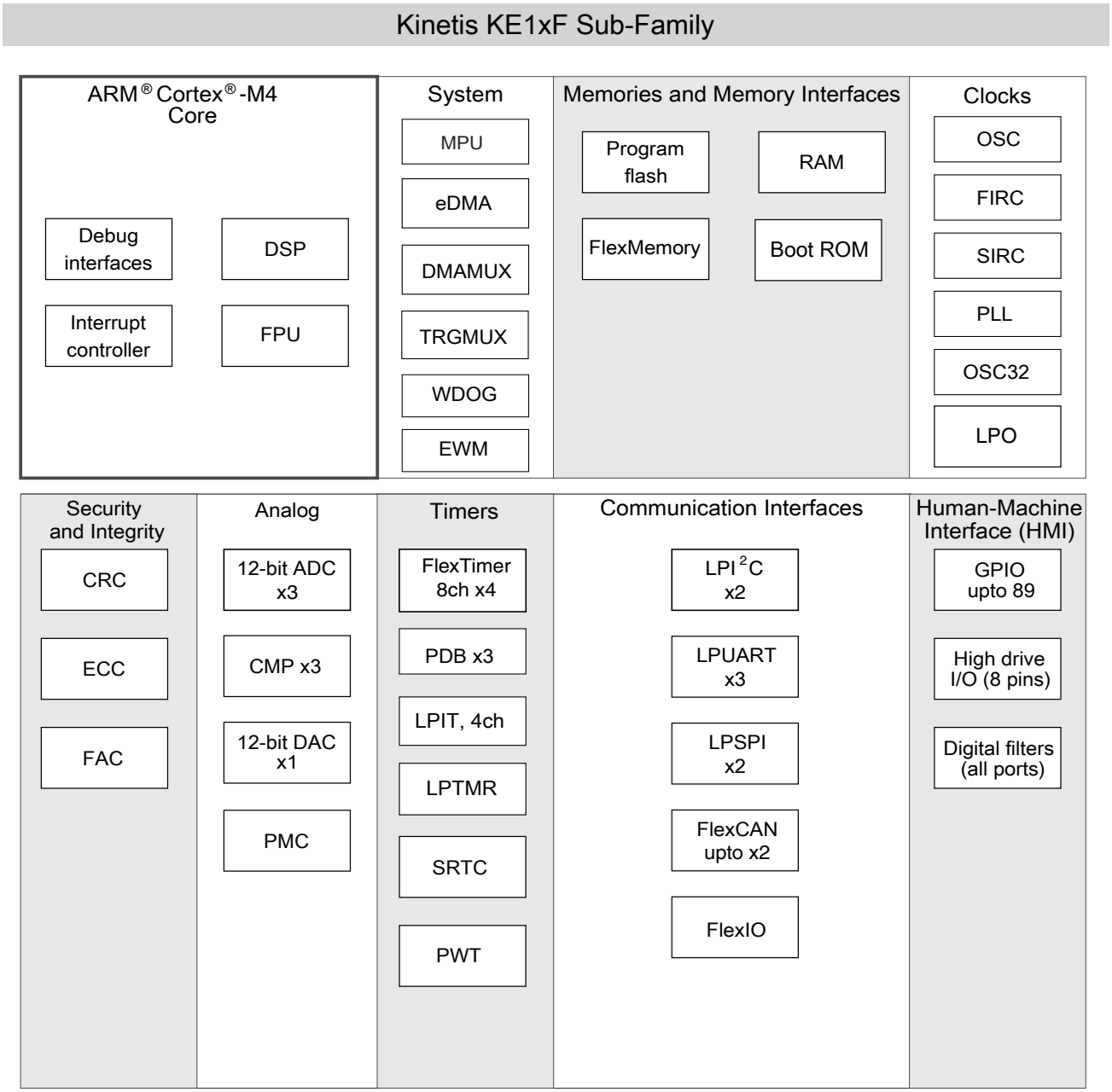


Figure 1. Functional block diagram

Table of Contents

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory			Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels	FlexCAN
MKE18F512VLL16	MKE18F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	2
MKE18F512VLH16	MKE18F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	2
MKE18F256VLL16	MKE18F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	2
MKE18F256VLH16	MKE18F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	2
MKE16F512VLL16	MKE16F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	1
MKE16F512VLH16	MKE16F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	1
MKE16F256VLL16	MKE16F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	1
MKE16F256VLH16	MKE16F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	1
MKE14F512VLL16	MKE14F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	0
MKE14F512VLH16	MKE14F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	0
MKE14F256VLL16	MKE14F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	0
MKE14F256VLH16	MKE14F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	0

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device.

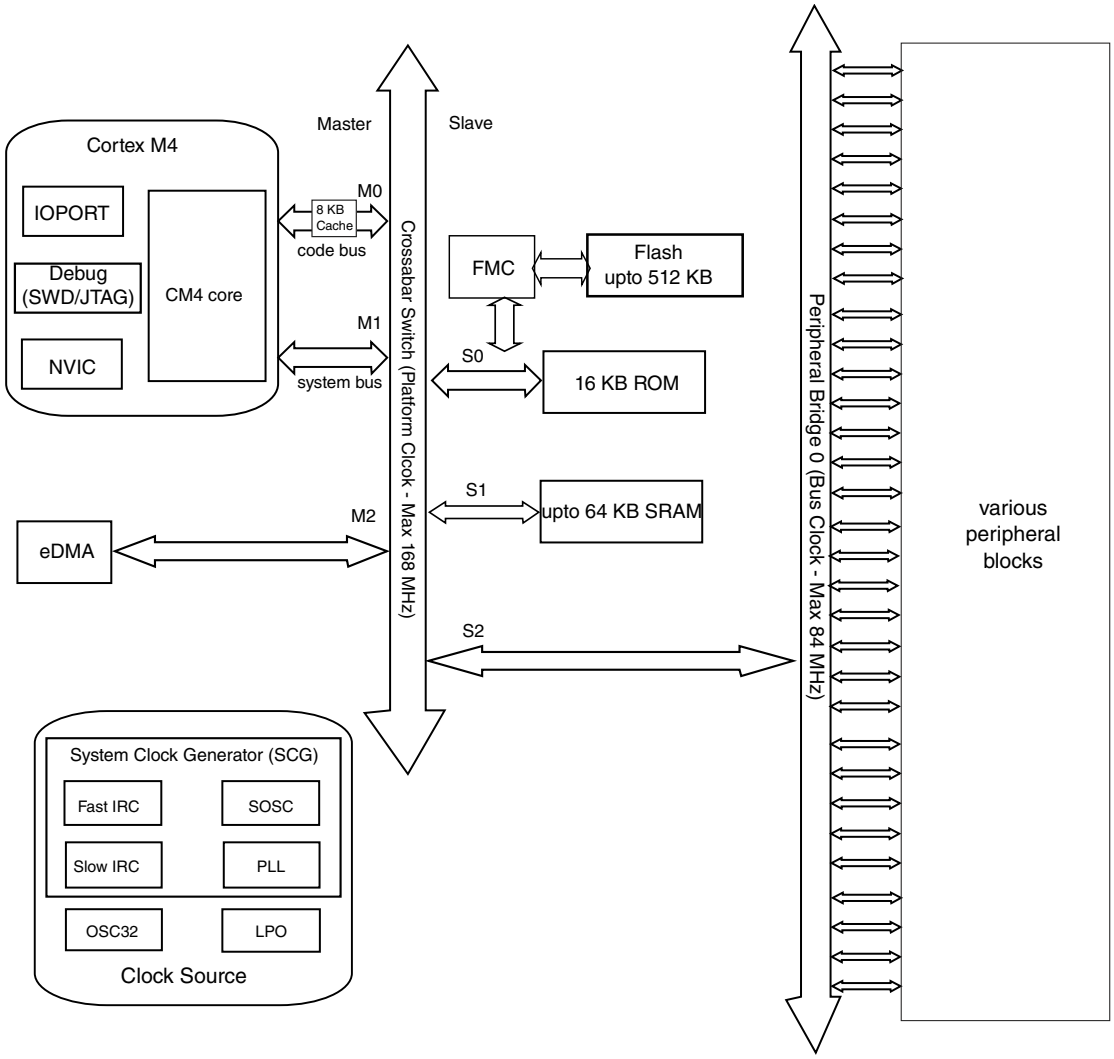


Figure 2. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	RESET pin, WDOG, JTAG , loss of clock(LOC) reset and loss of lock (LOL) reset
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	ADCx is optional functional with clock source from SIRC or OSC
CMPx	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPI2C	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPUART	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPSPI	Functional in Stop/VLPS modes with clock source from SIRC or OSC

Table continues on the next page...

Table 2. AWIC Stop and VLPS Wake-up Sources (continued)

Wake-up source	Description
LPIT	Functional in Stop/VLPS modes with clock source from SIRC or OSC
FlexIO	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPTMR	Functional in Stop/VLPS modes
RTC	Functional in Stop/VLPS modes
SCG	Functional in Stop mode (Only SIRC)
CAN	CAN stop wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- Upto 512 KB of embedded program flash memory.
- Upto 64 KB of embedded SRAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into several arrays:
  - 64 KB of embedded data flash memory
  - 4 KB of Emulated EEPROM
  - 16 KB ROM (built-in bootloader to support UART, I2C, and SPI interfaces)

The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 4 KB.

The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the

specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules									
		PMC	SIM	SMC	RCM	Reset pin is negated	WDOG	SCG	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	Y	N	Y	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Watchdog (WDOG) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of clock (LOC) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of lock (LOL) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Except SMC_PMPROT, SMC_PMCTRL_RUM, SMC_PMCTRL_STOPM, SMC_STOPCTRL, SMC_PMSTAT
4. Except RCM_RPC, RCM_MR, RCM_FM, RCM_SRIE, RCM_SRS, RCM_SSRS
5. Except WDOG_CS[TST]
6. Except SCG_CSR and SCG_FIRCSTAT

This device supports booting from:

- internal flash
- boot ROM

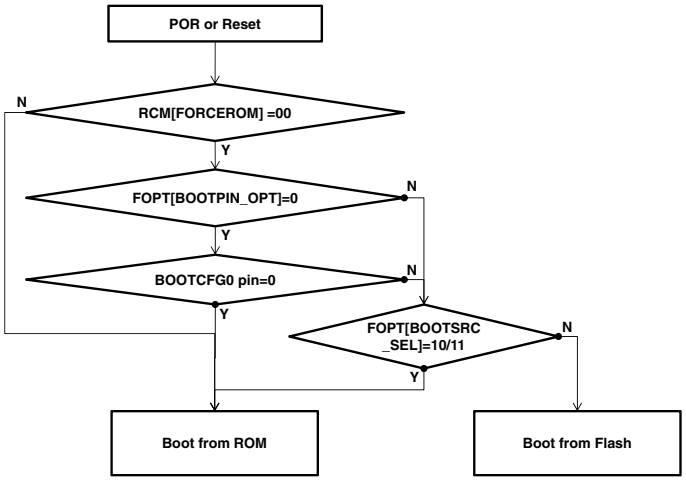


Figure 3. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.1.6 Clock options

The SCG module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory . The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The following figure is a high level block diagram of the clock generation. For more details on the clock operation and configuration, see the Clocking chapter in the Reference Manual.

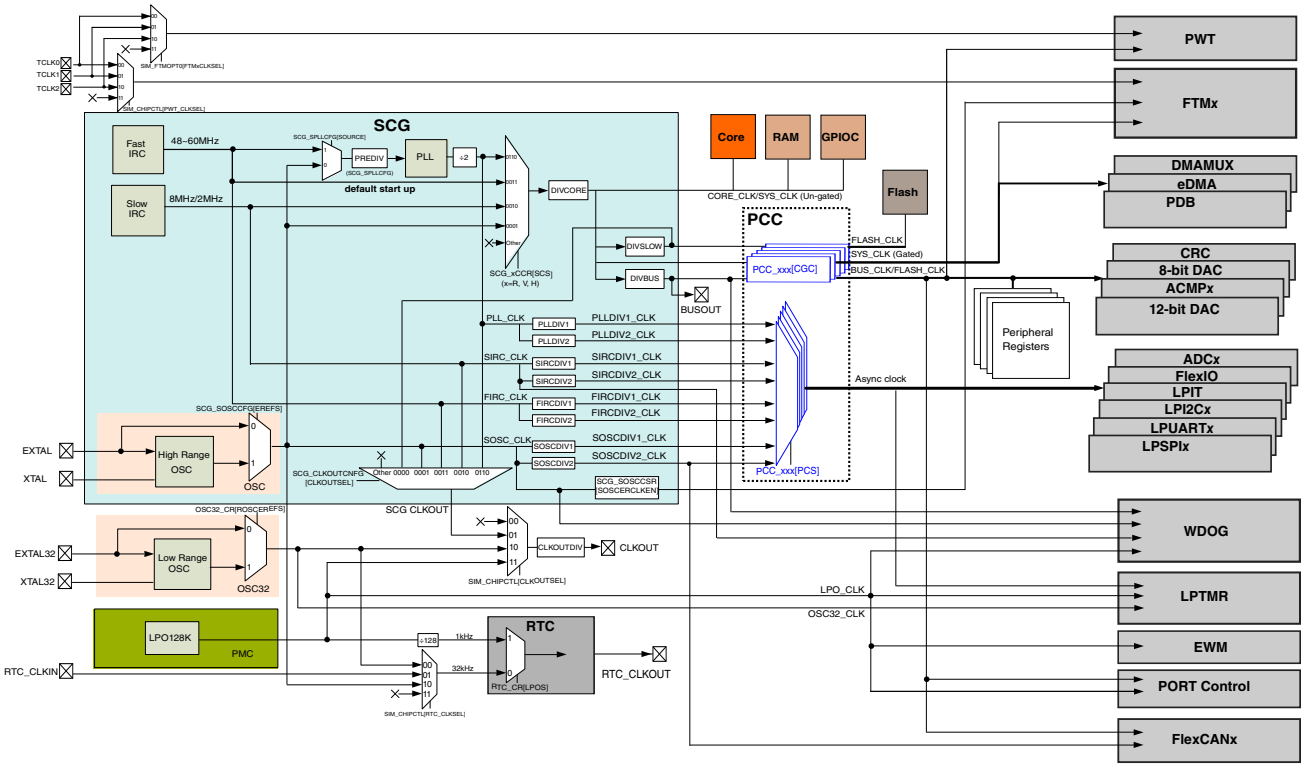


Figure 4. Clocking block diagram

2.1.7 Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD/JTAG port cannot access the memory resources of the MCU.

External interface	Security	Unsecure
SWD/JTAG port	Can't access memory source by SWD/ JTAG interface	the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command

2.1.7.1 Flash Access Control (FAC)

The FAC is a native or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these

segments is controlled as the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

2.1.7.2 Error-correcting code (ECC)

The ECC detection is also supported on Flash and SRAM memories. It supports auto correction of one-bit error and reporting more than one-bit error.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 5. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	High Speed Run	In HSRun mode, MCU is able to operate at a faster frequency, and all device modules are operational.
	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, DAC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.

2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD/JTAG interface.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 16 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- All data movement via dual-address transfers: read from source, write to destination
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.2 FTM

This device contains four FlexTimer modules.

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Several key enhancements of this module are made:

- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

2.2.3 ADC

This device contains three 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 16 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 Vin to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources

- Static operation in Normal Stop mode
- 16-word data buffer supported with multiple operation modes
- DMA support

2.2.5 CMP

There are three analog comparators on this device.

- Each CMP has its own independent 8-bit DAC.
- Each CMP supports up to 7 analog inputs from external pins.
- Each CMP is able to convert an internal reference from the bandgap.
- Each CMP supports internal reference from the on-chip 12-bit DAC out.
- Each CMP supports the round-robin sampling scheme. In summary, this allow the CMP to operate independently in VLPS and Stop modes, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, windowed, or digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: Shorter propagation delay at the expense of higher power, and Low power with longer propagation delay
- DMA transfer support
- Functional in all power modes available on this MCU
- The window and filter functions are not available in STOP mode
- Integrated 8-bit DAC with selectable supply reference source and can be power down to conserve power

2.2.6 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator, or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

2.2.7 LPIT

The Low Power Periodic Interrupt Timer (LPIT) is a multi-channel timer module generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

This device contains one LPIT module with four channels. The LPIT generates periodic trigger events to the DMAMUX.

2.2.8 PDB

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PDB module has the following capabilities:

- trigger input sources and one software trigger source
- 1 DAC refresh trigger output, for this device
- configurable PDB channels for ADC hardware trigger
- 1 pulse output, for this device

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×

- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.12 LPSPI

This device contains two LPSPI modules. The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Host request input can be used to control the start time of an SPI bus transfer

2.2.13 FlexCAN

This device contains two FlexCAN modules. The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

Each FlexCAN module contains 16 message buffers. Each message buffer is 16 bytes.

The FlexCAN module has the following features:

- Flexible mailboxes of zero to eight bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Remote request frames may be handled automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability

2.2.14 LPI2C

This device contains two LPI2C modules. The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

The LPI2C modules have the following features:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- HS-mode supported in slave mode
- Multi-master support including synchronization and arbitration
- Clock stretching
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID require software support
- For master mode:
  - command/transmit FIFO of 4 words
  - receive FIFO of 4 words
- For slave mode:
  - separate I2C slave registers to minimize software overhead due to master/slave switching
  - support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
  - transmit/receive data register supporting interrupt or DMA requests

2.2.15 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer

- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.16 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

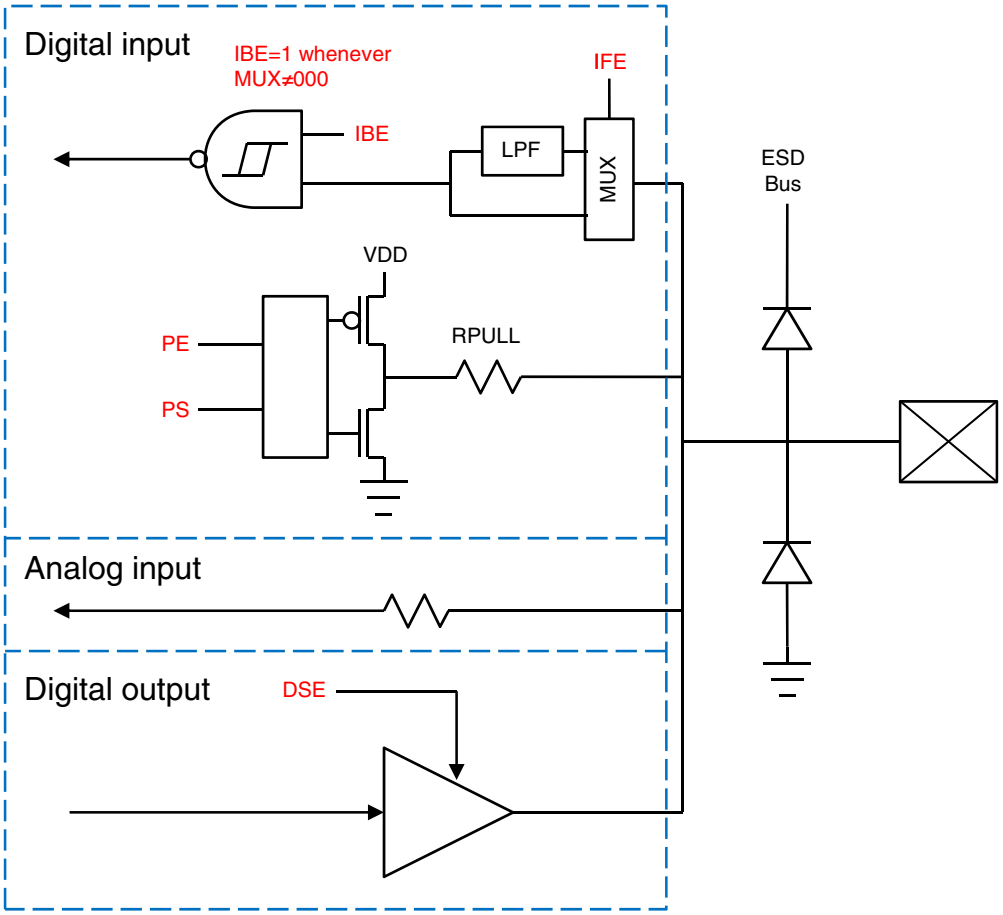


Figure 5. I/O simplified block diagram

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

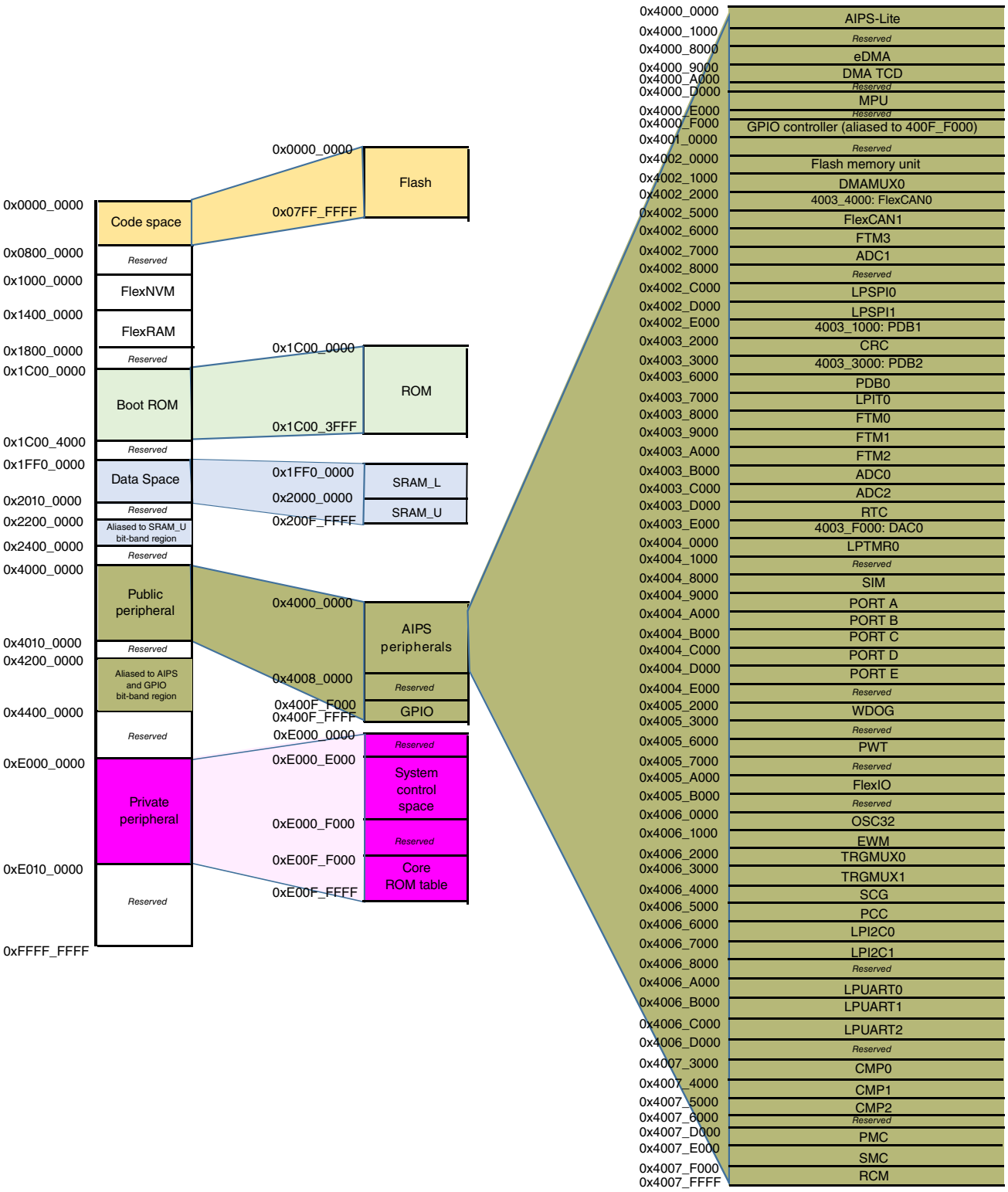


Figure 6. Memory map