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Document Number: KL03P24M48SF0
Rev. 5.1 08/2017

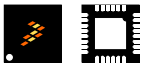
Kinetis KL03 32 KB Flash

48 MHz Cortex-M0+ Based Microcontroller

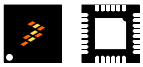
MKL03ZxxVFG4
MKL03ZxxVFK4
MKL03Z32CAF4R
MKL03Z32CBF4R

Supports ultra low power 48 MHz devices with up to 32 KB Flash.
World's smallest MCU based on ARM® technology. Ideal solution for Internet of Things edge nodes design with ultra small form factor and ultra low power consumption. The products offers:

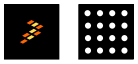
- Tiny footprint packages, including 1.6 x 2.0 mm^2 WLCSP
- Run power consumption as low as 50 µA/MHz
- Static power consumption as low as 2.2 µA with 7.5 µs wakeup time for full retention and lowest static mode down to 77 nA in deep sleep
- Highly integrated peripherals, including new boot ROM and high accurate internal voltage reference, etc



16-pin QFN (FG)
3 x 3 x 0.65 Pitch 0.5 mm



24-pin QFN (FK)
4 x 4 x 0.65 Pitch 0.5 mm



20 WLCSP
2 x 1.61 x 0.56 Pitch 0.4 mm(AF) 2 x 1.61 x 0.32 Pitch 0.4 mm (BF)

Core

- ARM® Cortex®-M0+ core up to 48 MHz

Memories

- Up to 32 KB program flash memory
- 2 KB SRAM
- 8 KB ROM with build-in bootloader
- 16 bytes regfile

System peripherals

- Nine low-power modes to provide power optimization based on application requirements
- COP Software watchdog
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

Clocks

- 48 MHz high accuracy internal reference clock
- 8/2 MHz low power internal reference clock
- 32 kHz to 40 kHz crystal oscillator
- 1 kHz LPO clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C for QFN packages; -40 to 85°C for WLCSP packages

Human-machine interface

- General-purpose input/output up to 22

Communication interfaces

- One 8-bit SPI module
- One LPUART module
- One I2C module supporting up to 1 Mbit/s, with double buffer

Analog Modules

- 12-bit SAR ADC with internal voltage reference, up to 818 ksps and 7 channels
- High-speed analog comparator containing a 6-bit DAC and programmable reference input
- 1.2 V voltage reference (Vref)

Timers

- Two 2-channel Timer/PWM modules
- One low-power timer
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information[1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL03Z8VFG4(R)	8	2	14
MKL03Z16VFG4(R)	16	2	14
MKL03Z32VFG4(R)	32	2	14
MKL03Z32CAF4R	32	2	18
MKL03Z32CBF4R	32	2	18
MKL03Z8VFK4(R)	8	2	22
MKL03Z16VFK4(R)	16	2	22
MKL03Z32VFK4(R)	32	2	22

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL03PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL03P24M48SF0RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL03P24M48SF0[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KL03Z_*x*N86K[2]
Package drawing	Package dimensions are provided in package drawings.	QFN 16-pin: 98ASA00525D[1] QFN 24-pin: 98ASA00602D[1] WLCSP 20-pin: 98ASA00676D[1] WLCSP 20-pin (ultra thin): 98ASA00964D[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.
2. To find the associated resource, go to http://www.nxp.com and perform a search using this term with the “x” replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

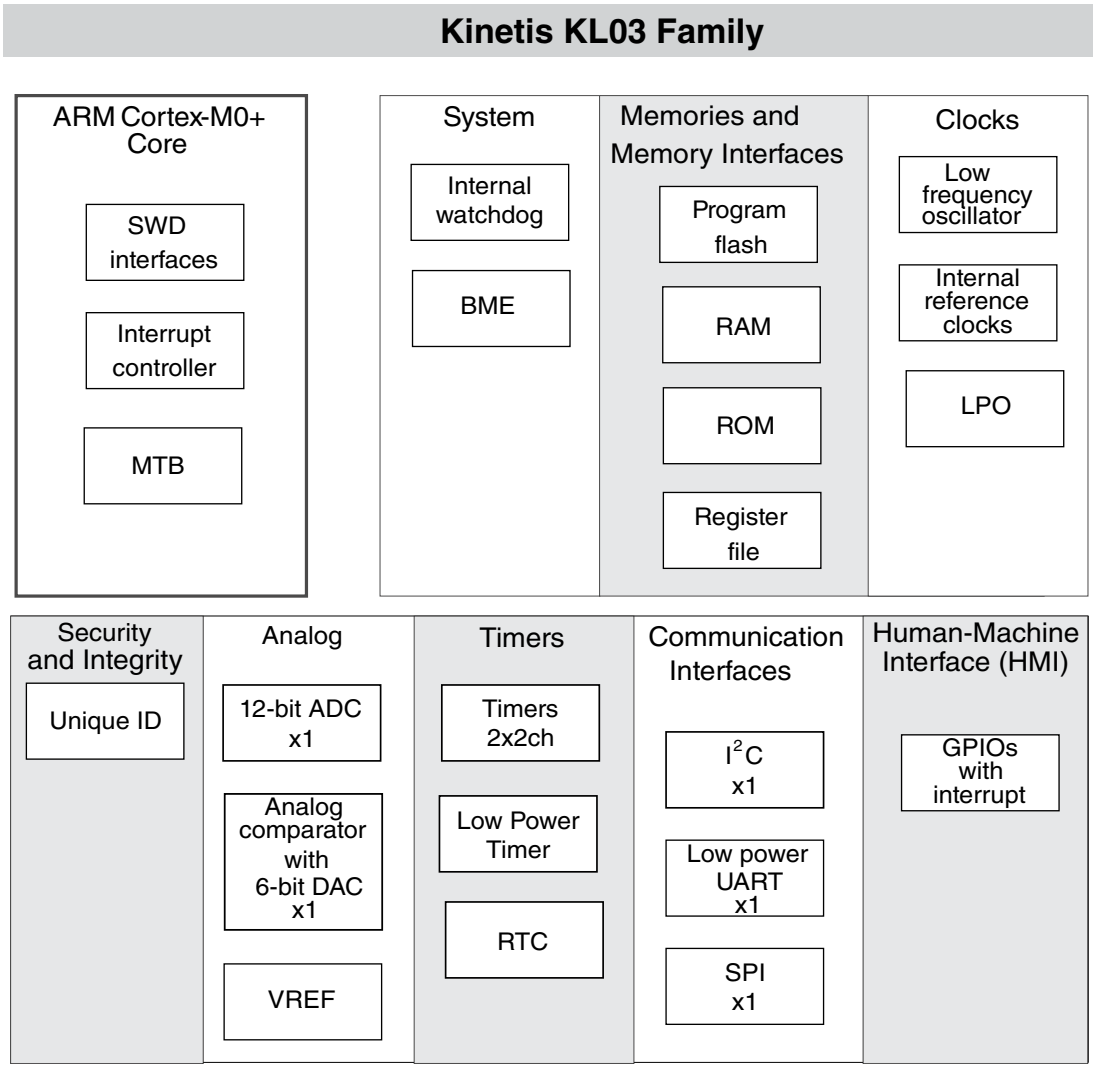


Figure 1. Functional block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. QFN packages moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

Table 3. WLCSP packages moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 4. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 5. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

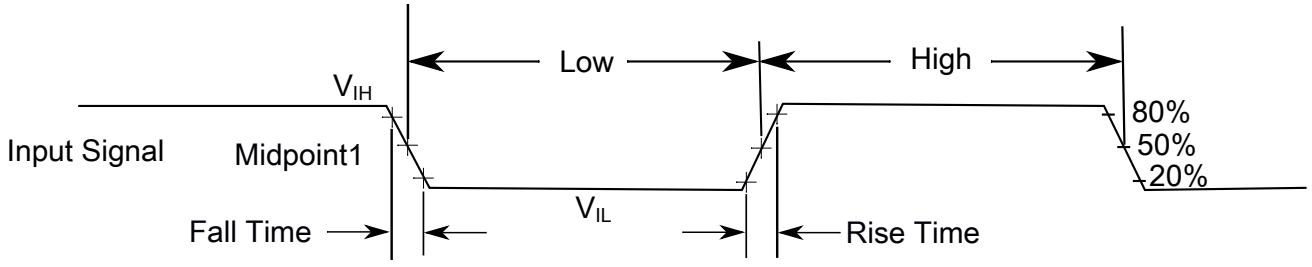


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- C_L=30 pF loads

- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 6. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	—
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	—
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	—
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	—
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	—
I_{ICIO}	IO pin negative DC injection current—single pin • V_{IN} < V_{SS}–0.3V	–5	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	 –25	 —	 mA	—
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	—

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.

2.2.2 LVD and POR operating requirements

Table 7. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 8. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –2.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except $\overline{\text{RESET}}$)				1, 2
		V_{DD} – 0.5	—	V	
		V_{DD} – 0.5	—	V	

Table continues on the next page...

Table 8. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –10 mA				
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —	 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	 — —	 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	—
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

VLLSx→RUN recovery uses LIRC clock mode at the default CPU and system frequency of 8 MHz, and a bus and flash clock frequency of 4 MHz.

Table 9. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Note
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	152	166	µs	—
	• VLLS1 → RUN	—	152	166	µs	—
	• VLLS3 → RUN	—	93	104	µs	—
	• VLPS → RUN	—	7.5	8	µs	—
	• STOP → RUN	—	7.5	8	µs	—

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

Table 10. KL03 QFN packages power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 105 °C	—	5.62	5.84		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 105 °C	—	5.27	5.48		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 105 °C	—	6.16	6.41		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					3

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C	—	3.71	3.86	mA	
	• at 105 °C	—	3.81	3.96		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	2.47	2.57	mA	
	• at 105 °C	—	2.58	2.68		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.43	6.69	mA	
	• at 105 °C	—	6.56	6.82		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					—
	• at 25 °C	—	5.71	5.94	mA	
	• at 105 °C	—	5.82	6.05		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					—
	• at 25 °C	—	3.3	3.43	mA	
	• at 105 °C	—	3.4	3.54		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V					—
	• at 25 °C	—	2.28	2.37	mA	
	• at 105 °C	—	2.38	2.48		
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					—
	• at 25 °C	—	6.1	6.34	mA	
	• at 105 °C	—	6.22	6.47		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					—
	• at 25 °C	—	3.14	3.23	mA	
	• at 105 °C	—	3.27	3.36		
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					—
		—	3.54	3.63	mA	
		—	3.67	3.76		

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C • at 105 °C					
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	500	750	µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	188	217	µA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	82	123	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	503	754	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	60	90	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	516	774	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	209	350	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	229	370	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	93	140	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V	—	31	81	µA	—

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C					
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	103	154	µA	—
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.4	1.94	mA	—
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.02	1.24	mA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	121	181	µA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	59	97	µA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	28	42	µA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V	—	1.53	2.03	mA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V	—	0.881	1.18	mA	—
I_{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	158 164 187 219	175.7 179.48 199.54 236.43	µA	—
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	2.2 3.9 13.9 28.4	2.71 6.63 18.25 36.59	µA	—
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below • at 50 °C	— —	2.2 3.8	2.674 6.44		—

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 85 °C	—	13.2	17.37	µA	
	• at 105 °C	—	27.8	35.54		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V				µA	—
	• at 25 °C and below	—	1.08	1.17		
	• at 50 °C	—	1.4	1.52		
	• at 85 °C	—	3.45	3.96		
	• at 105 °C	—	7.02	8.19		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V				µA	—
	• at 25 °C and below	—	1.47	1.56		
	• at 50 °C	—	1.82	1.94		
	• at 85 °C	—	3.93	4.44		
	• at 105 °C	—	7.6	8.77		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V				µA	—
	• at 25 °C and below	—	1.33	1.42		
	• at 50 °C	—	1.65	1.77		
	• at 85 °C	—	3.56	4.07		
	• at 105 °C	—	6.92	8.09		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V					—
	• at 25 °C and below	—	566	690		
	• at 50°C	—	788	839		
	• at 85°C	—	2270	2600	nA	
	• at 105 °C	—	4980	5820		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V					—
	• at 25 °C and below	—	969	1059		
	• at 50°C	—	1200	1251		
	• at 85°C	—	2740	3070	nA	
	• at 105 °C	—	5610	6450		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V					—
	• at 25 °C and below	—	826	916		
	• at 50°C	—	1040	1091		
	• at 85°C	—	2400	2730	nA	
	• at 105 °C	—	4910	5750		

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V					—
	• at 25 °C and below	—	265	373	nA	
	• at 50 °C	—	467	512.9		
	• at 85 °C	—	1920	2256		
	• at 105 °C	—	4540	5395		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					4
	• at 25 °C and below	—	77	350	nA	
	• at 50 °C	—	255	465.70		
	• at 85 °C	—	1640	1994		
	• at 105 °C	—	4080	4956		

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 11. KL03 WLCSP package power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 85 °C	—	5.59	5.81		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 85 °C	—	5.24	5.45		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 85 °C	—	6.13	6.38		

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.71 3.78	 3.86 3.93	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 2.47 2.55	 2.57 2.65	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.43 6.53	 6.69 6.79	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 5.71 5.79	 5.94 6.02	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.3 3.37	 3.43 3.50	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 2.28 2.35	 2.37 2.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.1 6.19	 6.34 6.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V	 — —	 3.14 3.24	 3.23 3.33	 mA	—

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C • at 85 °C					
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	— —	3.54 3.64	3.63 3.73	mA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	500	750	µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	188	217	µA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	82	123	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	503	754	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	60	90	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	516	774	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	209	350	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	229	370	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all					—

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	93	140	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	31	81	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	103	154	µA	—
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.4	1.94	mA	—
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.02	1.24	mA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	121	181	µA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	59	97	µA	—
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	28	42	µA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V	—	1.53	2.03	mA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V	—	0.881	1.18	mA	—
I_{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	158 164 187	175.7 179.48 199.54	µA	—
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below	— —	2.2 3.9	2.71 6.63		—

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 50 °C • at 85 °C	—	13.9	18.25	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C	 — — —	 2.2 3.8 13.2	 2.674 6.44 17.37	 µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	 — — —	 1.08 1.4 3.45	 1.17 1.52 3.96	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	 — — —	 1.47 1.82 3.93	 1.56 1.94 4.44	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C	 — — —	 1.33 1.65 3.56	 1.42 1.77 4.07	µA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	 — — —	 566 788 2270	 690 839 2600	 nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	 — — —	 969 1200 2740	 1059 1251 3070	 nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 85°C	 — — —	 826 1040 2400	 916 1091 2730	 nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	—	265	373		—

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C and below • at 50 °C • at 85 °C	— —	467 1920	512.9 2256	nA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	77 255 1640	350 465.70 1994	nA	4

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 12. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105[1]	
$I_{LIRC8MHz}$	8 MHz internal reference clock (LIRC) adder. Measured by entering STOP or VLPS mode with 8 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	68	68	68	68	68	68	µA
$I_{LIRC2MHz}$	2 MHz internal reference clock (LIRC) adder. Measured by entering STOP mode with the 2 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	27	27	27	27	27	27	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • VLPS • STOP	340 340 340 340	410 410 420 420	460 460 480 480	470 490 570 570	480 530 610 610	600 600 850 850	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA

Table continues on the next page...

Table 12. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105[1]	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	15	15	15	15	15	15	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	340	440	440	480	520	620	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. • LIRC8M (8 MHz internal reference clock) • LIRC2M (2 MHz internal reference clock)	 85 28	 85 28	 85 28	 85 28	 85 28	 85 28	µA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. • LIRC8M (8 MHz internal reference clock) • LIRC2M (2 MHz internal reference clock)	 93 35	 93 35	 93 35	 93 35	 93 35	 93 35	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	340	340	340	340	340	340	µA

1. For QFN packages only.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

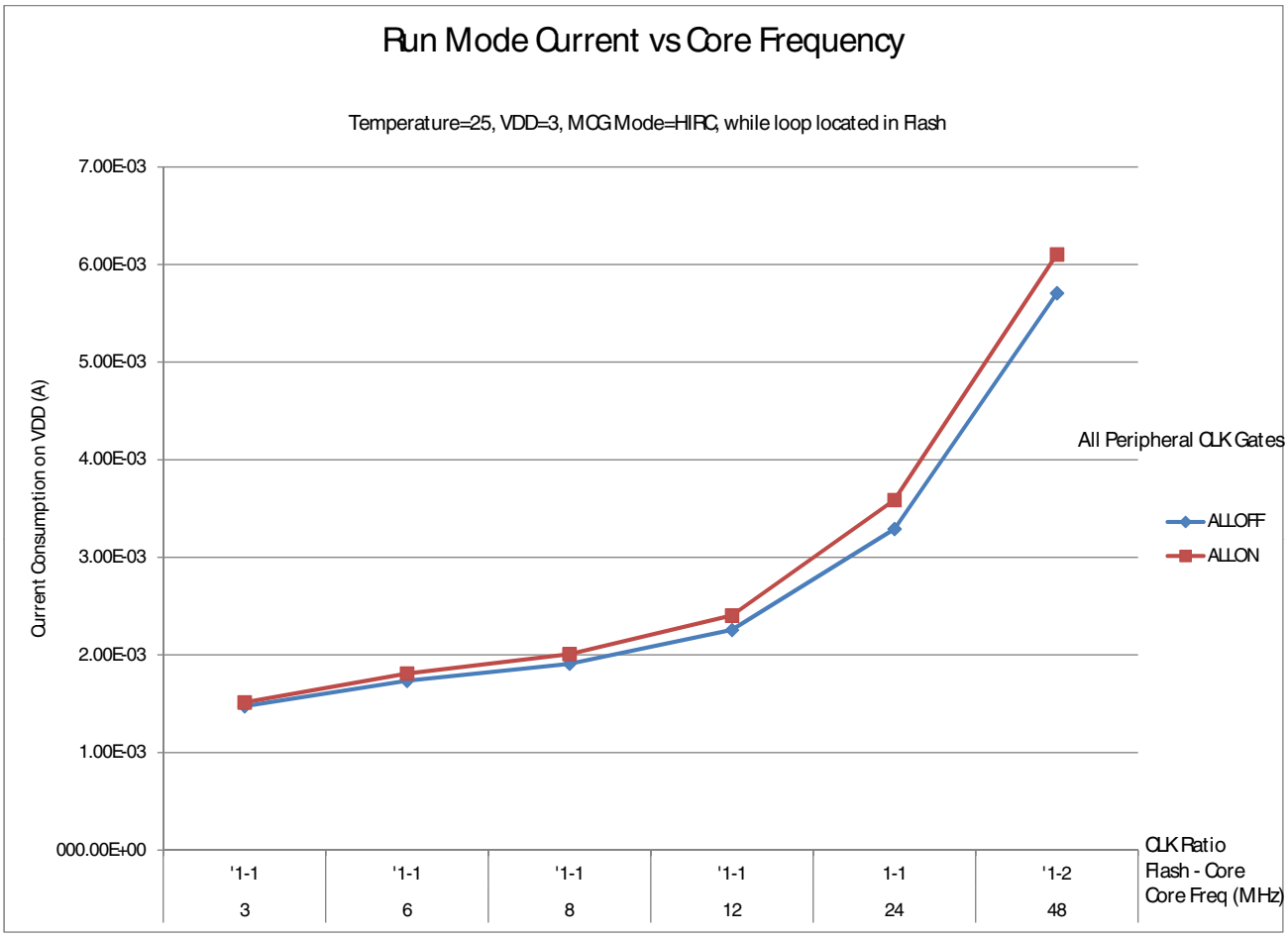


Figure 3. Run mode supply current vs. core frequency (loop located in flash)

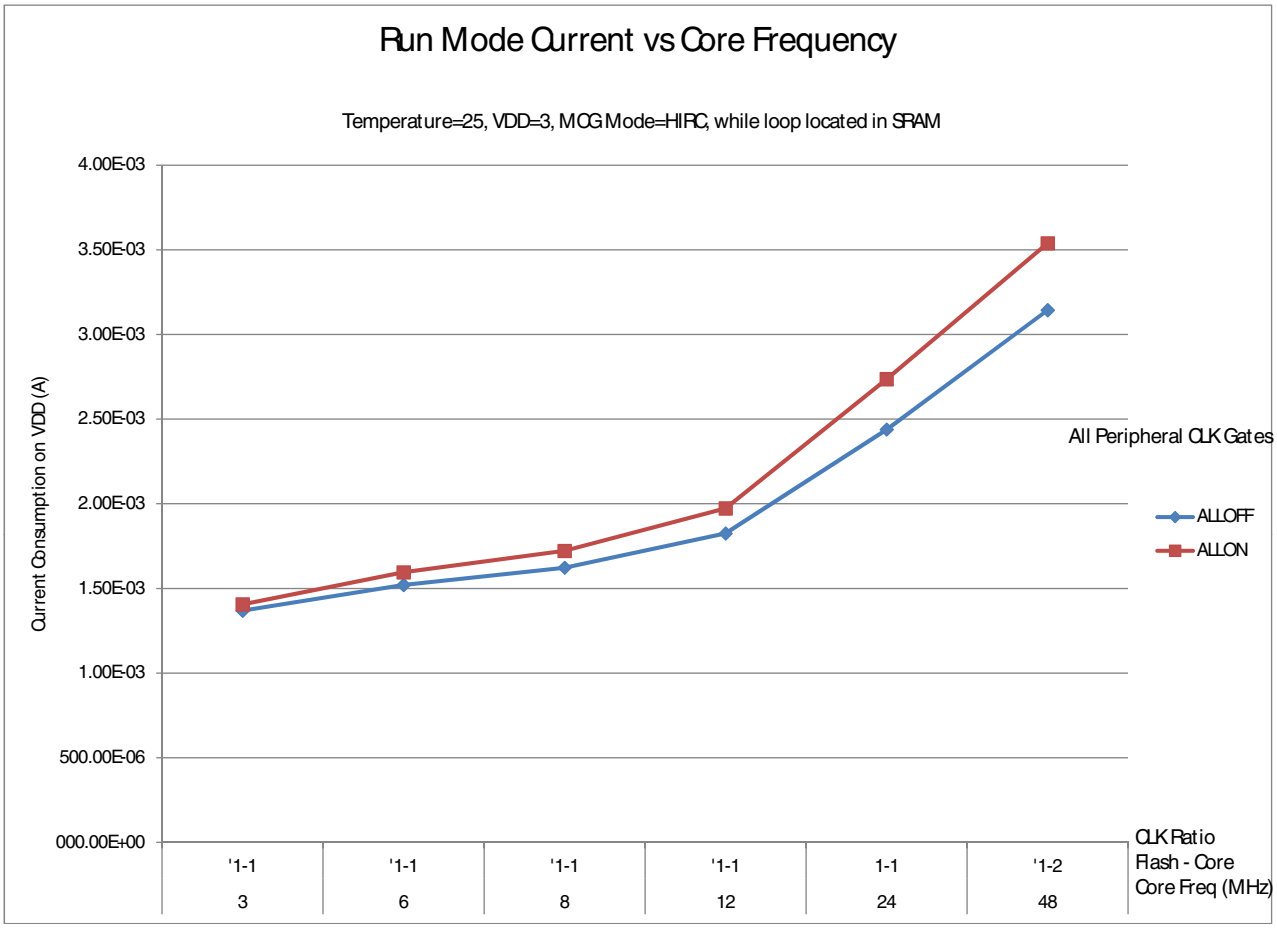


Figure 4. Run mode supply current vs. core frequency (loop located in SRAM)

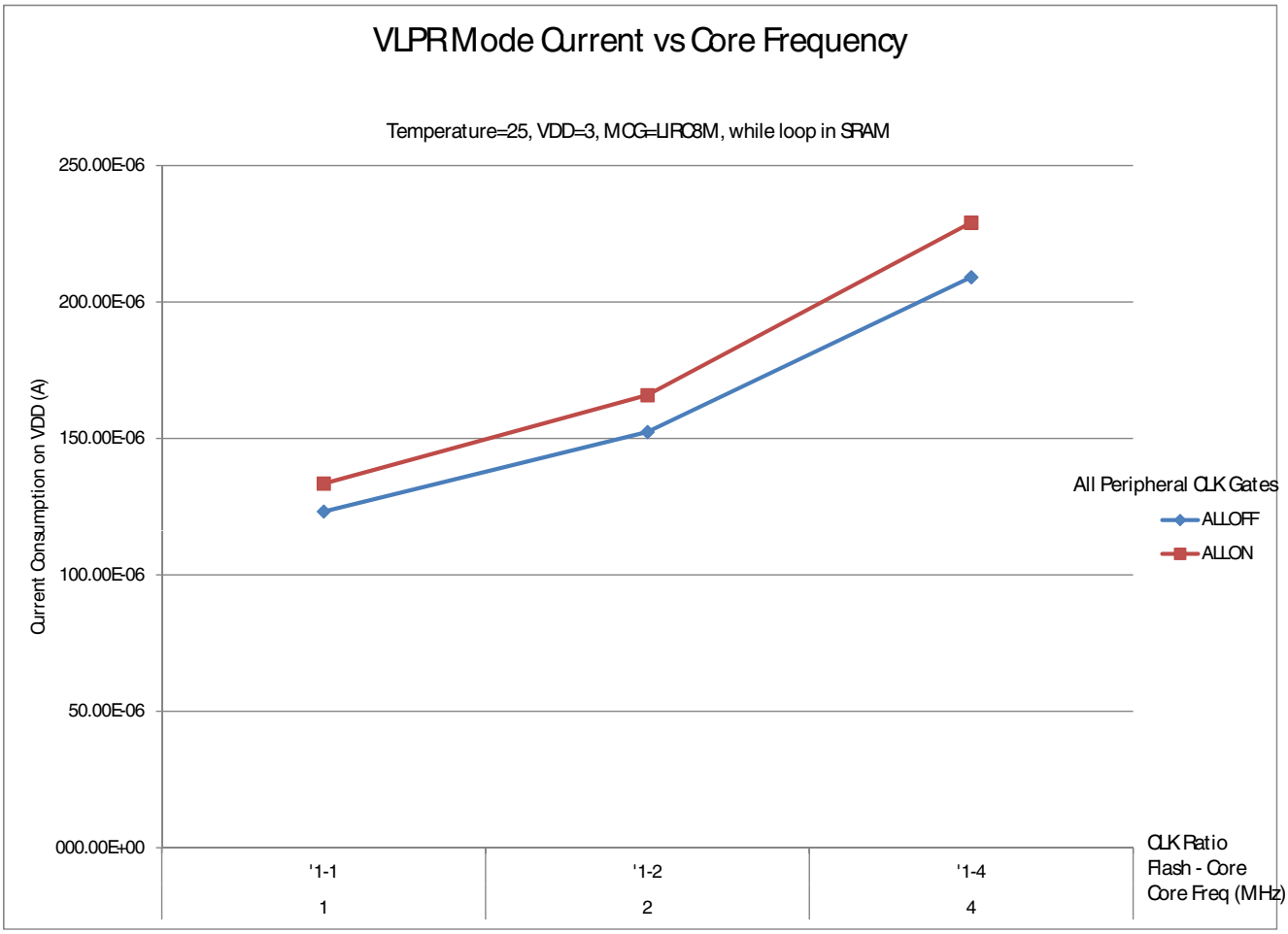


Figure 5. VLPR mode current vs. core frequency (loop in SRAM)

2.2.6 EMC radiated emissions operating behaviors

Table 13. EMC radiated emissions operating behaviors for 24-pin QFN package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	5	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	7	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	5	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC/SAE level	0.15–1000	N	—	2, 3

1. Determined according to IEC 61967-2 (and SAE J1752/3) radiated radio frequency (RF) emissions measurement standard. Typical Configuration: Appendix B: DUT Software Configuration—2. Typical Configuration.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{irc48m} = 48 MHz, f_{SYS} = 48 MHz, f_{BUS} = 24 MHz
3. IEC/SAE Level Maximums: N≤12 dBµV, M≤18 dBµV, L≤24 dBµV, K≤30 dBµV, I ≤ 36 dBµV, H ≤ 42 dBµV, G≤48 dBµV.

2.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design"

2.2.8 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 15. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{ERCLK}	External reference clock	—	32.768	kHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz