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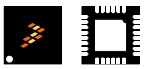
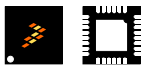
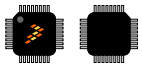
Kinetis KL04 32 KB Flash

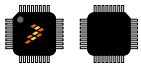
48 MHz Cortex-M0+ Based Microcontroller

MKL04ZxxVFK4
MKL04ZxxVLC4
MKL04ZxxVFM4
MKL04ZxxVLF4


24-pin QFN (FK)
4 x 4 x 1 Pitch 0.5 mm


32-pin QFN (FM)
5 x 5 x 1 Pitch 0.5 mm


32-pin LQFP (LC)
7 x 7 x 1.4 Pitch 0.8 mm


48-pin LQFP (LF)
7 x 7 x 1.4 Pitch 0.5 mm

Designed with efficiency in mind. Features a size efficient, small package, energy efficient ARM Cortex-M0+ 32-bit performance. Shares the comprehensive enablement and scalability of the Kinetis family.
This product offers:

- Run power consumption down to 45 µA/MHz in very low power run mode
- Static power consumption down to 2 µA with full state retention and 4 µs wakeup
- Ultra-efficient Cortex-M0+ processor running up to 48MHz with industry leading throughput
- Memory option is up to 32 KB Flash and 4 KB RAM
- Energy-saving architecture is optimized for low power with 90 nm TFS technology, clock and power gating techniques, and zero wait state flash memory controller

Performance

- 48 MHz ARM® Cortex®-M0+ core

Memories and memory interfaces

- Up to 32 KB program flash memory
- Up to 4 KB SRAM

System peripherals

- Nine low-power modes to provide power optimization based on application requirements
- COP Software watchdog
- 4-channel DMA controller, supporting up to 63 request sources
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

Clocks

- 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
- Multi-purpose clock source
- 1 kHz LPO clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Human-machine interface

- Up to 41 general-purpose input/output (GPIO)

Communication interfaces

- One 8-bit SPI module
- One low power UART module
- One I2C module

Analog Modules

- 12-bit SAR ADC
- Analog comparator (CMP) containing a 6-bit DAC and programmable reference input

Timers

- Six channel Timer/PWM (TPM)
- One 2-channel Timer/PWM module
- Periodic interrupt timers
- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL04Z8VFK4	8	1	22
MKL04Z16VFK4	16	2	22
MKL04Z32VFK4	32	4	22
MKL04Z8VLC4	8	1	28
MKL04Z16VLC4	16	2	28
MKL04Z32VLC4	32	4	28
MKL04Z8VFM4	8	1	28
MKL04Z16VFM4	16	2	28
MKL04Z32VFM4	32	4	28
MKL04Z16VLF4	16	2	41
MKL04Z32VLF4	32	4	41

Related Resources

Type	Description
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

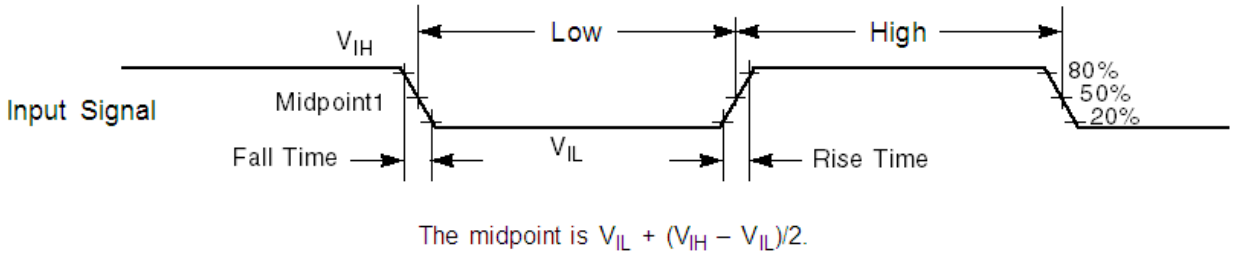


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	—
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	—
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	—
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	—
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	—
I_{ICIO}	IO pin negative DC injection current—single pin • V_{IN} < V_{SS}–0.3V (negative current injection) • V_{IN} < V_{SS}–0.3V (positive current injection)	 –3 —	 — +3	 mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 –25 —	 — +25	 mA	—
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	—

1. All IO pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{IO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{IO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V_{IO_MIN}-V_{IN})/|I_{ICIO}|. The positive injection current limiting resistor is calculated as R=(V_{IN}-V_{IO_MAX})/|I_{ICIO}|. Select the larger of these two calculated resistances.
2. Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except RESET_b)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	0.5	V	

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	 — —	 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	95	115	µs	
	• VLLS1 → RUN					

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	
		—	93	115	µs	
	• VLLS3 → RUN	—	42	53	µs	
	• LLS → RUN	—	4	4.6	µs	
	• VLPS → RUN	—	4	4.4	µs	
	• STOP → RUN	—	4	4.4	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	—	4.0	4.3	mA	3
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash • at 3.0 V	—	4.9	5.3	mA	3
I_{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash • at 3.0 V • at 25 °C • at 125 °C	— —	5.7 6.0	5.8 6.2	mA	3, 4
I_{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	2.7	2.9	mA	3

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	2.2	2.3	mA	3
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus / flash disabled (flash doze enabled) • at 3.0 V	—	1.5	1.7	mA	3
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash • at 3.0 V	—	182	253	µA	5
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash • at 3.0 V	—	213	284	µA	5
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash • at 3.0 V	—	243	313	µA	4, 5
I_{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	111	170	µA	5
I_{DD_STOP}	Stop mode current • at 3.0 V • at 25 °C • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 257 265 278 295 353	 277 285 303 326 412	µA	
I_{DD_VLPS}	Very-low-power stop mode current • at 3.0 V • at 25 °C • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 2.25 4.08 8.10 14.18 37.07	 5.76 8.27 14.52 23.78 58.58	µA	
I_{DD_LLS}	Low-leakage stop mode current • at 3.0 V					

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C	—	1.72	2.01	µA	
	• at 50 °C	—	2.52	3.18		
	• at 70 °C	—	4.32	5.94		
	• at 85 °C	—	7.18	10.00		
	• at 105 °C	—	18.67	25.65		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current • at 3.0 V				µA	
	• at 25 °C	—	1.16	1.36		
	• at 50 °C	—	1.78	2.27		
	• at 70 °C	—	3.23	4.38		
	• at 85 °C	—	5.57	7.53		
	• at 105 °C	—	14.80	19.74		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current • at 3.0 V				µA	
	• at 25°C	—	0.64	0.81		
	• at 50°C	—	1.14	1.50		
	• at 70°C	—	2.35	3.20		
	• at 85°C	—	4.37	5.80		
	• at 105°C	—	12.40	16.13		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) • at 3.0 V				µA	
	• at 25 °C	—	0.38	0.54		
	• at 50 °C	—	0.88	1.23		
	• at 70 °C	—	2.10	2.95		
	• at 85 °C	—	4.14	5.59		
	• at 105 °C	—	12.00	15.73		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) • at 3.0 V				µA	6
	• at 25 °C	—	0.30	0.45		
	• at 50 °C	—	0.79	1.12		
	• at 70 °C	—	2.01	2.82		
	• at 85 °C	—	4.05	5.45		
	• at 105 °C	—	11.96	15.63		

1. Data based on characterization results.

2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • LLS • VLPS • STOP	 440 440 490 510 510	 490 490 490 560 560	 540 540 540 560 560	 560 560 560 560 560	 570 570 570 610 610	 580 580 680 680 680	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. • MCGIRCLK (4 MHz internal reference clock) • OSCERCLK (4 MHz external crystal)	 66 214	 66 237	 66 246	 66 254	 66 260	 66 268	µA

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. • MCGIRCLK (4 MHz internal reference clock) • OSCERCLK (4 MHz external crystal)	86 235	86 256	86 265	86 274	86 280	86 287	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

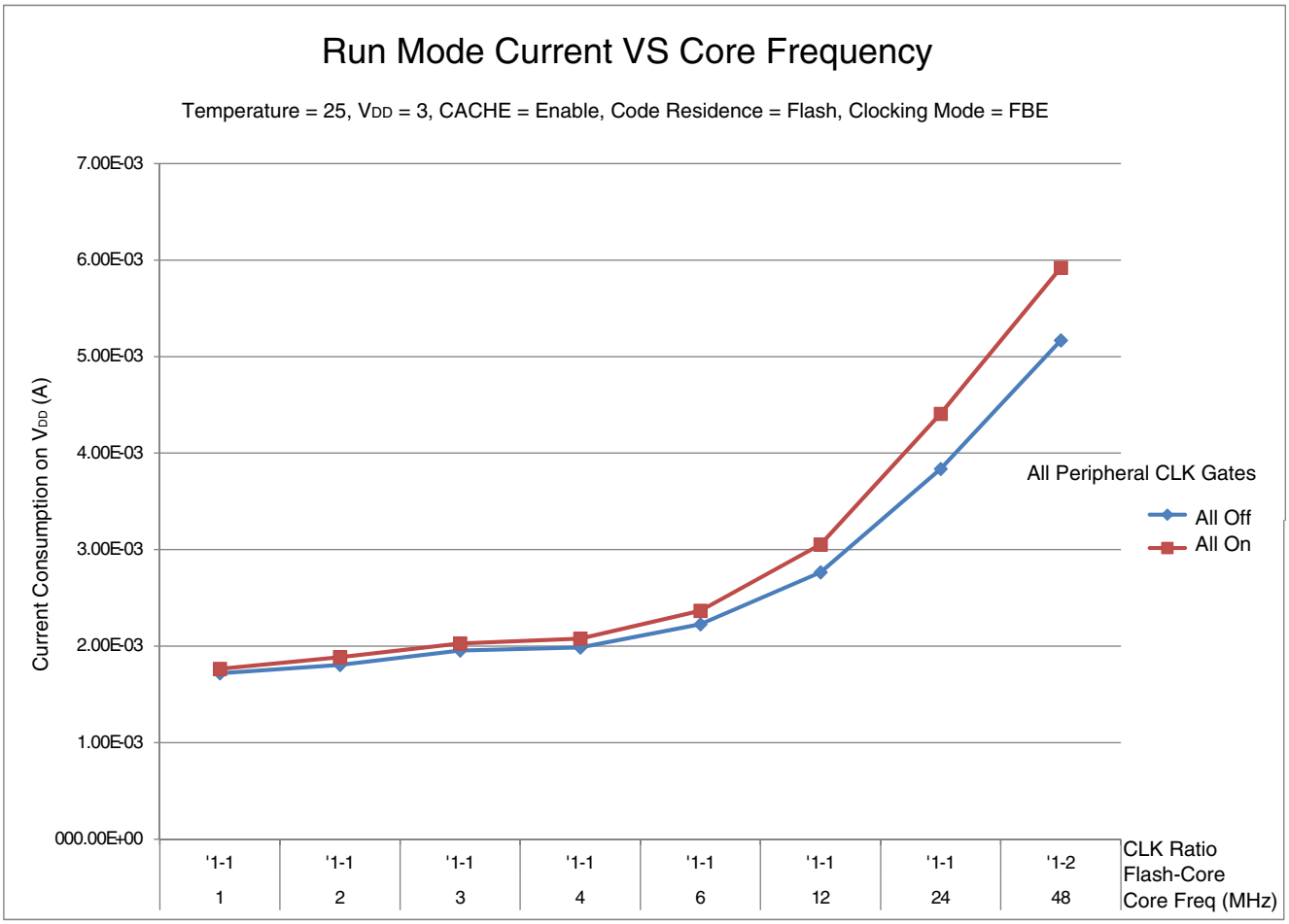


Figure 2. Run mode supply current vs. core frequency

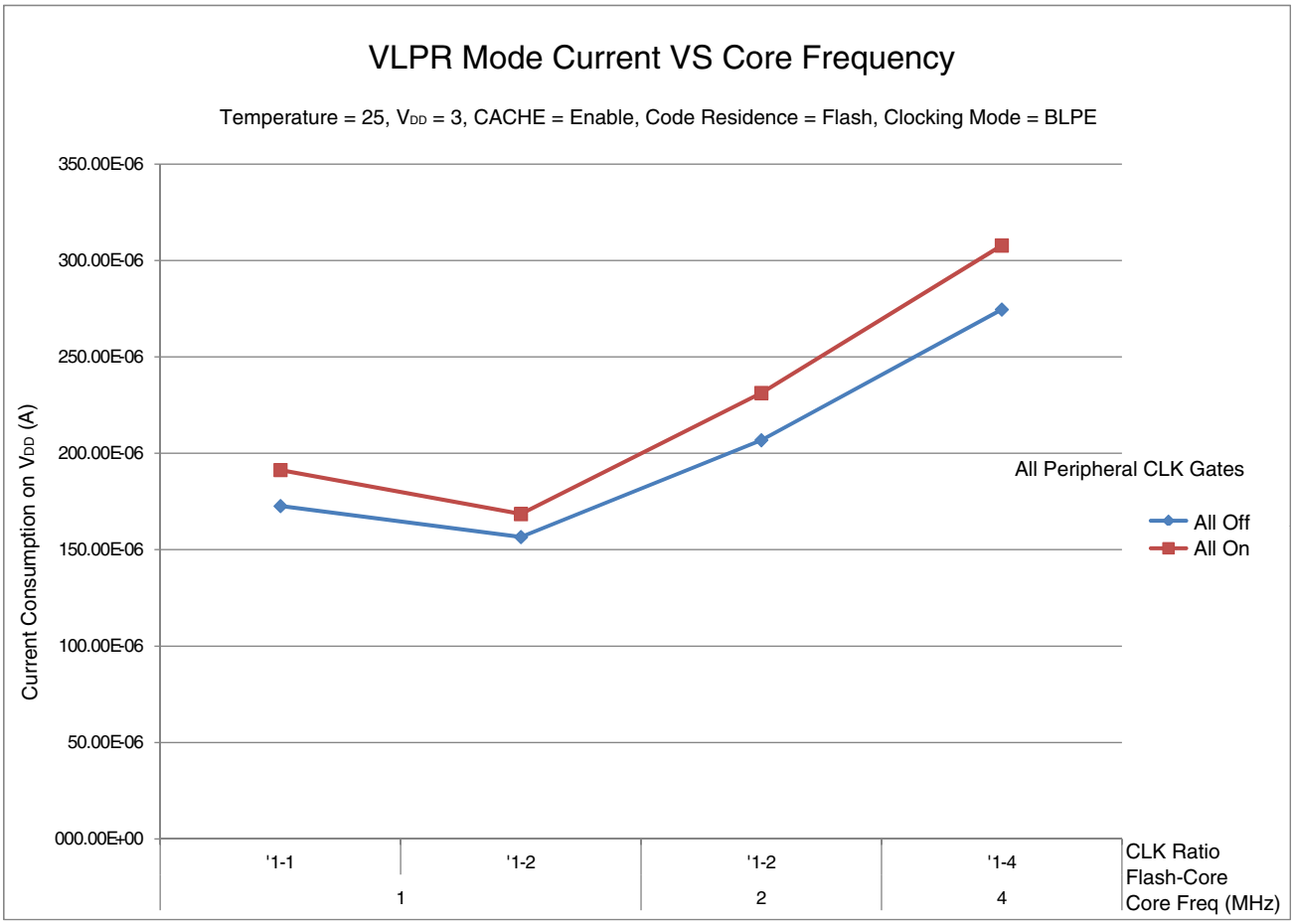


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

2.2.7 Capacitance attributes

Table 11. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 13. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 14. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

2.4.2 Thermal attributes

Table 15. Thermal attributes

Board type	Symbol	Description	48 LQFP	32 LQFP	32 QFN	24 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	82	88	97	110	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	58	59	34	42	°C/W	

Table continues on the next page...

Table 15. Thermal attributes (continued)

Board type	Symbol	Description	48 LQFP	32 LQFP	32 QFN	24 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	70	74	81	92	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	28	36	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	13	18	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	27	26	2.3	3.7	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	8	8	8	10	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 16. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width			

Table continues on the next page...

Table 16. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

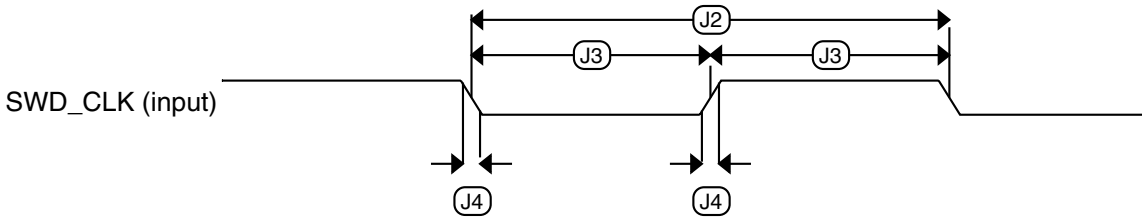


Figure 4. Serial wire clock input timing

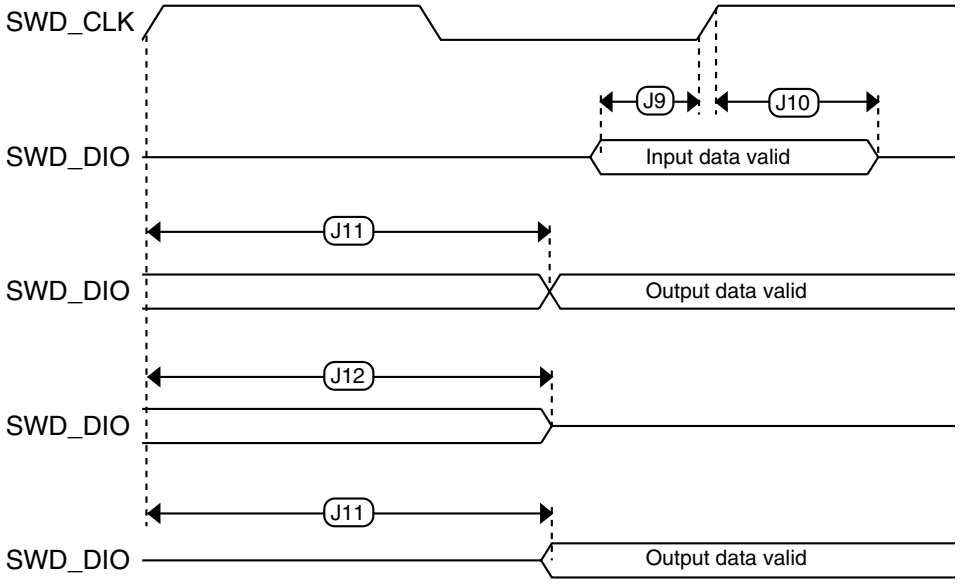


Figure 5. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 17. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 3	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency —		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) 1280 × f_{fll_ref}	40	41.94	48	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01)	—	47.97	—	MHz	

Table continues on the next page...

Table 17. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	1464 × f_{fll_ref}					
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz	—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 24 MHz • 32 MHz					
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.5	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	61	500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						

Table continues on the next page...

Table 23. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.6.1.1 12-bit ADC operating conditions

Table 24. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	

Table continues on the next page...