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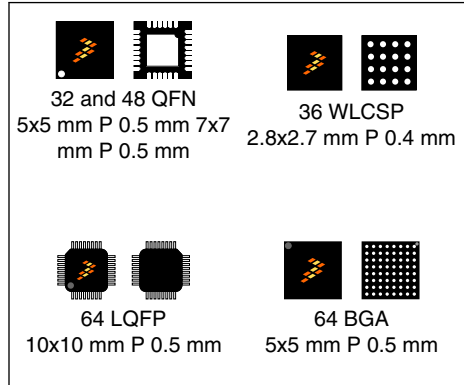
# Kinetis KL17 Microcontroller

48 MHz ARM® Cortex®-M0+ and 128/256 KB Flash

**MKL17Z128Vxx4**  
**MKL17Z256Vxx4**  
**MKL17Z256CAL4R**

The KL17 series is optimized for cost-sensitive and battery-powered applications requiring low-power general-purpose connectivity. The product offers:

- Embedded ROM with boot loader for flexible program upgrade
- High accuracy internal voltage and clock reference
- FlexIO to support any standard and customized serial peripheral emulation
- Down to 54uA/MHz in very low power run mode and 1.96uA in deep sleep mode (RAM + RTC retained)



## Core Processor

- ARM® Cortex®-M0+ core up to 48 MHz

## Memories

- 128/256 KB program flash memory
- 32 KB SRAM
- 16 KB ROM with build-in bootloader
- 32-byte backup register

## System

- 4-channel asynchronous DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin Serial Wire Debug (SWD) programming and debug interface
- Micro Trace Buffer
- Bit manipulation engine
- Interrupt controller

## Clocks

- 48MHz high accuracy (up to 0.5%) internal reference clock
- 8MHz/2MHz high accuracy (up to 3%) internal reference clock
- 1KHz reference clock active under all low-power modes (except VLLS0)
- 32–40KHz and 3–32MHz crystal oscillator

## Peripherals

- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules and I2C0 supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s
- One FlexIO module supporting emulation of additional UART, IrDA, SPI, I2C, I2S, PWM and other serial modules, etc.
- One serial audio interface I2S
- One 16-bit 818 ksp/s ADC module with high accuracy internal voltage reference (Vref) and up to 16 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC
- 1.2 V internal voltage reference

## Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock



### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 85 °C for WLCSP package and –40 to 105 °C for other packages

### Packages

- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness
- 36 WLCSP 2.8mm x 2.7mm, 0.4mm pitch, 0.6mm thickness

### Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security

### I/O

- Up to 54 general-purpose input/output pins (GPIO) and 6 high-drive pad

### Low Power

- Down to 54uA/MHz in very low power run mode
- Down to 1.96uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

### Ordering Information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD) <sup>1</sup>	ADC channels (SE/DP)
MKL17Z128VFM4	M17P7V	128	32	32	QFN	28	19/6	11/2
MKL17Z256VFM4	M17P8V	256	32	32	QFN	28	19/6	11/2
MKL17Z128VFT4	M17P7V	128	32	48	QFN	40	24/6	18/3
MKL17Z256VFT4	M17P8V	256	32	48	QFN	40	24/6	18/3
MKL17Z128VLH4	MKL17Z128V//LH4	128	32	64	LQFP	54	31/6	20/4
MKL17Z256VLH4	MKL17Z256V//LH4	256	32	64	LQFP	54	31/6	20/4
MKL17Z128VMP4	M17P7V	128	32	64	MAPBGA	54	31/6	20/4
MKL17Z256VMP4	M17P8V	256	32	64	MAPBGA	54	31/6	20/4
MKL17Z256CAL4R	MKL17Z256CAL4	256	32	36	WLCSP	26	23/6	7/0

1. INT: interrupt pin numbers; HD: high drive pin numbers

### Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Solution Advisor</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL1XPB <sup>1</sup>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL17P64M48SF6RM <sup>1</sup>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_1N71K <sup>1</sup>

Table continues on the next page...

### Related Resources (continued)

Type	Description	Resource
Package drawing	Package dimensions are provided in package drawings.	64-LQFP: 98ASS23234W <sup>1</sup> 64-MAPBGA: 98ASA00420D <sup>1</sup> 32-QFN: 98ASA00615D <sup>1</sup> 48-QFN: 98ASA00616D <sup>1</sup> 36-WLCSP: 98ASA00949D <sup>1</sup>

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.



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# 1 Ratings

## 1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

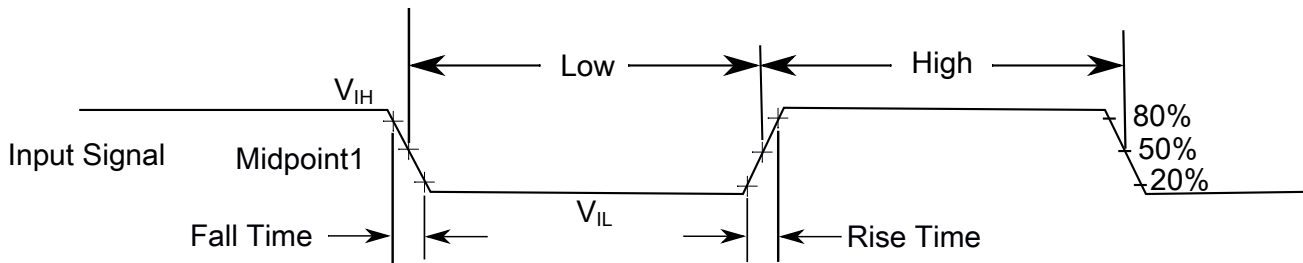
Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	120	mA
$V_{IO}$	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

### 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

**Table 5. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{ICIO}$	IO pin negative DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math></li> </ul>	-3	—	mA	1
$I_{ICcont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> </ul>	-25	—	mA	
$V_{ODPU}$	Open drain pullup voltage level	$V_{DD}$	$V_{DD}$	V	2
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	

- All I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{IO\_MIN}$  ( $= V_{SS}-0.3\text{ V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{ICIO}|$ .
- Open drain outputs must be pulled to  $V_{DD}$ .

## 2.2.2 LVD and POR operating requirements

**Table 6.  $V_{DD}$  supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling $V_{DD}$ POR detect voltage	0.8	1.1	1.5	V	—
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...



**Table 6.  $V_{DD}$  supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{LVW1H}$	<ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul>	2.62	2.70	2.78	V	
$V_{LVW2H}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul>	2.72	2.80	2.88	V	
$V_{LVW3H}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul>	2.82	2.90	2.98	V	
$V_{LVW4H}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul>	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
$V_{LVW1L}$	<ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul>	1.74	1.80	1.86	V	
$V_{LVW2L}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul>	1.84	1.90	1.96	V	
$V_{LVW3L}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul>	1.94	2.00	2.06	V	
$V_{LVW4L}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul>	2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
$V_{BG}$	Bandgap voltage reference	0.97	1.00	1.03	V	—
$t_{LPO}$	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — normal drive pad <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -1.5\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1
$V_{OH}$	Output high voltage — high drive pad <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -18\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -6\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OL}$	Output low voltage — normal drive pad <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 1.5\text{ mA}</math></li> </ul>	— —	0.5 0.5	V V	1
$V_{OL}$	Output low voltage — high drive pad	—	0.5	V	1

Table continues on the next page...

**Table 7. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 18\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 6\text{ mA}</math></li> </ul>	—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range	—	1	$\mu\text{A}$	2
$I_{IN}$	Input leakage current (per pin) at 25 °C	—	0.025	$\mu\text{A}$	2
$I_{IN}$	Input leakage current (total all pins) for full temperature range	—	64	$\mu\text{A}$	2
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	20	50	k $\Omega$	3

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD} = 3.6\text{ V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $VLLSx \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

**Table 8. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	$\mu\text{s}$	1
	• $VLLS0 \rightarrow \text{RUN}$	—	152	166	$\mu\text{s}$	
	• $VLLS1 \rightarrow \text{RUN}$	—	152	166	$\mu\text{s}$	
	• $VLLS3 \rightarrow \text{RUN}$	—	93	104	$\mu\text{s}$	
	• $LLS \rightarrow \text{RUN}$	—	7.5	8	$\mu\text{s}$	

Table continues on the next page...

**Table 8. Power mode transition operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLPS → RUN	—	7.5	8	μs	
	• STOP → RUN	—	7.5	8	μs	

1. Normal boot (FTFA\_FOFT[LPBOOT]=11)

## 2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

### NOTE

The while (1) test is executed with flash cache enabled.

### NOTE

The data at 105 °C are for QFN, LQFP and MAPBGA packages only.

**Table 9. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_RUNCO</sub>	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	— —	5.76 6.04	6.40 6.68	mA	2
I <sub>DD_RUNCO</sub>	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	— —	3.21 3.49	3.85 4.13	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	— —	6.45 6.75	7.09 7.39	mA	2
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V					2

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	3.95	4.59	mA	
		—	4.23	4.87		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.68	3.32	mA	2
		—	2.96	3.60		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	8.08	8.72	mA	2
		—	8.39	9.03		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	3.90	4.54	mA	
		—	4.21	4.85		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.66	3.30	mA	
		—	2.94	3.58		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.03	2.67	mA	
		—	2.31	2.95		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	5.52	6.16	mA	
		—	5.83	6.47		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	5.29	5.93	mA	
		—	5.56	6.20		
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V	—	6.91	7.55	mA	
		—	7.19	7.91		

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>					
I <sub>DD_VLPRCO</sub>	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	826	907	μA	
I <sub>DD_VLPRCO</sub>	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	405	486	μA	
I <sub>DD_VLPRCO</sub>	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	154	235	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	108	189	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	39	120	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	249	330	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	337	418	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	416	497	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	494	575	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	166	247	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock					

Table continues on the next page...



**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0\text{ V}$ • at 25 °C	—	50	131	$\mu\text{A}$	
$I_{DD\_VLPR}$	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0\text{ V}$ • at 25 °C	—	208	289	$\mu\text{A}$	
$I_{DD\_WAIT}$	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$	—	1.81	1.89	mA	
$I_{DD\_WAIT}$	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$	—	1.22	1.39	mA	
$I_{DD\_VLPW}$	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$	—	172	182	$\mu\text{A}$	
$I_{DD\_VLPW}$	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$	—	69	76	$\mu\text{A}$	
$I_{DD\_VLPW}$	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$	—	36	40	$\mu\text{A}$	
$I_{DD\_PSTOP2}$	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, $V_{DD} = 3.0\text{ V}$	—	1.81	2.06	mA	
$I_{DD\_PSTOP2}$	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD} = 3.0\text{ V}$	—	1.00	1.25	mA	
$I_{DD\_STOP}$	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	161.93 181.45 236.29 390.33	171.82 191.96 271.17 465.58	$\mu\text{A}$	
$I_{DD\_VLPS}$	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	3.31 10.43 34.14 104.38	5.14 17.68 61.06 164.44	$\mu\text{A}$	
$I_{DD\_VLPS}$	Very-low-power stop mode current at 1.8 V • at 25 °C and below	—	3.21	5.22		

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
	<ul style="list-style-type: none"> <li>• at 50 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	10.26	17.62	μA		
		—	33.49	60.19			
		—	102.92	162.20			
I <sub>DD_LLS</sub>	Low-leakage stop mode current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C and below</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	2.06	3.33	μA		
		—	4.72	6.85			
		—	8.13	13.30			
		—	13.34	24.70			
		—	41.08	52.43			
I <sub>DD_LLS</sub>	Low-leakage stop mode current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C and below</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	2.46	3.73	μA		
		—	5.12	7.25			
		—	8.53	11.78			
		—	13.74	18.91			
		—	41.48	52.83			
I <sub>DD_LLS</sub>	Low-leakage stop mode current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>• at 25 °C and below</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	2.35	2.70	μA	3	
		—	4.91	6.75			
		—	8.32	11.78			
		—	13.44	18.21			
		—	40.47	51.85			
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C and below</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	1.45	1.85	μA		
		—	3.37	4.39			
		—	5.76	8.48			
		—	9.72	14.30			
		—	30.41	37.50			
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C and below</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	2.05	2.45	μA	3	
		—	3.97	4.99			
		—	6.36	9.08			
		—	10.32	14.73			
		—	31.01	38.10			

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.96	2.36	μA	3
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	0.66	0.80	μA	
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.26	1.40	μA	3
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.16	1.30	μA	3
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	0.35	0.47	μA	
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					

**Table 9. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	0.18	0.28	μA	
		—	1.09	1.31		
		—	2.25	2.94		
		—	4.25	5.10		
		—	15.95	19.10		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG\_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

**Table 10. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IRC8MHz</sub>	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	93	93	93	93	93	93	μA
I <sub>IRC2MHz</sub>	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	29	29	29	29	29	29	μA
I <sub>EREFSTEN4MHz</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	μA
I <sub>EREFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> <li>VLLS1</li> <li>VLLS3</li> <li>LLS</li> <li>VLPS</li> <li>STOP</li> </ul>	440	490	540	560	570	580	nA
		440	490	540	560	570	580	
		490	490	540	560	570	680	
		510	560	560	560	610	680	
		510	560	560	560	610	680	
I <sub>LPTMR</sub>	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	

Table continues on the next page...

**Table 10. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
								nA
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul>	114	114	114	114	114	114	μA
		34	34	34	34	34	34	
I <sub>TPM</sub>	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul>	147	147	147	147	147	147	μA
		42	42	42	42	42	42	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	μA
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	330	330	330	330	330	330	μA

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



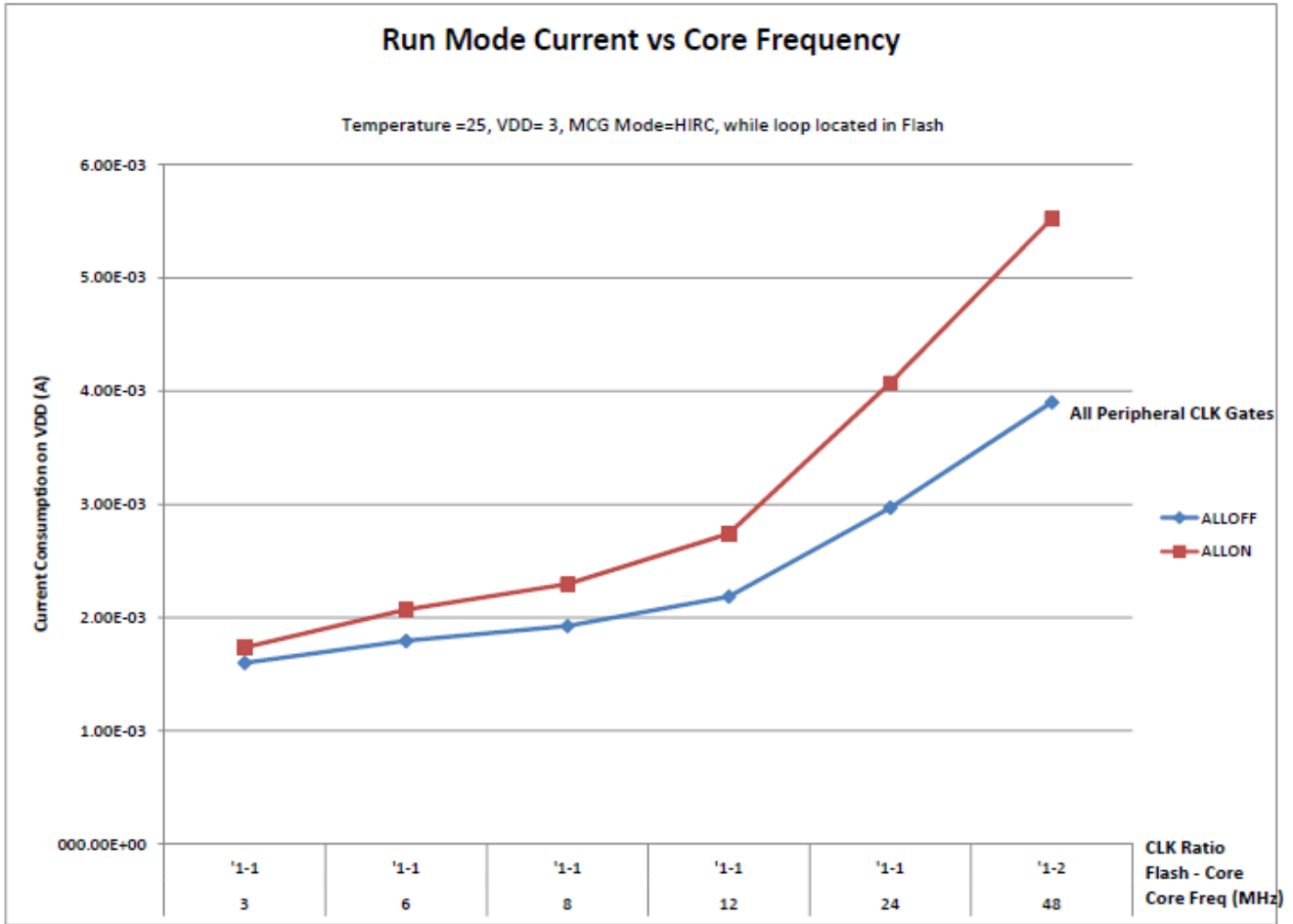
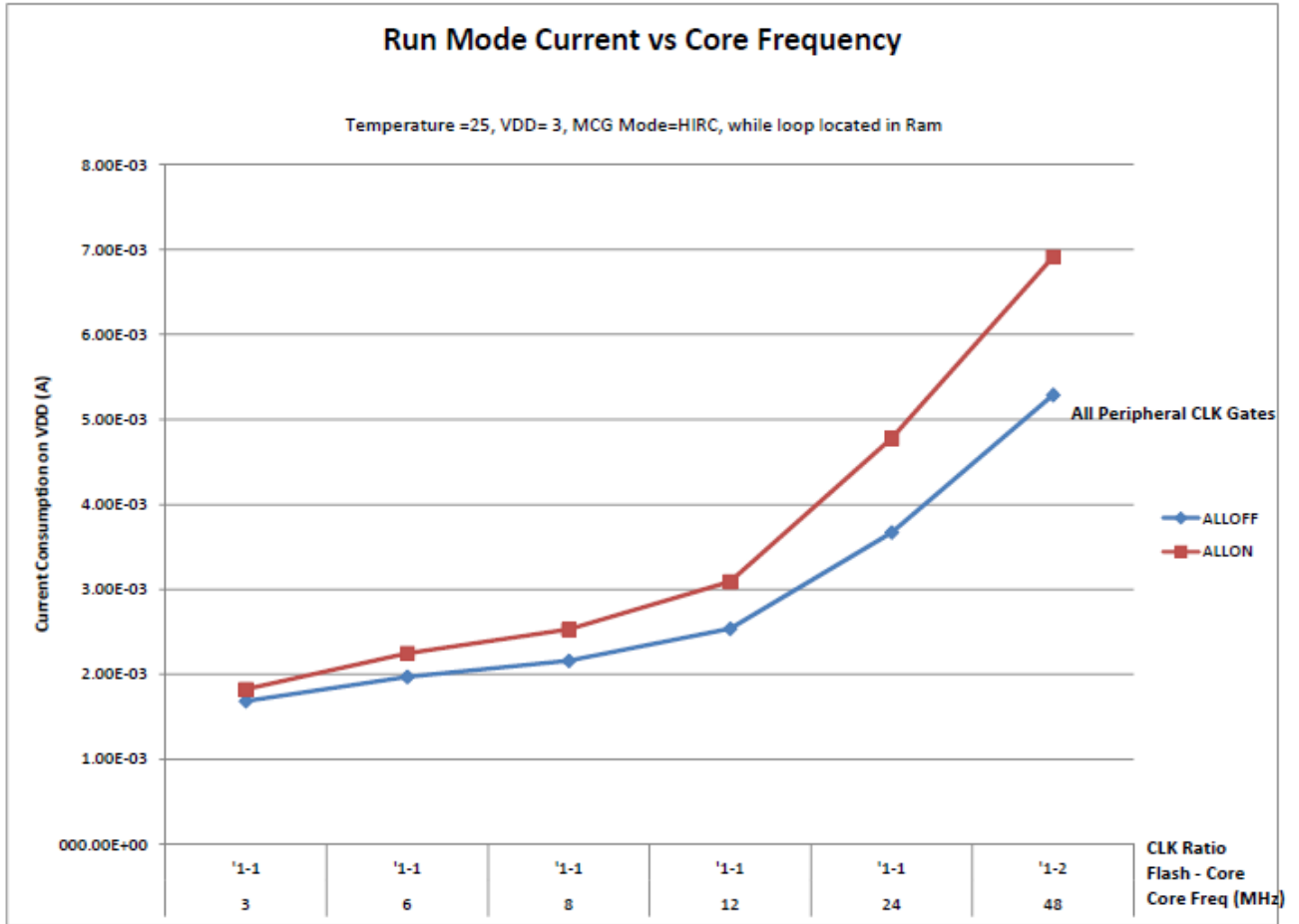


Figure 2. Run mode supply current vs. core frequency



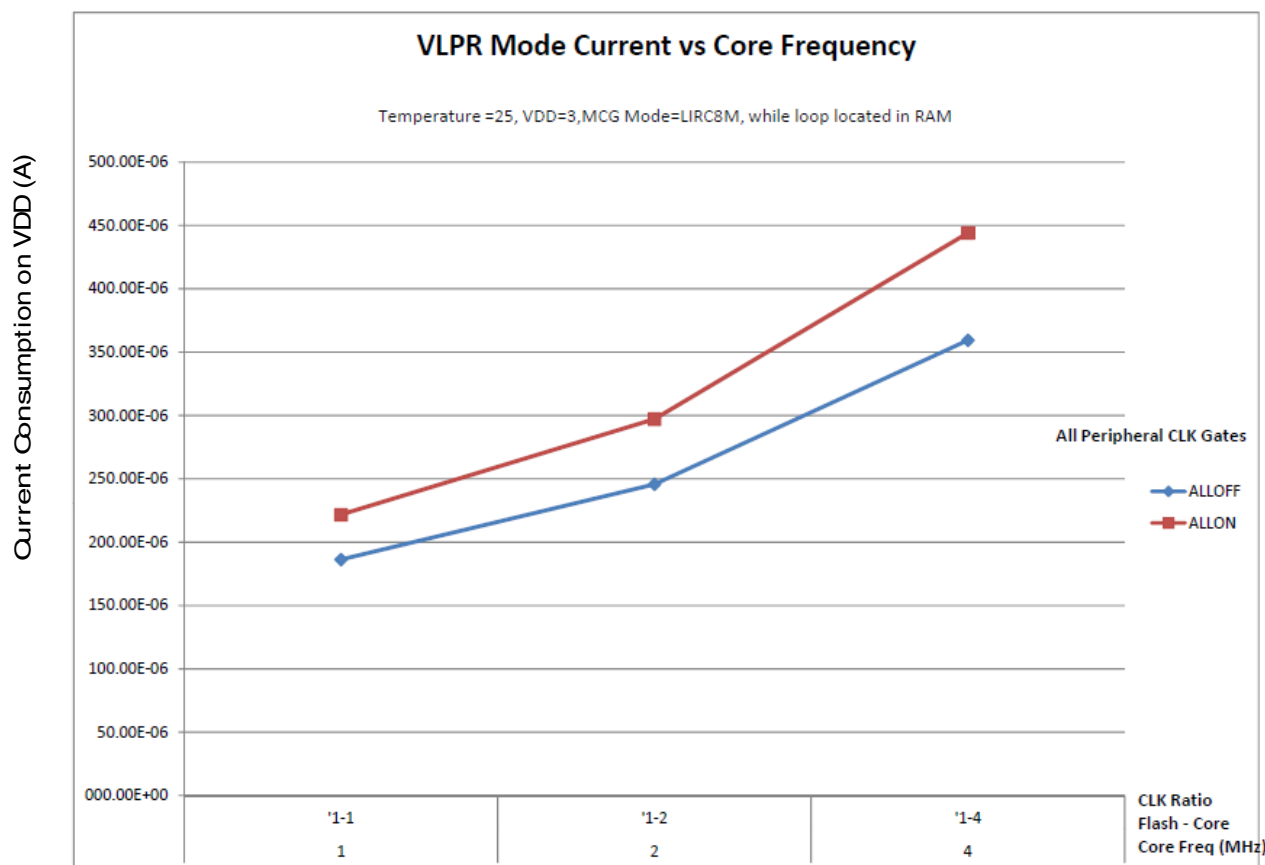


Figure 3. VLPR mode current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	11	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	12	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	10	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	6	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement*

of *Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ ,  $f_{OSC} = 1\text{ IRC48M}$ ,  $f_{SYS} = 48\text{ MHz}$ ,  $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN}$	Input capacitance	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
$f_{SYS}$	System and core clock <sup>1</sup>	—	48	MHz
$f_{BUS}$	Bus clock <sup>1</sup>	—	24	MHz
$f_{FLASH}$	Flash clock <sup>1</sup>	—	24	MHz
$f_{LPTMR}$	LPTMR clock	—	24	MHz
VLPR and VLPS modes <sup>2</sup>				
$f_{SYS}$	System and core clock	—	4	MHz
$f_{BUS}$	Bus clock	—	1	MHz
$f_{FLASH}$	Flash clock	—	1	MHz
$f_{LPTMR}$	LPTMR clock <sup>3</sup>	—	24	MHz

Table continues on the next page...

**Table 13. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f <sub>TPM</sub>	TPM asynchronous clock	—	8	MHz
f <sub>LPUART0/1</sub>	LPUART0/1 asynchronous clock	—	8	MHz

1. The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48MHz is used as the clock source.
2. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
3. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

## 2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 14. General switching specifications**

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 15. Thermal operating requirements for WLCSP package**

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>J</sub>	Die junction temperature	−40	95	°C	
T <sub>A</sub>	Ambient temperature	−40	85	°C	1



- Maximum  $T_A$  can be exceeded only if the user ensures that  $T_J$  does not exceed the maximum. The simplest method to determine  $T_J$  is:  $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$ .

**Table 16. Thermal operating requirements for other packages**

Symbol	Description	Min.	Max.	Unit	Notes
$T_J$	Die junction temperature	-40	125	°C	
$T_A$	Ambient temperature	-40	105	°C	1

- Maximum  $T_A$  can be exceeded only if the user ensures that  $T_J$  does not exceed the maximum. The simplest method to determine  $T_J$  is:  $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$ .

## 2.4.2 Thermal attributes

**Table 17. Thermal attributes**

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPB GA	36 WLCS P	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	77.6	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	38.9	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	69.6	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	35.6	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	34.8	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	0.37	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	0.2	°C/W	4
—	$\Psi_{JB}$	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	-	°C/W	5

- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
- Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

## Peripheral operating requirements and behaviors

- Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
- Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

#### 3.1.1 SWD electricals

Table 18. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

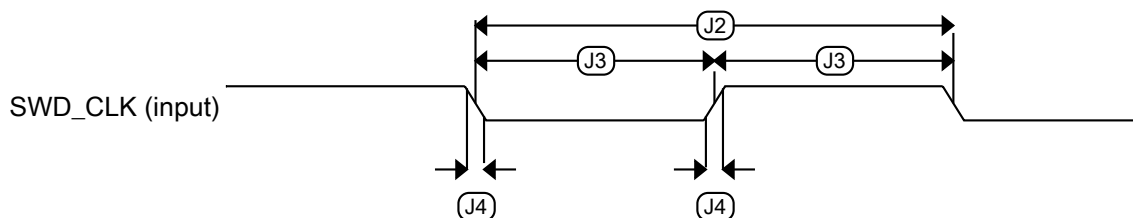


Figure 4. Serial wire clock input timing

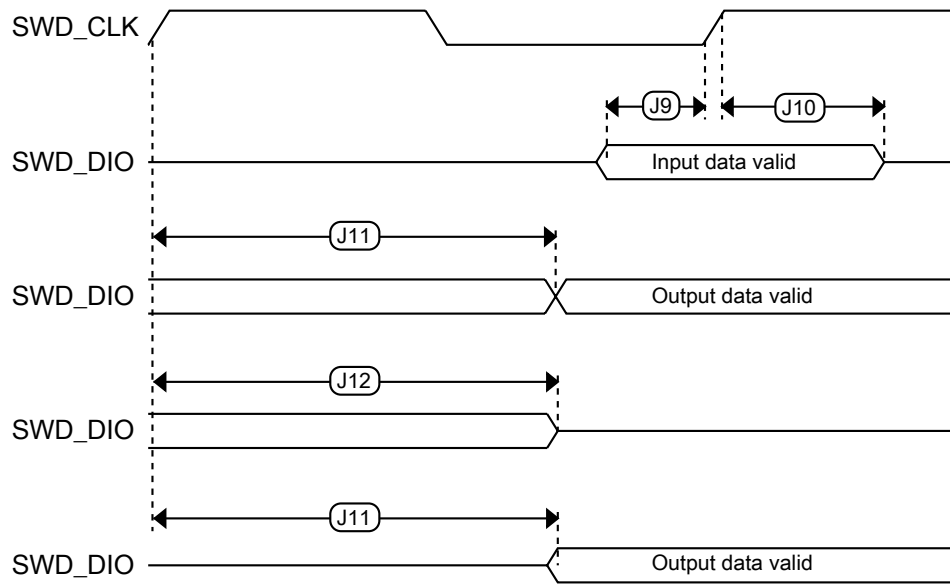


Figure 5. Serial wire data timing

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG-Lite specifications

Table 19. IRC48M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD}$	Supply current	—	400	500	$\mu A$	—
$f_{IRC}$	Output frequency	—	48	—	MHz	—
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature	—	$\pm 0.5$	$\pm 1.5$	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	$\pm 0.5$	$\pm 1.0$	$\%f_{irc48m}$	1

Table continues on the next page...