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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





KL24 Sub-Family Data Sheet

Supports the following:

MKL24Z32VFM4, MKL24Z64VFM4,
MKL24Z32VFT4, MKL24Z64VFT4,
MKL24Z32VLH4, MKL24Z64VLH4,
MKL24Z32VLK4, MKL24Z64VLK4

Features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 48 MHz ARM® Cortex-M0+ core
- Memories and memory interfaces
 - Up to 64 KB program flash memory
 - Up to 8 KB RAM
- Clocks
 - 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
 - Multi-purpose clock source
- System peripherals
 - Nine low-power modes to provide power optimization based on application requirements
 - 4-channel DMA controller, supporting up to 63 request sources
 - COP Software watchdog
 - Low-leakage wakeup unit
 - SWD interface and Micro Trace buffer
 - Bit Manipulation Engine (BME)
- Security and integrity modules
 - 80-bit unique identification (ID) number per chip
- Human-machine interface
 - General-purpose input/output
- Analog modules
 - 12-bit SAR ADC
 - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- Timers
 - Six channel Timer/PWM (TPM)
 - Two 2-channel Timer/PWM (TPM)
 - Periodic interrupt timers
 - 16-bit low-power timer (LPTMR)
 - Real-time clock
- Communication interfaces
 - USB full-/low-speed On-the-Go controller with on-chip transceiver and 5 V to 3.3 V regulator
 - Two 8-bit SPI modules
 - Two I2C modules
 - One low power UART module
 - Two UART modules

KL24P80M48SF0



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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PKL24 and MKL24

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification
KL##	Kinetis family	<ul style="list-style-type: none"> KL24
A	Key attribute	<ul style="list-style-type: none"> Z = Cortex-M0+
FFF	Program flash memory size	<ul style="list-style-type: none"> 32 = 32 KB 64 = 64 KB
R	Silicon revision	<ul style="list-style-type: none"> (Blank) = Main A = Revision after main
T	Temperature range (°C)	<ul style="list-style-type: none"> V = -40 to 105

Table continues on the next page...

Terminology and guidelines

Field	Description	Values
PP	Package identifier	<ul style="list-style-type: none">• FM = 32 QFN (5 mm x 5 mm)• FT = 48 QFN (7 mm x 7 mm)• LH = 64 LQFP (10 mm x 10 mm)• LK = 80 LQFP (12 mm x 12 mm)
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none">• 4 = 48 MHz
N	Packaging type	<ul style="list-style-type: none">• R = Tape and reel• (Blank) = Trays

2.4 Example

This is an example part number:

MKL24Z64VLK4

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

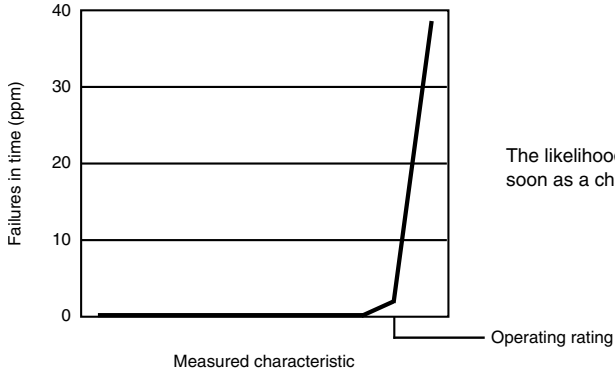
3.4.1 Example

This is an example of an operating rating:

Terminology and guidelines

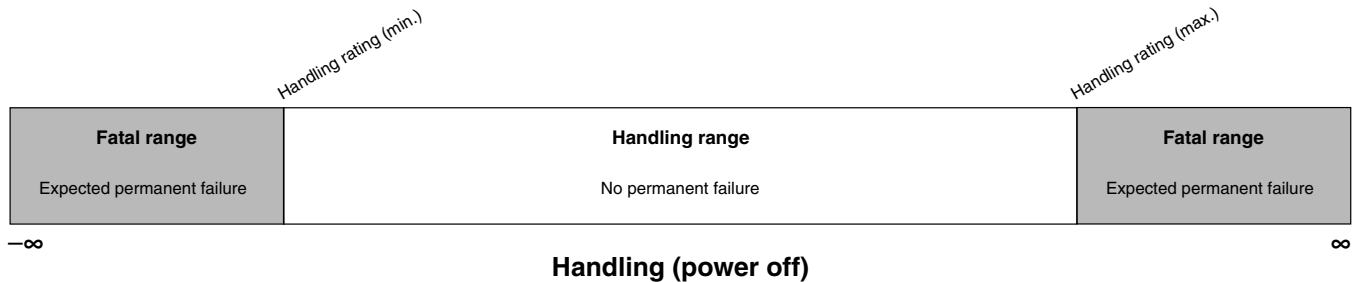
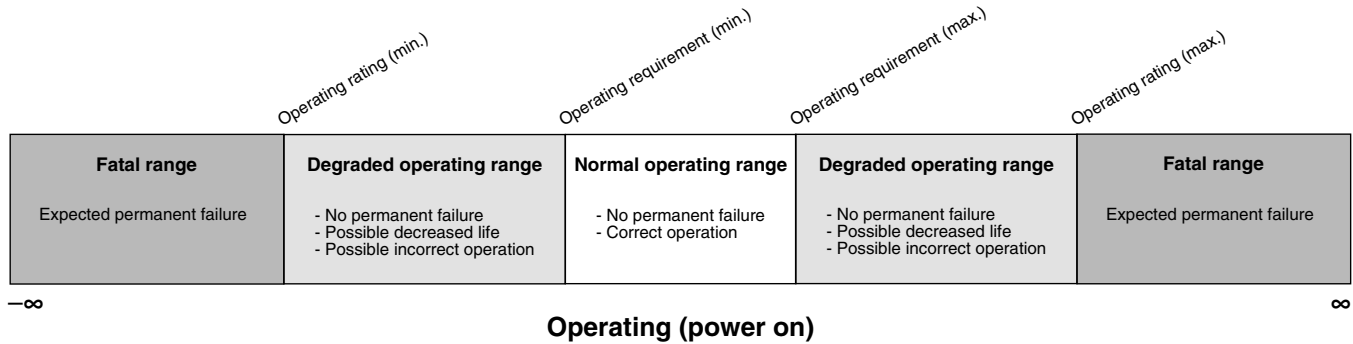
Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

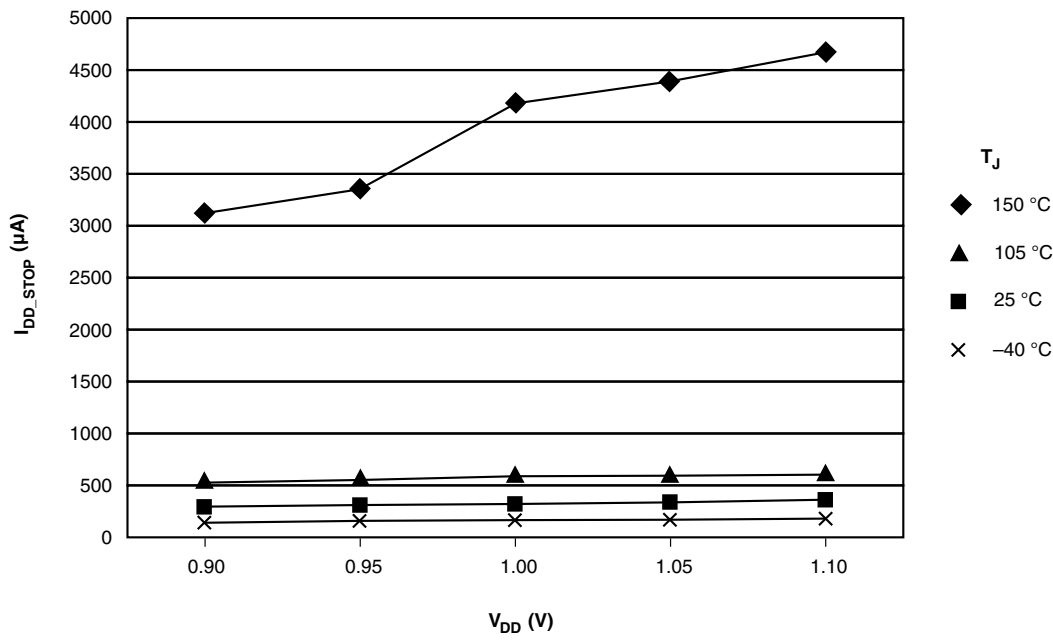
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

Ratings



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	120	mA
V _{DIO}	Digital pin input voltage (except $\overline{\text{RESET}}$)	-0.3	3.6	V
V _{AIO}	Analog pins ¹ and $\overline{\text{RESET}}$ pin input voltage	-0.3	V _{DD} + 0.3	V
I _D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} - 0.3	V _{DD} + 0.3	V
V _{USB_DP}	USB_DP input voltage	-0.3	3.63	V
V _{USB_DM}	USB_DM input voltage	-0.3	3.63	V
V _{REGIN}	USB regulator input	-0.3	6.0	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

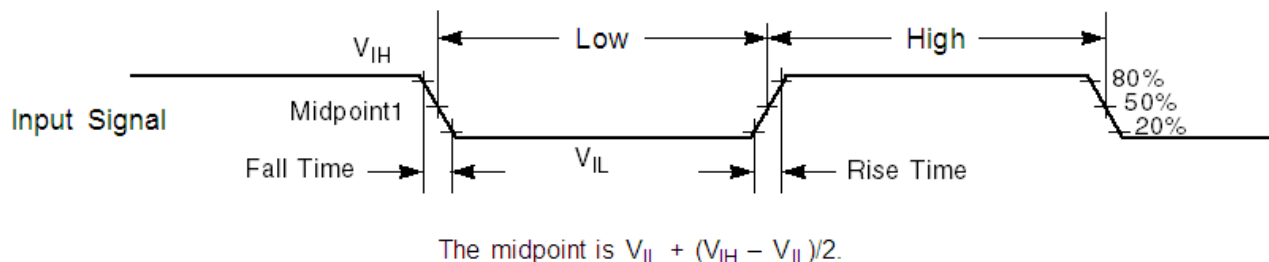


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assumes:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are slew rate disabled, and
 - are normal drive strength

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ 	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I _{CDIO}	Digital pin negative DC injection current — single pin • $V_{IN} < V_{SS}-0.3V$	-5	—	mA	1
I _{CAIO}	Analog ² pin DC injection current — single pin • $V_{IN} < V_{SS}-0.3V$ (Negative current injection) • $V_{IN} > V_{DD}+0.3V$ (Positive current injection)	-5 —	— +5	mA	3
I _{CCont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	-25 —	— +25	mA	
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	—	V	

- All digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{DIO_MIN} (=V_{SS}-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{IC}|$.
- Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{AIO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H}	Low-voltage warning thresholds — high range • Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	1
V _{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW1L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	1
V _{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -5 mA • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -1.5 mA	V _{DD} - 0.5 V _{DD} - 0.5	— —	V V	1
V _{OH}	Output high voltage — High drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -18 mA • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -6 mA	V _{DD} - 0.5 V _{DD} - 0.5	— —	V V	1
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 1.5 mA	— —	0.5 0.5	V V	1
V _{OL}	Output low voltage — High drive pad • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 18 mA • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 6 mA	— —	0.5 0.5	V V	1
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	2
I _{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	2
I _{IN}	Input leakage current (total all pins) for full temperature range	—	65	µA	2
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	

Table continues on the next page...

Table 3. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
R _{PU}	Internal pullup resistors	20	50	kΩ	3
R _{PD}	Internal pulldown resistors	20	50	kΩ	4

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD} = 3.6 V
3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	
	• VLLS0 → RUN	—	95	115	μs	
	• VLLS1 → RUN	—	93	115	μs	
	• VLLS3 → RUN	—	42	53	μs	
	• LLS → RUN	—	4	4.6	μs	
	• VLPS → RUN	—	4	4.4	μs	
	• STOP → RUN	—	4	4.4	μs	

5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO_CM}	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4MHz internal reference clock, CoreMark® benchmark code executing from flash <ul style="list-style-type: none"> at 3.0 V 	—	6.4	—	mA	2
I _{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> at 3.0 V 	—	4.1	5.2	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> at 3.0 V 	—	5.1	6.3	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> at 3.0 V at 25 °C at 125 °C 	— —	6.4 6.8	7.8 8.3	mA mA	3, 4,
I _{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> at 3.0 V 	—	3.7	5.0	mA	3
I _{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> at 3.0 V 	—	2.9	4.2	mA	3
I _{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus <ul style="list-style-type: none"> at 3.0 V 	—	2.5	3.7	mA	3
I _{DD_VLPRCO}	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> at 3.0 V 	—	188	570	μA	5
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> at 3.0 V 	—	224	613	μA	5

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash • at 3.0 V	—	300	745	μA	5, 4
I _{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	135	496	μA	5
I _{DD_STOP}	Stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	345 357 392 438 551	490 827 869 927 1065	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	4.4 10 20 37 81	16 35 50 112 201	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	1.9 3.6 6.5 13 30	3.7 39 43 49 69	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V at 25 °C at 50 °C at 70 °C at 85 °C at 105 °C	— — — — —	1.4 2.5 5.1 9.2 21	3.2 19 21 26 38	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0V at 25°C at 50°C at 70°C at 85°C at 105°C	— — — — —	0.7 1.3 2.3 5.1 13	1.4 13 14 17 25	μA	

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	—	381	943	nA	
	at 25 °C	—	956	11760		
	at 50 °C	—	2370	13260		
	at 70 °C	—	4800	15700		
	at 85 °C	—	12410	23480		
	at 105 °C	—				
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	—	176	860	nA	6
	at 25 °C	—	760	3577		
	at 50 °C	—	2120	11660		
	at 70 °C	—	4500	18450		
	at 85 °C	—	12130	22441		
	at 105 °C	—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using Keil 4.54 with optimization level 3, optimized for time.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{IREFSTEN4MHz}	External 4MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSCO_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
		440	490	540	560	570	580	
	VLLS1	490	490	540	560	570	680	
	VLLS3	510	560	560	560	610	680	
	LLS	510	560	560	560	610	680	
	VLPS							
	STOP							
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4MHz internal reference clock)	66	66	66	66	66	66	μA
	OSCERCLK (4MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							
	MCGIRCLK (4MHz internal reference clock)	86	86	86	86	86	86	μA
	OSCERCLK (4MHz external crystal)	235	256	265	274	280	287	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	μA

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

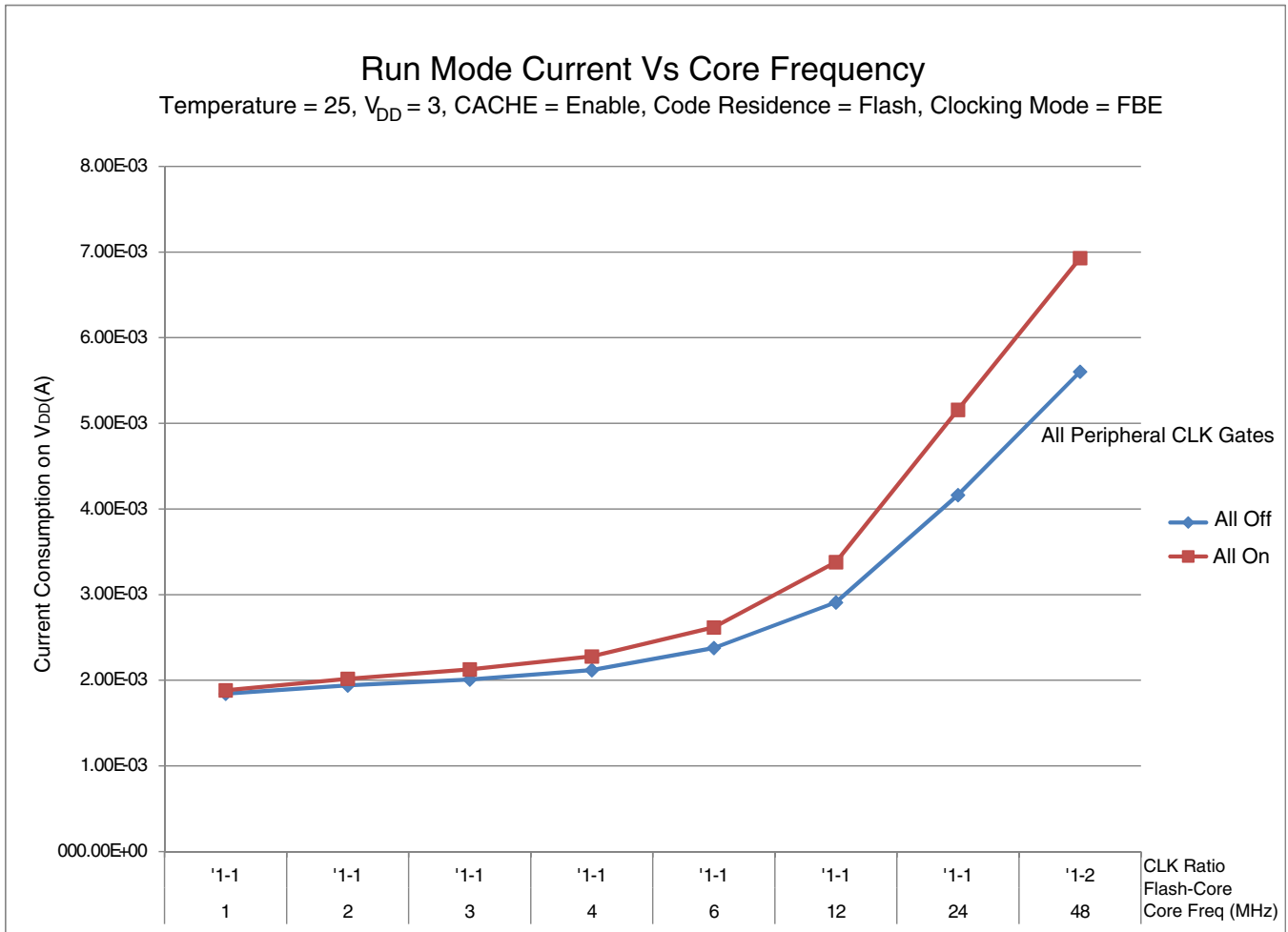


Figure 2. Run mode supply current vs. core frequency

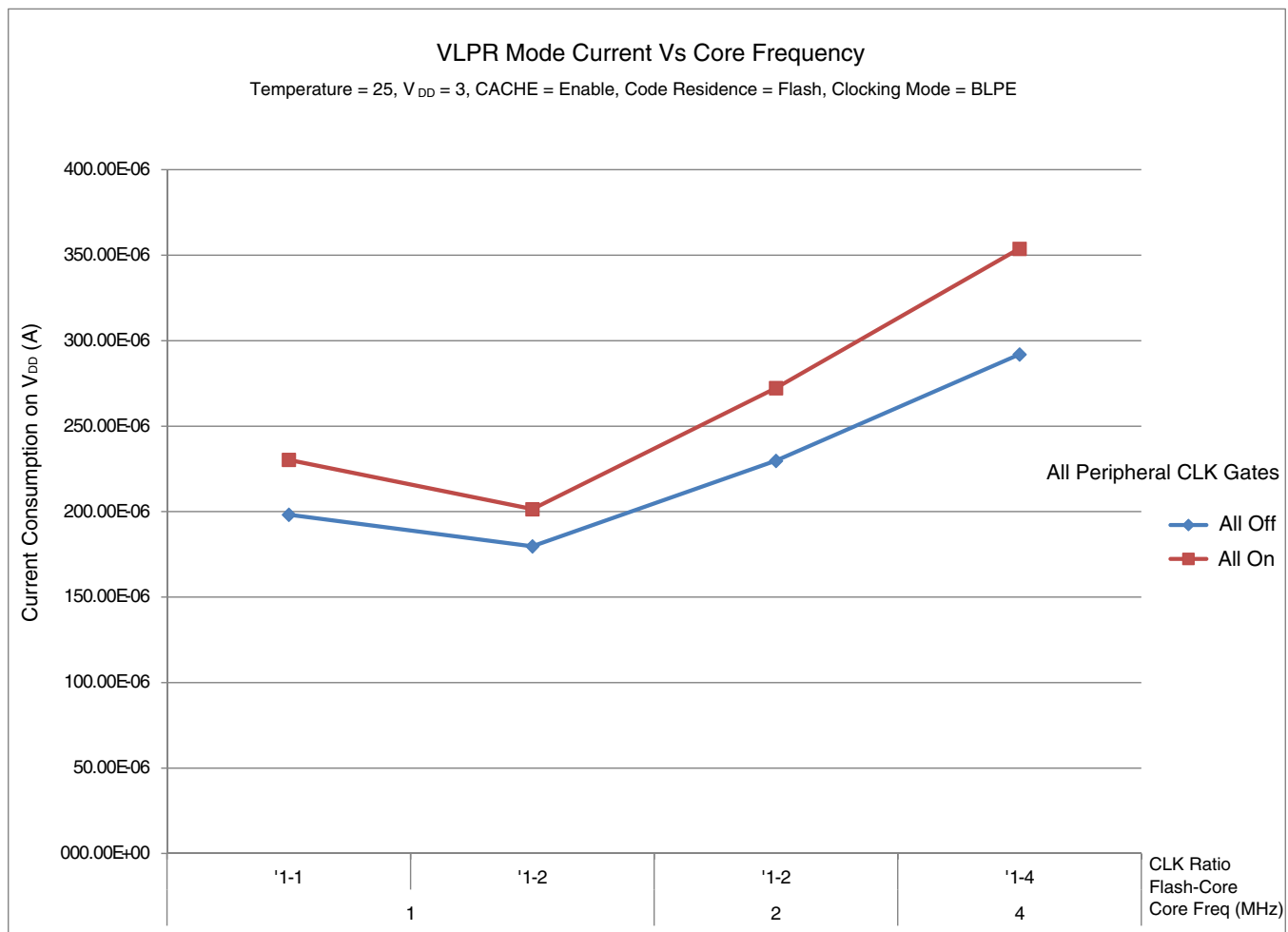


Figure 3. VLPR mode current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	13	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	15	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	12	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	7	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{OSC} = 8\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	48	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	24	MHz	

Table continues on the next page...

General

Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	
f _{TPM}	TPM asynchronous clock	—	8	MHz	
f _{UART0}	UART0 asynchronous clock	—	8	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I²C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	−40	125	°C
T _A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Table 10. Thermal attributes

Board type	Symbol	Description	80 LQFP	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	70	71	84	92	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	52	28	33	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	59	69	75	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	46	22	27	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	34	34	10	12	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	20	2.0	1.8	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.6	5	5.0	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD Electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 11. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> Serial wire debug 	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width <ul style="list-style-type: none"> Serial wire debug 	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

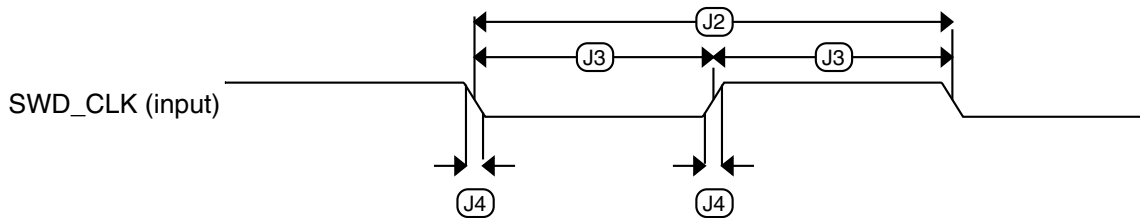


Figure 4. Serial wire clock input timing

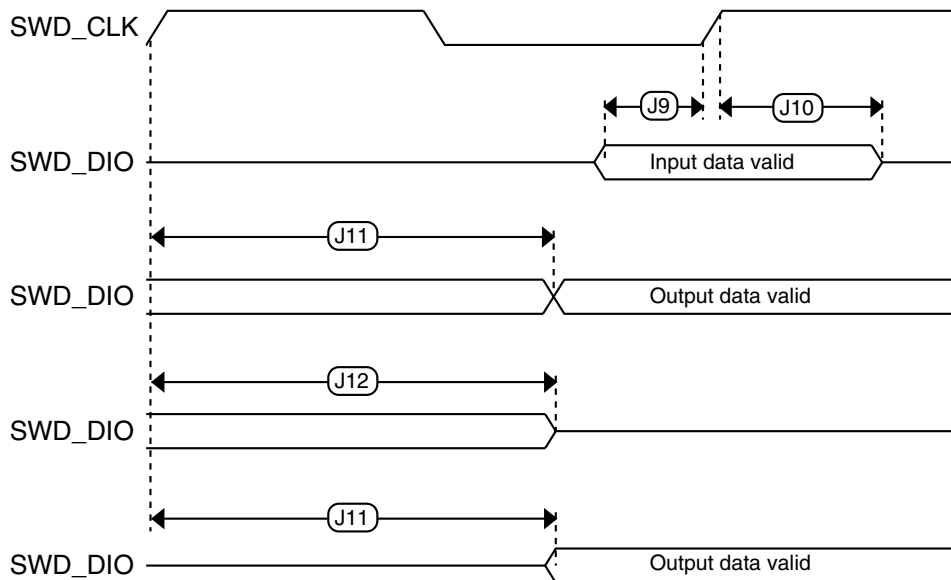


Figure 5. Serial wire data timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 12. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz		
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	% f_{dco}	1, 2	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	—	± 0.4	± 1.5	% f_{dco}	1, 2	
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C	—	4	—	MHz		
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage --- factory trimmed at nominal V_{DD} and 25 °C	—	+1/-2	± 3	% f_{intf_ft}	2	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C	3	—	5	MHz		
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints_t}$	—	—	kHz		
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints_t}$	—	—	kHz		
FLL							
f_{fill_ref}	FLL reference frequency range	31.25	—	39.0625	kHz		
f_{dco}	DCO output frequency range	Low range (DRS = 00) $640 \times f_{fill_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) $1280 \times f_{fill_ref}$	40	41.94	48	MHz	

Table continues on the next page...