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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

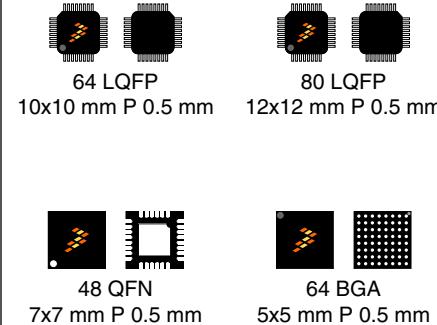
Kinetis KL33 Microcontroller

48 MHz ARM® Cortex®-M0+ and 64 KB Flash

The KL33 series is optimized for cost-sensitive and battery-powered applications requiring low-power segment LCD. The product offers:

- Low power segment LCD up to 40x8/42x6/44x4
- Embedded ROM with boot loader for flexible program upgrade
- High accuracy internal voltage and clock reference
- FlexIO to support any standard and customized serial peripheral emulation
- Hardware CRC module
- Down to 60 μ A/MHz in very low power run mode and 1.83 μ A in deep sleep mode (RAM + RTC retained)

MKL33Z32Vxx4
MKL33Z64Vxx4



Core Processor

- ARM® Cortex®-M0+ core up to 48 MHz

Memories

- 32/64 KB program flash memory
- 4/8 KB SRAM
- 8 KB ROM with build-in bootloader
- 32-byte backup register

System

- 4-channel asynchronous DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin Serial Wire Debug (SWD) programming and debug interface
- Micro Trace Buffer
- Bit manipulation engine
- Interrupt controller

Clocks

- 48 MHz high accuracy (up to 0.5%) internal reference clock
- 8MHz/2MHz high accuracy (up to 3%) internal reference clock
- 1KHz reference clock active under all low-power modes (except VLLS0)
- 32–40KHz and 3–32MHz crystal oscillator

Peripherals

- Segment LCD supporting up to 40x8/42x6/44x4 segments
- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules and I2C0 supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s
- One FlexIO module supporting emulation of additional UART, IrDA, SPI, I2C, PWM and other serial modules, etc.
- One 16-bit 818 ksp/s ADC module with high accuracy internal voltage reference (Vref) and up to 20 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC
- 1.2 V internal voltage reference

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: -40 to 105 °C

Packages

- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm thickness
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness (Package Your Way)
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness (Package Your Way)

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security
- Hardware CRC module

I/O

- Up to 70 general-purpose input/output pins (GPIO) and 4 high-drive pad

Low Power

- Down to 60uA/MHz in very low power run mode
- Down to 1.83uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

Ordering Information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/ Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD) ¹	ADC channels (SE/DP)
MKL33Z32VFT4	TBD	32	4	48	QFN	40	40/4	17/3
MKL33Z64VFT4	TBD	64	8	48	QFN	40	40/4	17/3
MKL33Z32VLH4	MKL33Z32/VLH4	32	4	64	LQFP	54	54/4	20/4
MKL33Z64VLH4	MKL33Z64/VLH4	64	8	64	LQFP	54	54/4	20/4
MKL33Z32VMP4	TBD	32	4	64	MAPBGA	54	54/4	20/4
MKL33Z64VMP4	TBD	64	8	64	MAPBGA	54	54/4	20/4
MKL33Z32VLK4	MKL33Z32VLK4	32	4	80	LQFP	70	70/4	20/4
MKL33Z64VLK4	MKL33Z64VLK4	64	8	80	LQFP	70	70/4	20/4

1. INT: interrupt pin numbers; HD: high drive pin numbers

NOTE

The 48 QFN and 64 MAPBGA packages supporting MKLx3ZxxVFT4 and MKLx3ZxxVMP4 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL3xPB¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL33P80M48SF3RM¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.

Table continues on the next page...

Related Resources (continued)

Type	Description	Resource
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_0N01P ¹
Package drawing	Package dimensions are provided in package drawings.	<ul style="list-style-type: none">• 64-LQFP: 98ASS23234W¹• 64 MAPBGA: 98ASA00420D¹• 48 QFN: 98ASA00616D¹• 80 LQFP: 98ASS23174W¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

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1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	-55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

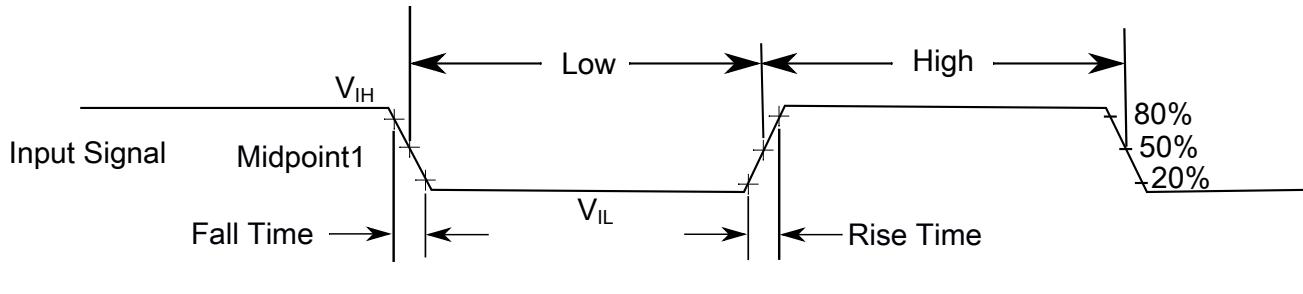


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30\text{ pF}$ loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage • $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ • $1.7 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage • $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ • $1.7 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • $V_{IN} < V_{SS} - 0.3 \text{ V}$	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{SRAM}	V_{DD} voltage required to retain SRAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS} - 0.3 \text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN}) / I_{ICIO}$.
2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V _{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V _{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V _{LVW1L}	Low-voltage warning thresholds — low range					1
V _{LVW2L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V _{LVW3L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V _{LVW4L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — normal drive pad				1
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -5 mA	V _{DD} - 0.5	—	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -1.5 mA	V _{DD} - 0.5	—	V	
V _{OH}	Output high voltage — high drive pad				1
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -18 mA	V _{DD} - 0.5	—	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -6 mA	V _{DD} - 0.5	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — normal drive pad				1
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 1.5 mA	—	0.5	V	
V _{OL}	Output low voltage — high drive pad				1

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$, $I_{OL} = 18 \text{ mA}$ $1.71 \text{ V} \leq V_{DD} \leq 2.7 \text{ V}$, $I_{OL} = 6 \text{ mA}$ 	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	2
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	μA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—	80	μA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	$\text{k}\Omega$	3

- PTB0, PTB1, PTC3, and PTD7 I/O have both high drive and normal drive capability selected by the associated PORTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
- Measured at $V_{DD} = 3.6 \text{ V}$
- Measured at V_{DD} supply voltage = V_{DD} min and $V_{IN} = V_{SS}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	<ul style="list-style-type: none"> $VLLS0 \rightarrow RUN$ 	—	152	166	μs	
	<ul style="list-style-type: none"> $VLLS1 \rightarrow RUN$ 	—	152	166	μs	
	<ul style="list-style-type: none"> $VLLS3 \rightarrow RUN$ 	—	93	104	μs	
	<ul style="list-style-type: none"> $LLS \rightarrow RUN$ 	—	7.5	8	μs	

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLPS → RUN	—	7.5	8	μs	
	• STOP → RUN	—	7.5	8	μs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	—	4.74	4.93	mA	2
I _{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	—	3.27	3.43	mA	
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	—	5.63	5.86	mA	2
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	—	3.47	3.61	mA	2,
		—	3.63	3.78	mA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	2.37	2.56	mA	2
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	6.91	7.19	mA	2
I _{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	4.14	4.31	mA	
I _{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	2.7	2.92	mA	
I _{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	1.99	2.15	mA	
I _{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C 	—	5.39	5.61	mA	
I _{DD_VLPRCO}	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C 	—	739	827.68	µA	
I _{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode—8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C 	—	339	406.8	µA	
I _{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C 	—	152	197.6	µA	
I _{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in flash all peripheral					

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	119	178.5	µA	
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	41	89.39	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	277	360.1	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	343	425.32	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	375	450	µA	
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	441	529.2	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	45	103.5	µA	
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	2.14	2.50	mA	
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	1.41	1.62	mA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0 \text{ V}$ • at 25 °C	—	193	239.023	µA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V _{DD} = 3.0 V • at 25 °C	—	78	124.8	µA	
I _{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V _{DD} = 3.0 V • at 25 °C	—	39	78	µA	
I _{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V _{DD} = 3.0 V • at 25 °C	—	1.72	2.06	mA	
I _{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V _{DD} = 3.0 V • at 25 °C	—	1.1	1.32	mA	
I _{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	161 171.9 206.8 255.9	178.2 181.17 229.72 302.01	µA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	2.20 4.57 18.02 39.60	3.80 8.03 31.98 65.80	µA	
I _{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	2.13 4.42 17.53 38.55	3.80 7.94 31.58 65.18	µA	
I _{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	— — — — —	1.63 2.42 4.22 7.16 15.34	2.25 3.55 7.08 10.22 22.69	µA	
I _{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V • at 25 °C and below	—	2.3	2.99	µA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	3.12	4.50		
		—	4.96	7.71		
		—	7.93	10.75		
		—	16.02	22.99		
I _{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	2.03	2.55	µA	³
		—	2.81	3.95		
		—	4.53	7.30		
		—	7.31	10.25		
		—	14.93	22.72		
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	1.16	1.65	µA	
		—	1.72	2.65		
		—	3.04	5.70		
		—	5.21	7.79		
		—	11.33	17.63		
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	1.83	2.35	µA	³
		—	2.43	3.39		
		—	3.78	5.95		
		—	5.98	8.14		
		—	12.02	17.89		
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	1.58	1.98	µA	³
		—	2.13	3.17		
		—	3.37	5.80		
		—	5.4	7.83		
		—	10.99	16.86		
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50°C • at 70°C 	—	0.62	1.06		
		—	0.99	1.43		
		—	1.88	2.65	µA	
		—	3.41	4.53		

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> • at 85°C • at 105 °C 	—	7.89	9.99		
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C 	—	1.31	1.52	μA	3
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C 	—	1.06	1.35	μA	3
I _{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	278	385	nA	
I _{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C 	—	95	218	nA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.20 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IRC8MHz}	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	85	87	88	88	89	90	µA
I _{IRC2MHz}	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	28	28	28	28	28	28	µA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	µA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of setting the OSC0_CR[EREFSTEN and EREFSTEN] bits to 1 and SIM_SOPT1[OSC32KSEL] to 01. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> • VLLS1 • VLLS3 • LLS • VLPS • STOP 	440 440 490 510 510	490 490 490 560 560	540 540 540 560 560	560 560 560 560 560	570 570 570 610 610	580 580 680 680 680	nA
I _{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	16	16	16	16	16	16	µA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	582	627	638	662	682	760	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.							

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	Includes selected clock source power consumption. <ul style="list-style-type: none">• IRC8M (8 MHz internal reference clock)• IRC2M (2 MHz internal reference clock)	105 34	110 34	110 34	111 34	112 34	114 34	µA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none">• IRC8M (8 MHz internal reference clock)• IRC2M (2 MHz internal reference clock)	130 40	130 40	130 40	130 40	130 40	130 40	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	320	320	320	320	320	320	µA
I_{LCD}	LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption.	4.9	4.9	4.9	4.9	4.9	4.9	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

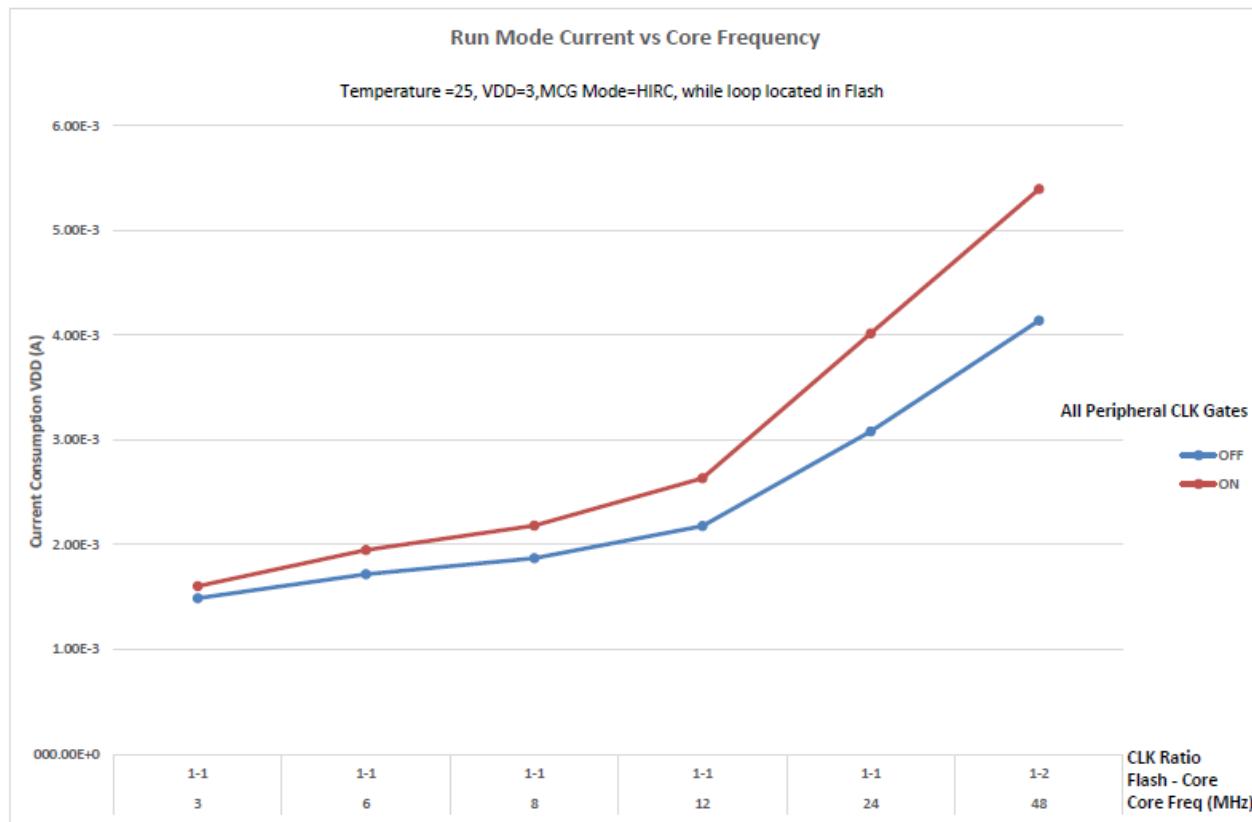


Figure 2. Run mode supply current vs. core frequency

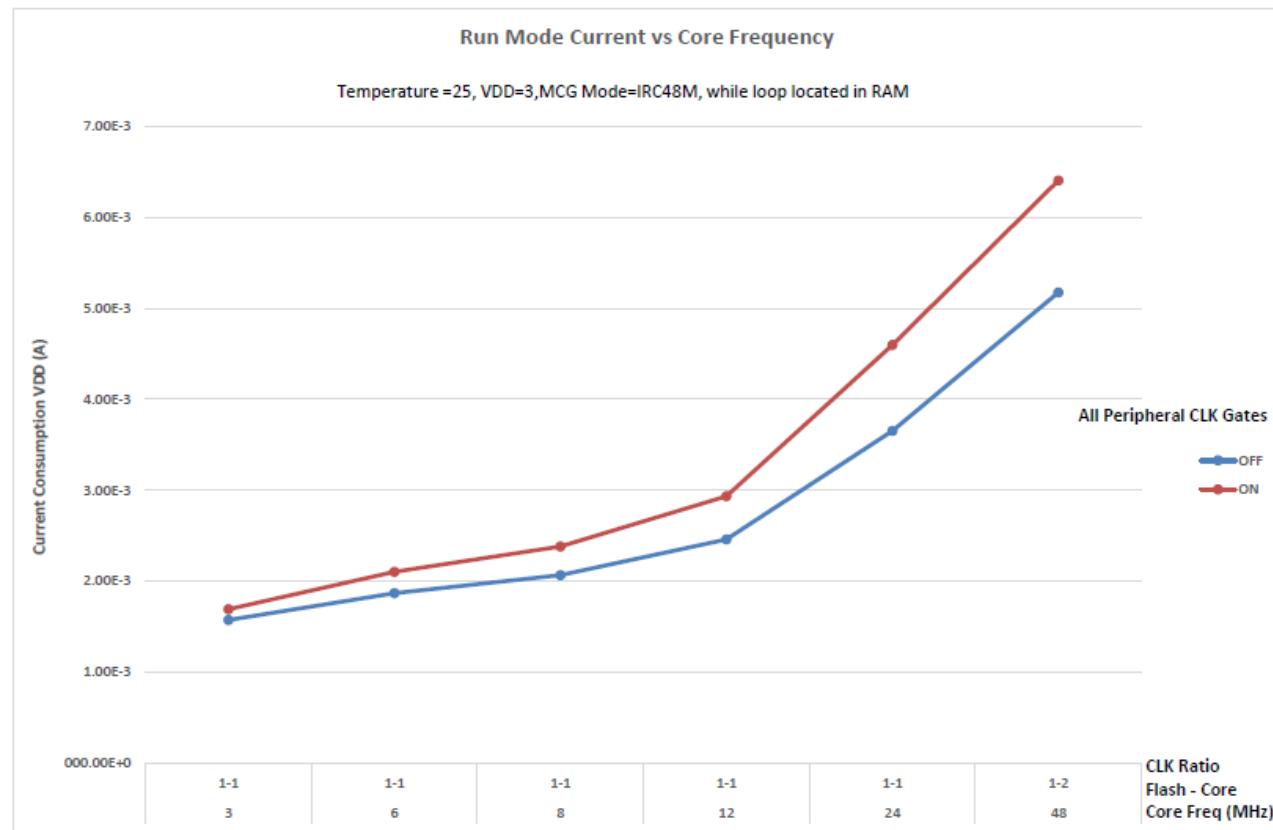




Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications

- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems
- KL-QRUG (Kinetis L-series Quick Reference).

2.2.7 Capacitance attributes

Table 11. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes ¹				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock ²	—	24	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
$f_{LPUART0/1}$	LPUART0/1 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 13. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 14. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _J	Die junction temperature	-40	125	°C	
T _A	Ambient temperature	-40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: T_J = T_A + θ_{JA} × chip power dissipation.

2.4.2 Thermal attributes

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Table 15. Thermal attributes

Board type	Symbol	Description	64 LQFP	80 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	58	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	43	°C/W	1, 2
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	60	47	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	37	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	26	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	15	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

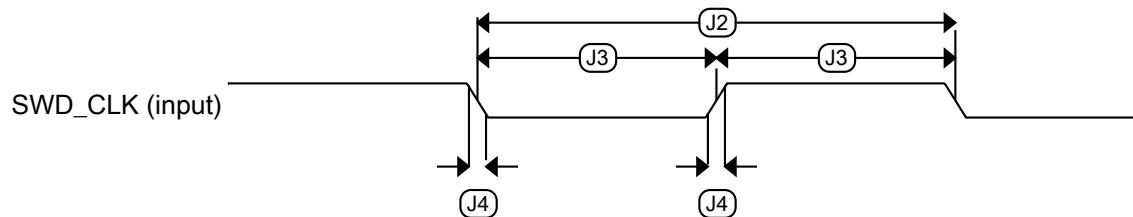
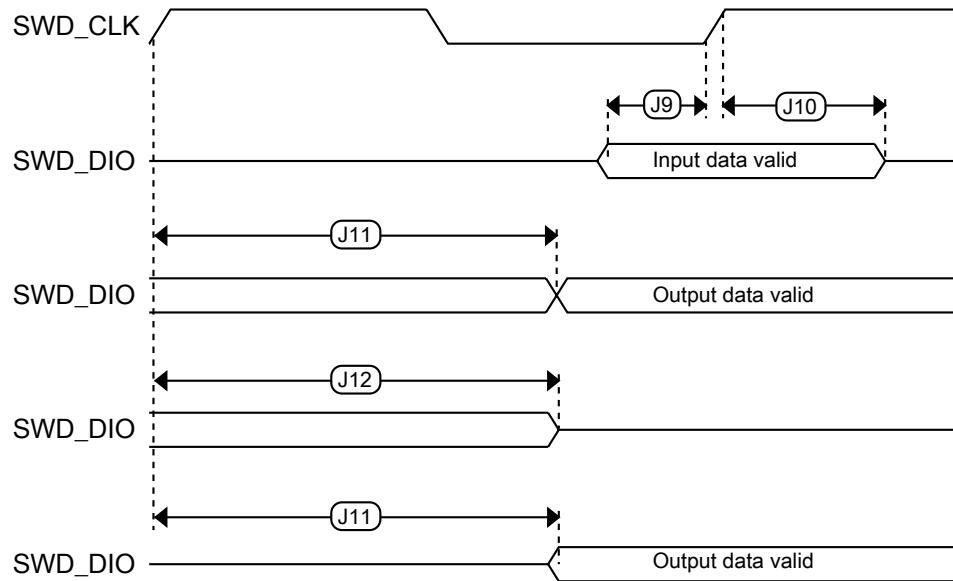
Table 16. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 16. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

**Figure 4. Serial wire clock input timing****Figure 5. Serial wire data timing**

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG-Lite specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD48M}	Supply current	—	400	500	μA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage ($VDD=1.71V-1.89V$) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage ($VDD=1.89V-3.6V$) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μs	

Table 18. IRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	μA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	μA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC_T_2M}$	Output frequency range (trimmed)	—	—	± 3	$\%f_{IRC}$	—
$f_{IRC_T_8M}$	Output frequency range (trimmed)	—	—	± 3	$\%f_{IRC}$	—
T_{su_2M}	Startup time	—	—	12.5	μs	—
T_{su_8M}	Startup time	—	—	12.5	μs	—

3.3.2 Oscillator electrical specifications