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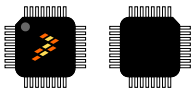
Document Number: KL82P121M72SF0
Rev. 4, 12/2016

Kinetis KL82 Microcontroller

72 MHz ARM® Cortex®-M0+ with 128 KB Flash and 96 KB SRAM

MKL82Z128Vxx7(R)

121 & 64 MAPBGA
(MC&MP)
8x8x1.43 mm Pitch
0.65 mm 5x5x1.23 mm
Pitch 0.5 mm



100 & 80 & 64 LQFP
(LL&LK&LH)
14x14 x1.7 mm Pitch
0.5mm 12x12x1.6 mm
Pitch 0.5 mm
10x10x1.6 mm Pitch
0.5 mm

The KL82 MCU family's high performance, encryption features and ultra-low power capabilities extend its reach beyond traditional mPOS pin pads and terminals into more power-restricted payment applications, such as smartphone and tablet attach readers, as well as those embedded in wearable technology.

The product offers:

- Hardware asymmetric cryptography – high-speed, code- and power-efficient data authentication with support for latest encryption protocols
- EMV®-compatible with ISO7816-3 SIM interfaces – architected for EMV compliance and supported by an EMV Level 1 software stack
- QSPI interface to expand program memory
- Sleep mode power consumption from 2.5 µA with the SRAM content retained and RTC enabled
- Crystal-less USB OTG controller, 16-bit ADC and multiple serial communication interfaces can all function autonomously in low-power modes with minimal CPU intervention
- FlexIO to support any standard and customized serial peripheral emulation

Core Processor

- 72 MHz ARM® Cortex®-M0+ core (up to 96 MHz for high-speed run)

Memories

- 128 KB program flash memory
- 96 KB SRAM
- 32 KB ROM with built-in boot loader
- 32 B backup register
- QSPI to expand program code in external high-speed serial NOR flash memory

System

- 8-channel asynchronous enhanced DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin serial wire debug (SWD) programming and debugging interface
- Micro trace buffer
- Bit manipulation engine
- Interrupt controller

Peripherals

- USB full-speed 2.0 OTG controller supporting crystal-less operation and keeping connection alive under ultra-low power
- Three low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules supporting up to 1 Mbps
- Two 16-bit SPI modules supporting up to 24Mbps
- One FlexIO module supporting emulation of additional UART, SPI, I2C, I2S, PWM and other serial modules, etc. up to 32 channels
- One 16-bit ADC module with high accurate internal voltage reference and up to 16 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC module
- Two EMVSIM modules supporting EMV L1 compatible interface
- Touch sensing interface up to 16 channels

- Memory protection unit
- SRAM bit-banding

Clocks

- 48 MHz high accuracy (up to 0.5%) internal reference clock for high-speed run
- 4 MHz high accuracy (up to 2%) internal reference clock for low-speed run
- 32 kHz internal reference clock
- 1 kHz internal reference clock
- 32–40 kHz and 3–32 MHz crystal oscillator
- PLL/FLL

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- Two low-power timers
- 4-channel periodic interrupt timer
- Independent real time clock

Security

- 128-bit unique identification number per chip
- Advanced flash security and access control
- Hardware CRC module
- Low-power trusted crypto engine supporting AES128/256, DES, 3DES, SHA256, RSA and ECC, with hardware DPA
- True random number generator

I/O

- Up to 85 General-purpose input/output pins (GPIO)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Low Power

- Down to 125 µA/MHz in Run mode
- Down to 272 nA in Stop mode (RAM and RTC retained)
- Six flexible static modes

Packages

- 121 MAPBGA 8mm x 8mm, 0.65mm pitch, 1.43mm max thickness
- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm max thickness
- 100 LQFP 14mm x 14mm, 0.5mm pitch, 1.7mm max thickness (Package Your Way)
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm max thickness (Package Your Way)
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm max thickness (Package Your Way)

NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages supporting MKL82Z128VLL7, MKL82Z128VLH7 and MKL82Z128VMP7 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Related resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL82P121M72SF0RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL82P121M72SF0[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	*x*N51R[2]
Package drawing	Package dimensions are provided in package drawings.	MAPBGA 121-pin: 98ASA00423D MAPBGA 64-pin: 98ASA00420D LQFP 100-pin: 98ASS23308W LQFP 80-pin: 98ASS23174W LQFP 64-pin: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

2. To find the associated resource, go to http://www.nxp.com and perform a search using this term with the "x" replaced by the revision of the device you are using.

Table of Contents

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/ HD)[1]	ADC channels (SE/DP)
MKL82Z128VMC7(R)	MKL82 Z128VMC7	128	96	121	MAPBGA	85	85/0	16/2
MKL82Z128VLL7(R)	MKL82Z128VL L7	128	96	100	LQFP	66	66/0	14/1
MKL82Z128VLK7(R)	MKL82Z128 VLK7	128	96	80	LQFP	56	56/0	12/1
MKL82Z128VMP7(R)	M82N7V	128	96	64	MAPBGA	41	41/0	11/1
MKL82Z128VLH7(R)	MKL82Z128V LH7	128	96	64	LQFP	41	41/0	11/1

1. INT: interrupt pin numbers; HD: high drive pin numbers

NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages supporting MKL82Z128VLL7, MKL82Z128VLH7 and MKL82Z128VMP7 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

2 Overview

The following figure shows the system diagram of this device

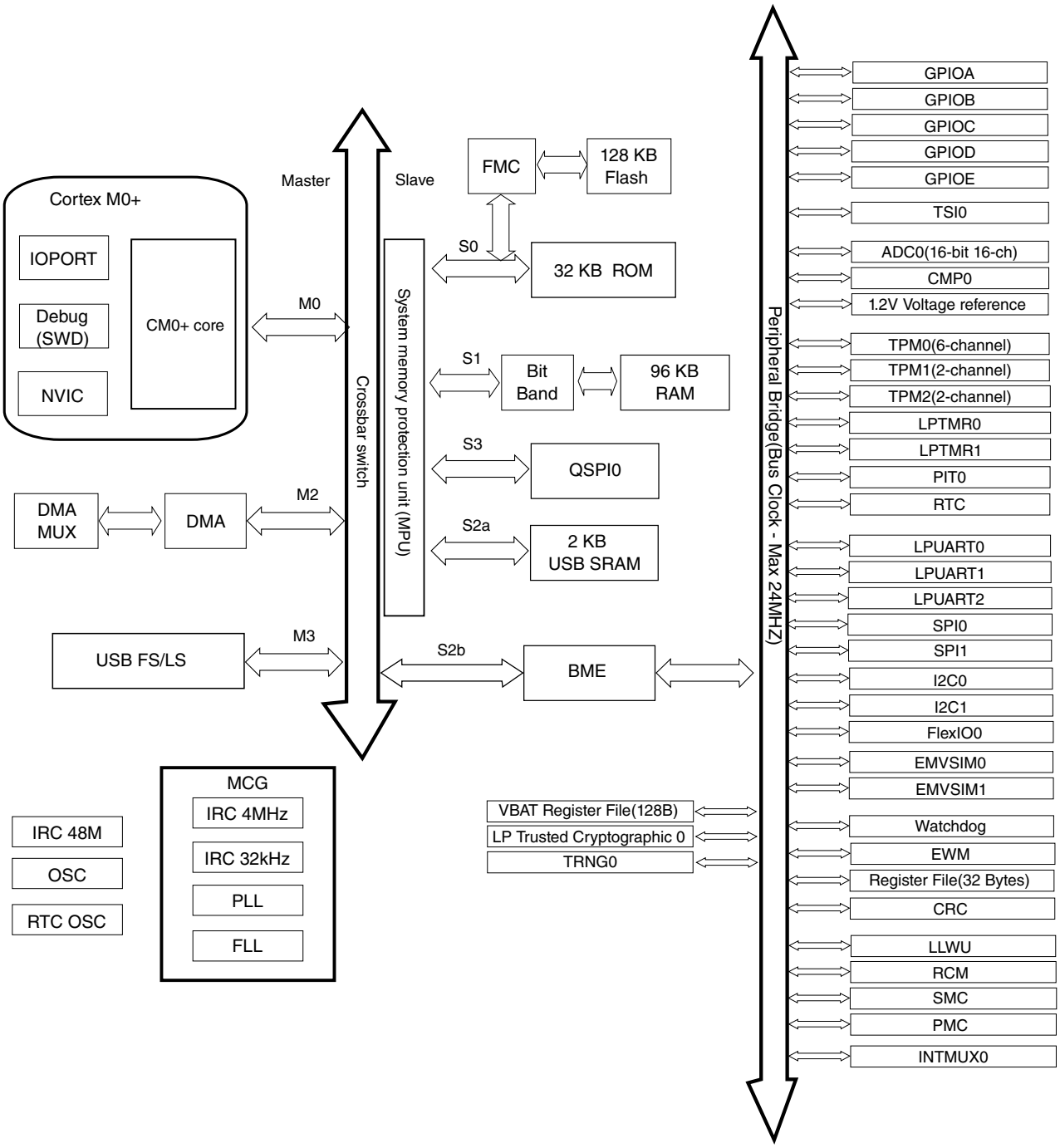


Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains two bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Stop and VLPS modes.

Wake-up sources are listed as below:

Table 2. AWIC Partial Stop, Stop and VLPS wake-up sources

Wake-up source	Description
Available system resets	RESET_b pin and WDOG when LPO is its clock source, and Debug
Low-voltage detect	Power mode controller
Low-voltage warning	Power mode controller
Pin interrupts	Port control module - any enabled pin interrupt is capable of waking the system
ADC0	The ADC is functional when using internal clock source
CMPx	Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling
I2Cx	Address match wakeup
LPUARTx	Functional when using clock source which is active in Stop and VLPS modes
USB FS/LS Controller	Wakeup
FlexIO0	Functional when using clock source which is active in Stop and VLPS modes
LPTMR	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
RTC	Functional in Stop/VLPS modes
TPM	Functional when using clock source which is active in Stop and VLPS modes
TSI0	Wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- 96 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays
  - 128 KB of embedded program memory
  - 32 KB ROM (built-in bootloader to support UART, I2C, USB, and SPI interfaces)

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC[1]	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	N	Y	Y
System reset	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

1. The VBAT POR asserts on a VBAT POR reset source. It affects only the modules withinthe VBAT power domain: RTC and VBAT Register File. These modules are notaffected by the other reset types.
2. Except SIM_SOPT1
3. Only if $\overline{\text{RESET}}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

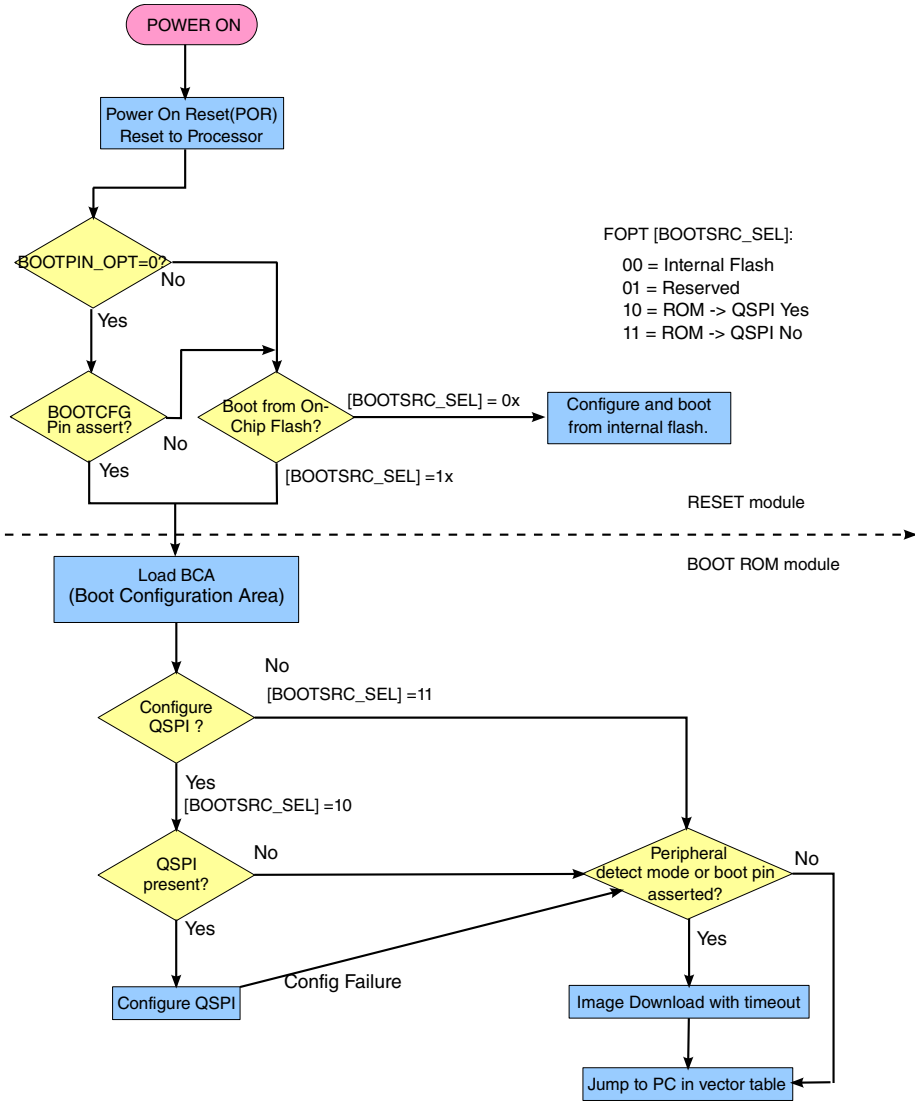


Figure 2. Boot Flow For Devices with QSPI

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

If booting from ROM, the device executes in boot loader mode or proceeds with a secondary boot to a QSPI device connected to QSPI0.

2.1.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, ceramic resonators, phase-locked loop (PLL) and frequency-locked loop (FLL). These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the 48 MHz internal resister capacitor (IRC48M) oscillator, the 4 MHz internal resister capacitor (4 MHz IRC) oscillator, the 32 kHz internal resister capacitor (32 kHz IRC) oscillator, and the low power oscillator (LPO).

The 48 MHz internal resister capacitor (IRC48M) oscillator generates a 48 MHz clock and synchronizes with the USB clock in full speed mode to achieve the required accuracy.

The 4 MHz internal resister capacitor (4 MHz IRC) oscillator generates a 4 MHz clock. It can serve as the low power, low speed system clock under very low power run (VLPR) mode or very low power wait (VLPW) mode. It can also be provided as clock source for other on-chip modules. The 4 MHz IRC cannot be used in any VLLS modes.

The 32 kHz internal resister capacitor (32 kHz IRC) oscillator generates a 32 kHz clock. It can be used as FLL internal reference clock or can be provided as low power clock source to other on-chip modules. The 32 kHz IRC cannot be used in any VLLS modes.

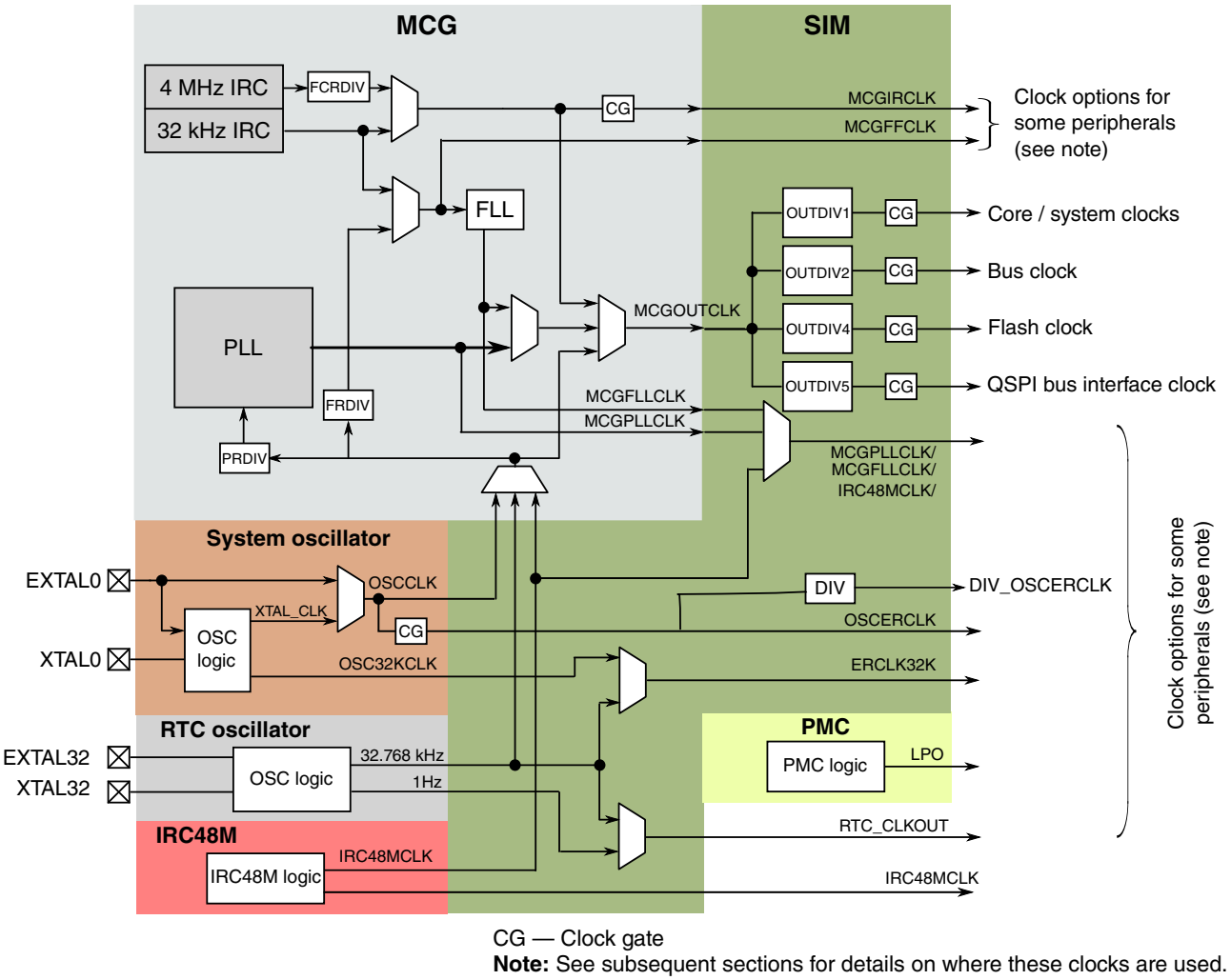
The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (1 MHz to 32 MHz), and ceramic resonators (1 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

The frequency-locked loop (FLL) can generate clock up to four programmable different frequency ranges (20–25 MHz, 40–50 MHz, 60–75 MHz or 80–100 MHz) with low speed (31.25–39.0625 kHz) internal or external reference clock. The FLL can be used as the system clock or clock source for other on-chip modules.

The phase-locked loop (PLL) can generate up to 144 MHz high speed, low jitter clock with 8–16 MHz internal or external reference clock. The PLL can be used as the system clock or clock source for other on-chip modules.

For more details on the clock operations and configurations, see Reference Manual.



CG — Clock gate
Note: See subsequent sections for details on where these clocks are used.

Figure 3. Clocking diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M0+ core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	SWD_CLK
System modules			
DMA	System clock	—	—
DMAMUX	Bus clock	—	—
Port control	Bus clock	LPO	—
Crossbar Switch	System clock	—	—
Peripheral bridges	System clock	Bus clock	—
LLWU, PMC, SIM, RCM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
INTMUX	Bus clock	—	—
MCM	System clock	—	—
EWM	Bus clock	LPO	—
Watchdog timer	Bus clock	LPO	—
Clocks			
MCG	Flash clock	MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCERCLK	—
OSC	Bus clock	OSCERCLK	—
IRC48M	—	IRC48MCLK	—
Memory and memory interfaces			
Flash controller	System clock	Flash clock	—
Flash memory	Flash clock	—	—
QSPI controller	QSPI bus interface clock	QSPI clock	QSPIx_SCK
Security			
CRC	Bus clock	—	—
TRNG	Bus clock	—	—
LTC Encryption Engine	System clock	—	—
Analog			
ADC	Bus clock	OSCERCLK, IRC48MCLK	—
CMP	Bus clock	—	—
DAC	Bus clock	—	—
VREF	Flash clock	—	—
Timers			

Table continues on the next page...

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PDB	Bus clock	—	—
PIT	Bus clock	—	—
LPTMR	Bus clock	LPO, OSCERCLK, MCGIRCLK, ERCLK32K	—
RTC	Bus clock	EXTAL32	—
Communication interfaces			
USB FS OTG	System clock	USB FS clock	—
USB DCD	Bus clock	—	—
SPI	System clock	—	DSPI_SCK
I2C	Bus clock	—	I2C_SCL
LPUART	Bus clock	LPUART clock	—
EMVSIM	Bus clock	EMVSIM clock	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—
TSI	Bus clock	LPO, ERCLK32K, MCGIRCLK	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 128-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex User Guide.

The PMC provides High Speed Run (HSRUN), Run (Run), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	High Speed Run	In HSRun mode, MCU is able to operate at a faster frequency, all device modules are operational.
	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, DAC, CMP, LPTimer, RTC, TPM, LPUART, TSI and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, USB, TSI and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.
	Low Leakage Stop	In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, CRC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM, UART, USB, and WDOGCOP are static, but retain their programming. The DAC, GPIO, and VREF are static, retain their programming, and continue to drive their previous values.
	Very Low Leakage Stop	In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes. In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The DAC, GPIO, and VREF are not operational but continue driving. In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The DAC, GPIO, and VREF are not operational but continue driving. In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled.

2.1.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 25 external wakeup pin inputs and five internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

Table 7. Wakeup sources for LLWU inputs

LLWU pins	Module sources or pin names
LLWU_P0	PTE1
LLWU_P1	PTE2
LLWU_P2	PTE4
LLWU_P3	PTA4
LLWU_P4	PTA13
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P11	PTC11
LLWU_P12	PTD0
LLWU_P13	PTD2
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_P16	PTE6
LLWU_P17	PTE9
LLWU_P18	PTE10
LLWU_P19	Reserved
LLWU_P20	Reserved
LLWU_P21	Reserved
LLWU_P22	PTA10
LLWU_P23	PTA11
LLWU_P24	PTD8
LLWU_P25	PTD11
LLWU_P26	Reserved
LLWU_P27	USB0_DP
LLWU_P28	USB0_DM[1]
LLWU_P29	Reserved
LLWU_P30	Reserved
LLWU_P31	Reserved
LLWU_M0IF	LPTMR0 or LPTMR1[2]

Table continues on the next page...

Table 7. Wakeup sources for LLWU inputs (continued)

LLWU pins	Module sources or pin names
LLWU_M1IF	CMP0
LLWU_M2IF	Reserved
LLWU_M3IF	Reserved
LLWU_M4IF	TSI0[2]
LLWU_M5IF	RTC alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC second

1. A wakeup source of LLWU, USB0_DP or USB0_DM is available only when the chip is in USB host mode.
2. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU_ME[WUMEn] (n=0-7) bit enables the internal module flag a wakeup inputs. After wakeup, the flags are cleared based on the peripheral clearing mechanism.

2.1.10 Debug controller

This device supports standard ARM 2-pin SWD debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.11 INTMUX

The Interrupt Multiplexer (INTMUX) routes the interrupt sources to the interrupt outputs. It provides interrupt status registers to monitor interrupt pending status and vector numbers and implements the ability to logical AND or OR enabled interrupts on a given channel.

The INTMUX has the following features:

- Supports 4 multiplex channels
- Each channel receives 32 interrupt sources and has one interrupt output
- Each interrupt source can be enabled or disabled
- Each channel supports logic AND or logic OR of all enabled interrupt sources

2.1.12 Watch dog

The Watchdog Timer (WDOG) keeps a watch on the system functioning and resets it in case of its failure.

The WDOG has the following features:

- Clock source input independent from CPU/bus clock. Choice between low-power oscillator (LPO) and external system clock.
- Unlock sequence for allowing updates to write-once WDOG control/configuration bits.
- All WDOG control/configuration bits are writable once only within 256 bus clock cycles of being unlocked.
- Programmable time-out period specified in terms of number of WDOG clock cycles.
- Ability to test WDOG timer and reset with a flag indicating watchdog test.
- Windowed refresh option.
- Robust refresh mechanism.
- Count of WDOG resets as they occur.
- Configurable interrupt on time-out to provide debug breadcrumbs. This is followed by a reset after 256 bus clock cycles.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 BME

The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+ based microcontrollers. It reduces up to 30% of the code size and up to 9% of the cycles for bit-oriented operations to peripheral registers.

The BME supports unsigned bit field extract, load-and-set 1-bit, load-and-clear 1-bit, bit field insert, logical AND/OR/XOR operations with byte, halfword or word-sized data type.

2.2.2 eDMA and DMAMUX

The eDMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The eDMA controller in this device implements eight channels which can be routed from up to 63 DMA request sources through DMA MUX module. Some of the peripheral request sources have asynchronous eDMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include FlexIO, LPUART0, LPUART1, LPUART2, TPM0, TPM1, TPM2, PORTA-PORTE, ADC0, and CMP0. The DMA channel 0 t0 3 can be periodically triggered by PIT via DMA MUX.

Main features are listed below:

- Dual-address transfers via 32-bit master connection to the system bus and data transfers in 8-, 16-, or 32-bit blocks
- 8-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Provide the selectable channel activation methods.
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.3 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input or internal clock source, HIRC48M clock, external crystal input clock, MCGIRCLK, MCGPLLCLK, or MCGFLLCLK.
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow

- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.4 ADC

this device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-Calibration mode

2.2.5 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC, DAC or CMP.

The VREF supports the following programmable buffer modes:

- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

A 100 nF capacitor must always be connected between VERF output (VREFO) pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

2.2.6 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The window and filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

2.2.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers. During chip power-down, RTC is powered from the backup power supply (VBAT), electrically isolated from the rest of the chip, continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt
- 64-bit monotonic counter with roll-over protection

2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has four independent channels and each channel has a 32-bit counter. Two channels can be chained together to form a 64-bit counter.

The PIT module can trigger a DMA transfer on the first four DMA channels. and also can be selected as ADC, TPM, and DAC trigger source.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, both of their clock sources are selectable fromIRC48M, MCGFLLCLK, MCGPLLCLK, MCGIRCCLK or external crystal clock, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

- Full-duplex, standard non-return-to-zero (NRZ) format

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods: idle line wakeup, address mark wakeup, receive data match
- Automatic address matching to reduce ISR overhead
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width

2.2.12 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers
- Support DMA