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MKMxxZxxCxx5



KM Family

Supports the following:

MKM14Z64CHH5, MKM14Z128CHH5,
MKM33Z64CLH5, MKM33Z128CLH5,
MKM33Z64CLL5, MKM33Z128CLL5,
MKM34Z128CLL5

Features

- Operating Characteristics
 - Voltage range: 1.71 V to 3.6 V (when Analog Front End (AFE) is not used)
 - Voltage range: 2.7 V to 3.6 V (when Analog Front End (AFE) is used)
 - iRTC battery supply voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40°C to 85°C
- Performance
 - Up to 50 MHz ARM Cortex-M0+ core delivering 0.95 Dhrystone MIPS per MHz
- Memories and memory interfaces
 - 128/64 KB program flash memory. There is no FlexMemory on these devices
 - 16 KB of single access RAM
- Clocks
 - 1 to 32 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Multi-purpose clock generator
- System peripherals
 - Multiple low-power modes to provide power optimization based on application requirements
 - Memory protection unit with multi-master protection
 - 4-channel DMA controller, supporting up to 64 request sources
 - External watchdog monitor
 - Robust watchdog monitor
 - Low-leakage wakeup unit
 - Asynchronous wakeup unit
 - Peripheral Crossbar (allows internal signals to be connected to other on-chip modules)
- Security and integrity modules
 - Hardware programmable CRC module to support fast cyclic redundancy checks
 - Hardware random-number generator
 - 128-bit unique identification (ID) number per chip
- Human-machine interface
 - Segment LCD controller supporting up to 36 frontplanes and 8 backplanes or 40 frontplanes and 4 backplanes
 - General-purpose input/output which can act as Rapid GPIO (single cycle access)
- Analog modules
 - 16-bit SAR ADC
 - 24-bit Analog Front End comprising of 24-bit Sigma Delta ADCs (after averaging)
 - Programmable Gain Amplifier (PGA with gains up to 32)
 - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
 - 1.2V Voltage reference
- Timers
 - 4 channel Quad Timer with 16-bit counters
 - Periodic interrupt timers
 - 16-bit low-power timer
 - Independent Real Time Clock with calendaring and compensation
- Communication interfaces
 - One SPI module with FIFO support (supports 5V AMR operation)
 - One SPI module without FIFO (no AMR operation)
 - Two I2C modules with SMBus support
 - Two UART modules with ISO7816 support and Two UART without ISO 7816 support
 - Any one SCI can be used for IrDA operation. 5V AMR support on one SCI.

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 Ordering parts

1.1 Determining valid order-able parts

Valid order-able part numbers are provided on the web. To determine the order-able part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM13Z64CHH5
- MKM14Z64CHH5
- MKM14Z128CHH5
- MKM32Z64CLH5
- MKM33Z64CLH5
- MKM33Z128CLH5
- MKM32Z64CLL5
- MKM33Z64CLL5
- MKM33Z128CLL5
- MKM34Z128CLL5
- MKM38Z128CLL5

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K M S R FFF T PP CC N

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> M = Fully qualified, general market flow P = Pre-qualification (Proto)
K	Main family	<ul style="list-style-type: none"> K = Kinetis
M	Sub family	<ul style="list-style-type: none"> M1 = Metering only (No LCD support) M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	<ul style="list-style-type: none"> 2 = 1 SD ADC with PGA and 1 SD ADC 3 = 2 SD ADC with PGA and 1 SD ADC 4 = 2 SD ADC with PGA and 2 SD ADC 8 = Same as '4'.
R	Silicon revision	<ul style="list-style-type: none"> Z = Initial (Blank) = Main A = Revision after main
FFF	Program flash memory size	<ul style="list-style-type: none"> 64 = 64 KB 128 = 128 KB
T	Temperature range (°C)	<ul style="list-style-type: none"> C = -40 to 85
PP	Package identifier	<ul style="list-style-type: none"> HH = 44 LGA (5 mm x 5 mm) LH = 64 LQFP (10 mm x 10 mm) LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> 5 = 50 MHz
N	Packaging type	<ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

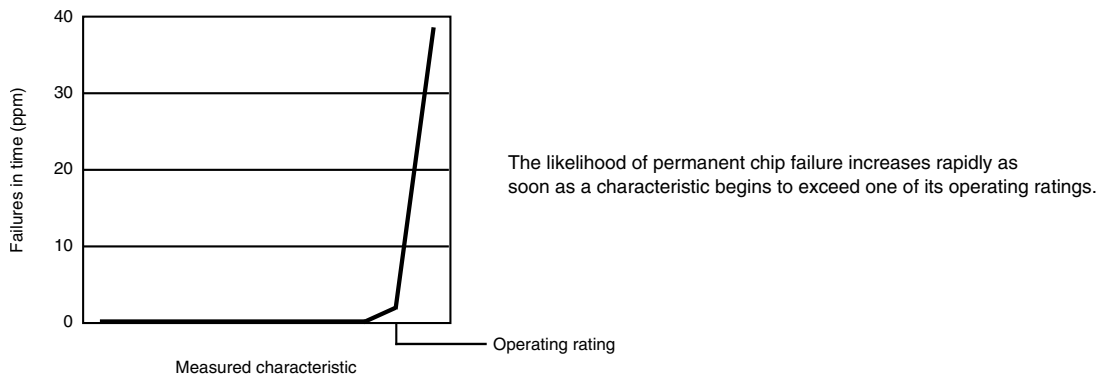
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

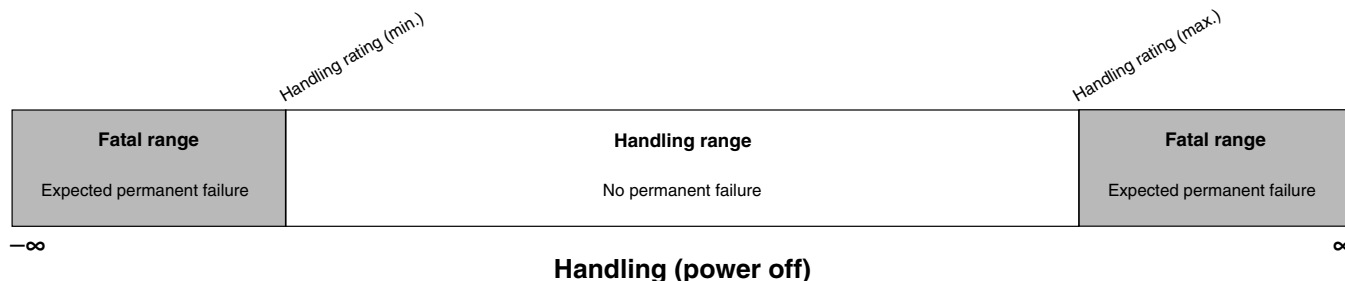
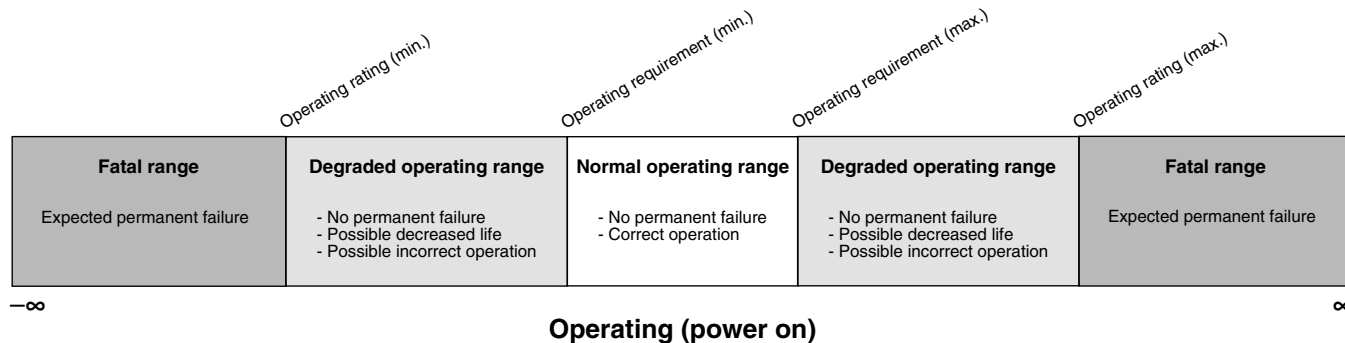
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

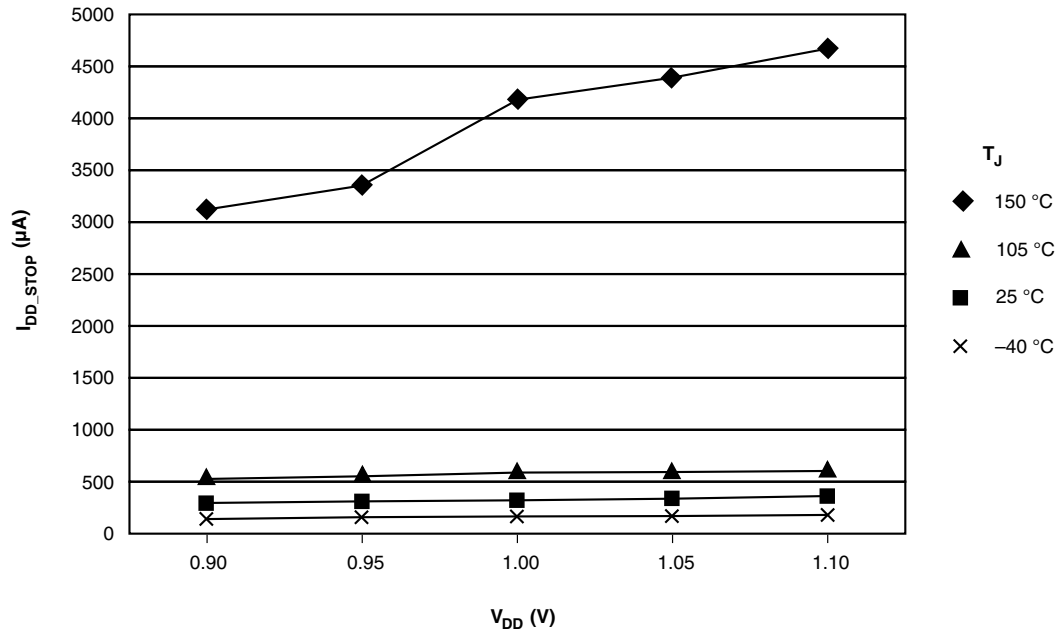
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	$^{\circ}\text{C}$
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	-4000	+4000	V	1
	Electrostatic discharge voltage, human body model (RESET pin only)	-2500	+2500	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	-750	+750	V	2
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	3
V _{PESD}	Powered ESD voltage	-6000	+6000	V	
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.6	V
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{DTamper}$	Tamper input voltage	-0.3	$V_{BAT} + 0.3$	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{BAT}	RTC battery supply voltage	-0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

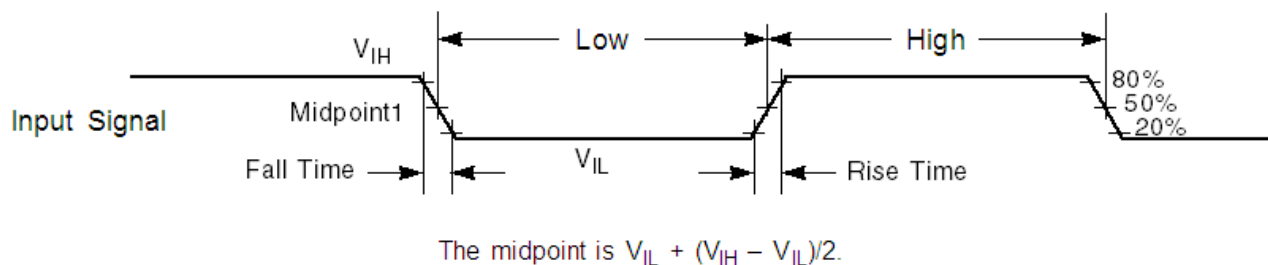


Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V _{DDA}	Analog supply voltage	2.7	3.6	V	
V _{DD} - V _{DDA}	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
V _{SS} - V _{SSA}	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V _{IH}	Input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	0.7 × V _{DD}	—	V	
		0.75 × V _{DD}	—	V	
V _{IL}	Input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	—	0.35 × V _{DD}	V	
		—	0.3 × V _{DD}	V	
V _{HYS}	Input hysteresis	0.06 × V _{DD}	—	V	
I _{CDIO}	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V 	-5	—	mA	
I _{CAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection) 	-3	—	mA	
		—	+3		
I _{Ccont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection • Positive current injection 	-25	—	mA	
		—	+25		
V _{RFVBAT}	V _{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW1H}	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	2.62	2.70	2.78	V	1
V _{LVW2H}		2.72	2.80	2.88	V	
V _{LVW3H}		2.82	2.90	2.98	V	
V _{LVW4H}		2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L}	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) 	1.74	1.80	1.86	V	1
V _{LVW2L}		1.84	1.90	1.96	V	
V _{LVW3L}		1.94	2.00	2.06	V	
V _{LVW4L}		2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high-drive strength <ul style="list-style-type: none"> 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 20 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 10 mA 	V _{DD} - 0.5	—	V	
		V _{DD} - 0.5	—	V	
	Output high voltage — low-drive strength <ul style="list-style-type: none"> 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA 	V _{DD} - 0.5	—	V	
		V _{DD} - 0.5	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — high-drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 10 mA	—	0.5	V	
	Output low voltage — low-drive strength				
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 2.5 mA	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R _{PU}	Internal pullup resistors	30	60	kΩ	1,
R _{PD}	Internal pulldown resistors	30	60	kΩ	2

1. Measured at V_{input} = V_{SS}
2. Measured at V_{input} = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLS_x→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temp: -40 °C, 25 °C, and 85 °C
- V_{DD}: 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563	659	μs	1
	• VLLS0 → RUN	—	372	μs	
	• VLLS1 → RUN	—	372	μs	
	• VLLS2 → RUN	—	273	μs	
	• VLLS3 → RUN	—	273	μs	
	• VLPS → RUN	—	5.0	μs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> • STOP → RUN 	—	5.0	μs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash <ul style="list-style-type: none"> • @ 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	6.17	7.1	mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash <ul style="list-style-type: none"> • @ 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	8.24	10.4	mA	2
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	3.95	4.65	mA	2
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power) <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	3.81	4.4	mA	2, 3
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	248.8	500	μA	4
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	343.4	530	μA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	336.62	500	μA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	626.18	2000	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	162	350	μA	6
		—	158.50	330	μA	
		—	446.94	1700	μA	
I _{DD_STOP}	Stop mode current at 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	311.90	730	μA	
		—	364	700	μA	
		—	645.13	2250	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	8.56	46	μA	
		—		44	μA	
		—		1500	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	1.98	3.5	μA	
		—		3.3	μA	
		—		85	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	1.24	2.6	μA	
		—		2.5	μA	
		—		59.5	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	0.89	1.7	μA	
		—		1.6	μA	
		—		38.8	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	0.35	0.67	μA	
		—		0.64	μA	
		—		38	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	0.472	0.76	μA	
		—		0.72	μA	
		—		38.4	μA	
I _{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	0.3	1	μA	
		—		0.95	μA	
		—		15	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz. <ul style="list-style-type: none"> • @ 3.0 V <ul style="list-style-type: none"> • 25 °C • -40 °C • 105 °C 	—	1.3 ⁷	3	μA	8, 9
				2.5	μA	
				16	μA	

1. See AFE specification for IDDA.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 μA.
4. 2 MHz core, system, bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core, system and bus clock, and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core, system and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Current consumption will vary with number of CPU accesses done and is dependent on the frequency of the accesses and frequency of bus clock. Number of CPU accesses should be optimized to get optimal current value.
8. Includes 32 kHz oscillator current and RTC operation.
9. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	16	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	12	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 50 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF
C _{IN_D_io60}	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f _{SYS}	System and core clock		50	MHz	
f _{BUS}	Bus clock		25	MHz	
f _{FLASH}	Flash clock		25	MHz	
f _{AFE}	AFE Modulator clock		6.5	MHz	
VLPR mode ¹					
f _{SYS}	System and core clock		2	MHz	
f _{BUS}	Bus clock		1	MHz	
f _{FLASH}	Flash clock		1	MHz	
f _{AFE}	AFE Modulator clock ²		1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time—Low (All pins) and high drive (only PTC2) strength				3
	<ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7 \text{ V}$ • $2.7 \leq V_{DD} \leq 3.6 \text{ V}$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7 \text{ V}$ • $2.7 \leq V_{DD} \leq 3.6 \text{ V}$ 	—	8	ns	
		—	5	ns	
		—	27	ns	
		—	16	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. Only PTC2 has high drive capability and load is 75 pF, other pins load (low drive) is 25 pF.

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	−40	105	°C
T _A	Ambient temperature	−40	85	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	44 LGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	63	95	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	50	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	53	79	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	44	45	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	18	28	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1
after clock edge, tDVO	Data valid Time	32	ns	1
tHO	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pf.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, tSUI	Data setup time	4.7	ns	
inputs,tHI	Data hold time	0	ns	
after clock edge, tDVO	Data valid Time	49.4	ns	2
tHO	Data Valid Hold	0	ns	

1. Frequency of SWD clock (18 Mhz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

6.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to the XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1

1. Input Transition: 1ns. Output Load: 50 pf.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports)

Table 15. AFE switching characteristics (2.7V-3.6V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	36	ns	
inputs, tHI	Data hold time	0	ns	

AFE switching characteristics at (1.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, tSUI	Data setup time	5.1	ns	
inputs, tHI	Data hold time	0	ns	

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports)

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	54	ns	
inputs, tHI	Data hold time	0	ns	

6.2 Clock modules

6.2.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$\Delta f_{\text{ints_t}}$	Total deviation of internal reference frequency (slow clock) over voltage and temperature	—	± 4	± 15	%		
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	33.4234	kHz		
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1	
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—			% f_{dco}	1	
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—			% f_{dco}	1	
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C			4	MHz		
$\Delta f_{\text{intf_t}}$	Total deviation of internal reference frequency (fast clock) over voltage and temperature	—	± 10	± 15	%		
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz		
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz		
FLL							
f_{dco}	DCO output frequency range	Low-range (DRS=00) $640 \times f_{\text{ints_t}}$	20	20.97	22	MHz	2, 3
		Mid-range (DRS=01) $1280 \times f_{\text{ints_t}}$	40	41.94	45	MHz	
		Mid-high range (DRS=10) $1920 \times f_{\text{ints_t}}$	60	62.91	67	MHz	
		High-range (DRS=11) $2560 \times f_{\text{ints_t}}$	80	83.89	90	MHz	
$f_{\text{dco_t_DMX32}}$	DCO output frequency	Low-range (DRS=00) $732 \times f_{\text{ints_t}}$	—	23.99	—	MHz	4, 5, 6
		Mid-range (DRS=01) $1464 \times f_{\text{ints_t}}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{\text{ints_t}}$	—	71.99	—	MHz	
		High-range (DRS=11) $2929 \times f_{\text{ints_t}}$	—	95.98	—	MHz	
$J_{\text{cyc_fll}}$	FLL period jitter	—	70	140	ps	7	
$t_{\text{fill_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	8	
PLL							

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{VCO}	VCO operating frequency	11.71875	12.288	14.6484375	MHz	
I_{PLL}	PLL operating current <ul style="list-style-type: none"> IO 3.3 V current Max core voltage current 	—	300 100	—	μ A	9
f_{PLL_ref}	PLL reference frequency range	31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) <ul style="list-style-type: none"> $f_{VCO} = 12$ MHz 			700	ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	11
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.2 Oscillator electrical specifications

6.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	μA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I _{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 1 MHz	—	300	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
	Capacitance of EXTAL	247	—	—	ff	
	• Die level (100 LQFP)	0.495			pF	
	• Package level (100 LQFP)					
	Capacitance of XTAL	265	—	—	ff	
	• Die level (100 LQFP)	0.495			pF	
	• Package level (100 LQFP)					
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...