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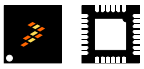
Kinetis V Series KV10, 32/16 KB Flash

75 MHz Cortex-M0+ Based Microcontroller

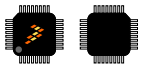
The Kinetis V Series KV1x MCU family is the entry point into the V Series and provides a high-performance, cost-competitive solution for 3-phase sensorless BLDC and PMSM motor control. Built upon the ARM® Cortex®-M0+ based core running at 75 MHz with hardware square root and divide capability, it delivers a 35% increase in performance versus comparable MCUs allowing it to target BLDC as well as PMSM motors.
Additional features include:

- dual 16-bit analog-to-digital controllers (ADCs) sampling at up to 1.2 MS/s in 12-bit mode.
- multiple motor control timers, up to 32 KB of flash memory and a comprehensive enablement suite from Freescale
- third-party resources including reference designs, software libraries and powerful motor configuration tools

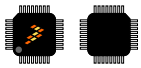
MKV10Z32VLC7
MKV10Z32VFM7
MKV10Z32VLF7
MKV10Z16VLC7
MKV10Z16VFM7
MKV10Z16VLF7



32 QFN
5 x 5 x 0.9 mm Pitch
0.5 mm



32 LQFP
7 x 7 x 1.4 mm Pitch
0.8 mm



48 LQFP
7 x 7 x 1.4 mm Pitch 0.5 mm

Performance
- Up to 75 MHz ARM Cortex-M0+ based core

Memories and memory interfaces
- Up to 32 KB of program flash memory
- Up to 8 KB of RAM

System peripherals
- Nine low-power modes to provide power optimization based on application requirements
- 4-channel DMA controller
- SWD interface and Micro Trace buffer
- Bit Manipulation Engine (BME)
- External watchdog timer
- Advanced independent clocked watchdog
- Memory Mapped Divide and Square Root (MMDVSQ) module

Clocks
- 32 to 40 kHz or 3 to 32 MHz crystal oscillator
- Multipurpose clock generator (MCG) with frequency-locked loop referencing either internal or external reference clock

Security and integrity modules
- 80-bit unique identification (ID) number per chip
- Hardware CRC module

Communication interfaces
- One 16-bit SPI module
- One I2C module
- Two UART modules

Timers
- Programmable delay block
- One 6-channel FlexTimer (FTM) for motor control/ general purpose applications
- Two 2-channel FlexTimers (FTM) with quadrature decoder functionality
- 16-bit low-power timer (LPTMR)

Operating Characteristics
- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): –40 to 105°C

Analog modules
- Two 16-bit SAR ADCs
- 12-bit DAC
- Analog comparator (CMP) containing a 6-bit DAC and programmable reference input

Human-machine interface
- General-purpose I/O

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKV10Z32VLC7	32	8	28
MKV10Z32VFM7	32	8	28
MKV10Z32VLF7	32	8	40
MKV10Z16VLC7	16	8	28
MKV10Z16VFM7	16	8	28
MKV10Z16VLF7	16	8	40

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KV10PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV10P48M75RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KV10Z_1N81H[1]
Package drawing	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D[1] LQFP 32-pin: 98ASH70029A[1] LQFP 48-pin: 98ASH00962A[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

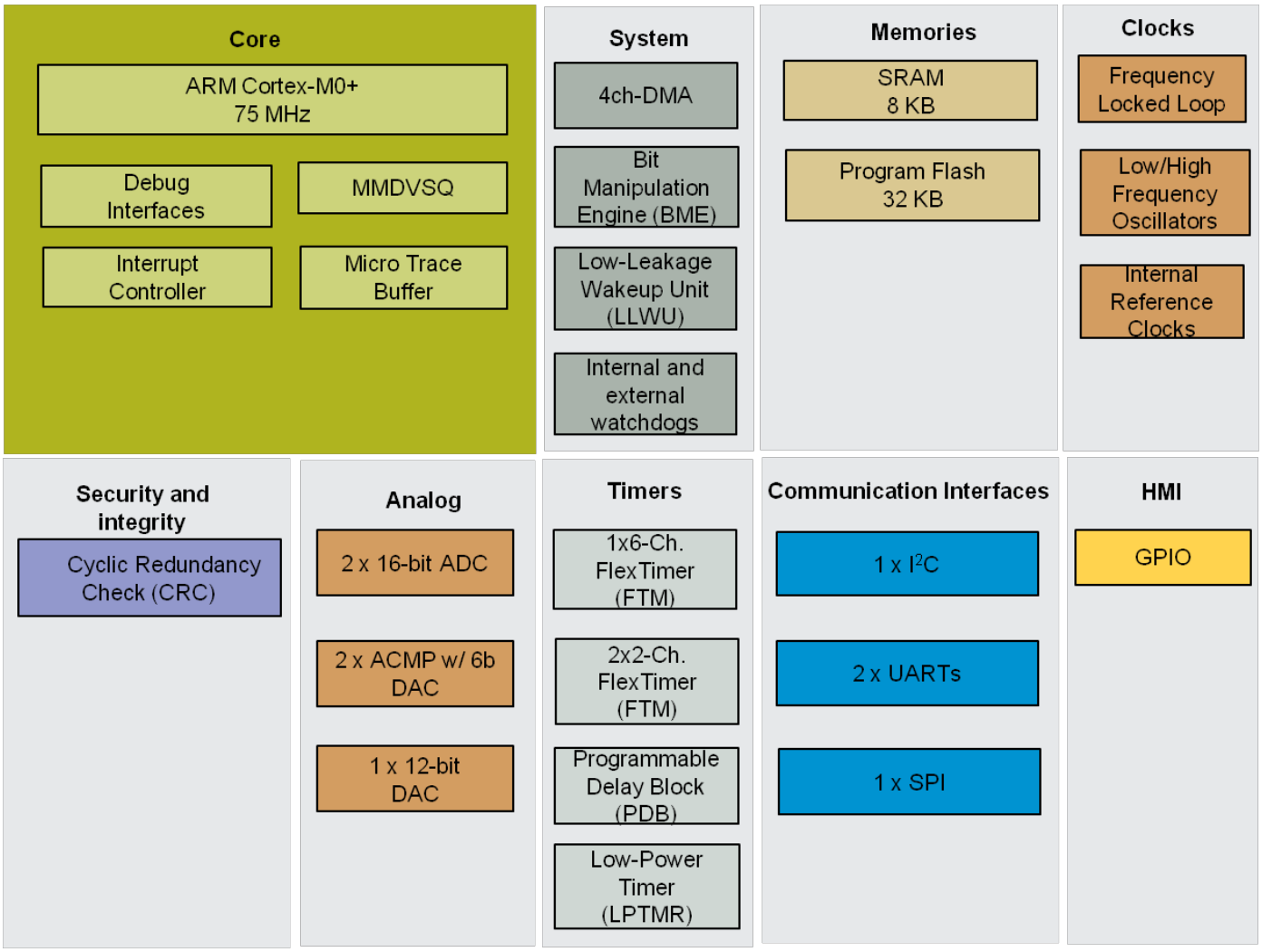


Figure 1. KV10 block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	–0.3	VDD + 0.3[1]	V
	Open drain pins (PTC6 and PTC7)	–0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

2 General

Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on freescale.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

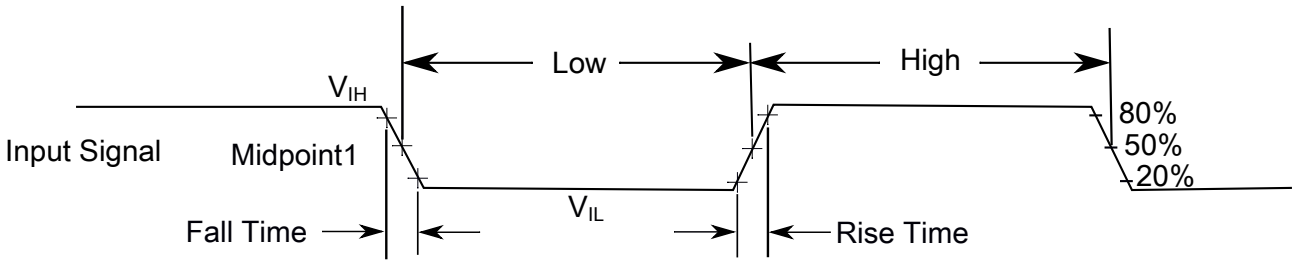


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	Pin negative DC injection current—single pin • V_{IN} < V_{SS}–0.3V	-5	—	mA	1

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current—regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	–25	—	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/I_{ICIO}.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad All port pins, except PTC6 and PTC7 • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
V_{OH}	Output high voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad All port pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	 — —	 0.5 0.5	 V V	
V_{OL}	Output low voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	1
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	2

1. Measured at V_{DD} = 3.6 V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	106	115	µs	
	• VLLS1 → RUN	—	106	115	µs	
	• VLLS3 → RUN	—	47	53	µs	
	• VLPS → RUN	—	4.5	4.8	µs	
	• STOP → RUN	—	4.5	4.8	µs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values stated in the following table represent characterized results equivalent to the mean plus six times the standard deviation (mean + 6 sigma).

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	5	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz (25 MHz Bus)	—	5	6.3	mA	

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 3.0 V 50 MHz (25 MHz Bus)	—	5	6.3	mA	
	• at 1.8 V 75 MHz (25 MHz Bus)	—	6.5	7.8	mA	
	• at 3.0 V 75 MHz (25 MHz Bus)	—	6.5	7.5	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz	—	7.1	8.2	mA	
	• at 3.0 V 50 MHz	—	7.1	8	mA	
	• at 1.8 V 75 MHz	—	9.4	10.9	mA	
	• at 3.0 V 75 MHz	—	9.4	10.6	mA	
I_{DD_WAIT}	Wait mode high frequency 75 MHz current at 3.0 V — all peripheral clocks disabled	—	4	5.2	mA	—
I_{DD_WAIT}	Wait mode reduced frequency 50 MHz current at 3.0 V — all peripheral clocks disabled	—	3.4	4.7	mA	—
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks disabled	—	215	437	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks enabled	—	313	570	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks disabled	—	149	303	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks enabled	—	244	347	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_STOP}	Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	248	280	µA	
	• at 50 °C	—	261	315		
	• at 70 °C	—	278	333		
	• at 85 °C	—	307	435		
	• at 105 °C	—	381	510		
I_{DD_VLPS}	Very-Low-Power Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	2.2	4.3		
	• at 50 °C	—	4.2	9.9		

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 70 °C	—	8.8	24	µA	
	• at 85 °C	—	16.2	59		
	• at 105 °C	—	36.7	82		
I_{DD_VLLS3}	Very-Low-Leakage Stop mode 3 current at 3.0 V • -40 °C to 25 °C				µA	—
	• at 50 °C	—	1.3	5.7		
	• at 70 °C	—	1.9	6.1		
	• at 85 °C	—	3.3	7.4		
	• at 105 °C	—	5.8	11.2		
		—	13	18		
I_{DD_VLLS1}	Very-Low-Leakage Stop mode 1 current at 3.0 V • -40°C to 25°C				µA	—
	• at 50°C	—	0.8	3.0		
	• at 70°C	—	1.2	4.9		
	• at 85°C	—	2.2	7.0		
	• at 105°C	—	4	12.5		
		—	9.4	29.0		
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • -40 °C to 25 °C				µA	—
	• at 50 °C	—	0.279	0.7		
	• at 70 °C	—	0.638	1.2		
	• at 85 °C	—	1.63	2.5		
	• at 105 °C	—	3.4	4.5		
		—	8.9	12.0		
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V • -40 °C to 25 °C				µA	2
	• at 50 °C	—	0.098	0.485		
	• at 70 °C	—	0.448	0.788		
	• at 85 °C	—	1.4	2.29		
	• at 105 °C	—	3.19	4.14		
		—	8.47	11.8		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. No brownout

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	510	560	560	560	610	680	
	VLPS	510	560	560	560	610	680	
	STOP							
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{SPI}	SPI peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{I2C}	I2C peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source							

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock) OSCERCLK (4 MHz external crystal)	66 214	66 237	66 246	66 254	66 260	66 268	µA
IFTM	FTM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. MCGIRCLK (4 MHz internal reference clock) OSCERCLK (4 MHz external crystal)	150 300	150 300	150 300	150 320	150 340	150 350	µA
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA
I_{WDOG}	WDOG peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock) OSCERCLK (4 MHz external crystal)	66 214	66 237	66 246	66 254	66 260	66 268	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode (except for 75 MHz which is in FEE mode), and BLPE for VLPR mode
- No GPIOs toggled

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

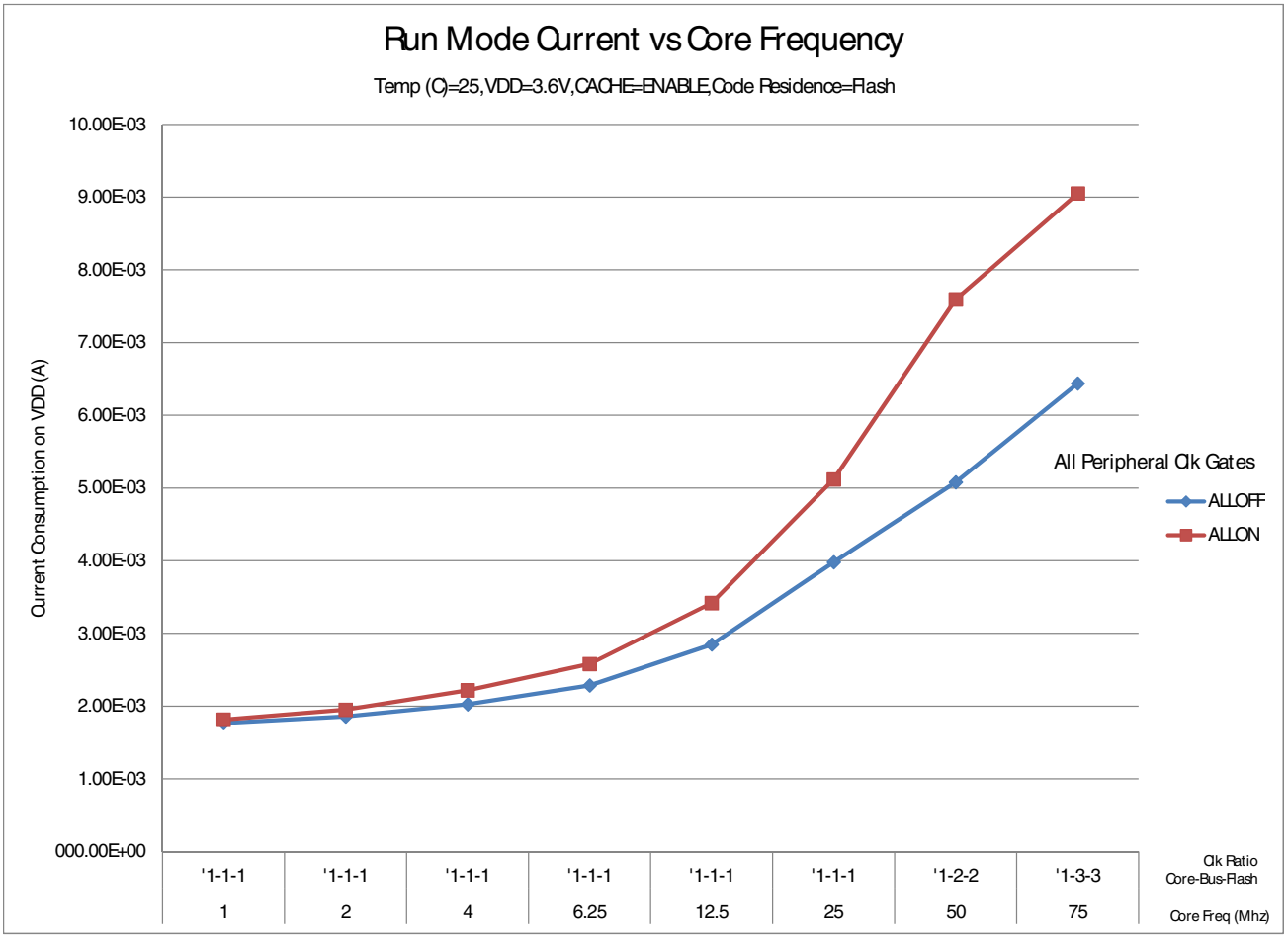


Figure 3. Run mode supply current vs. core frequency

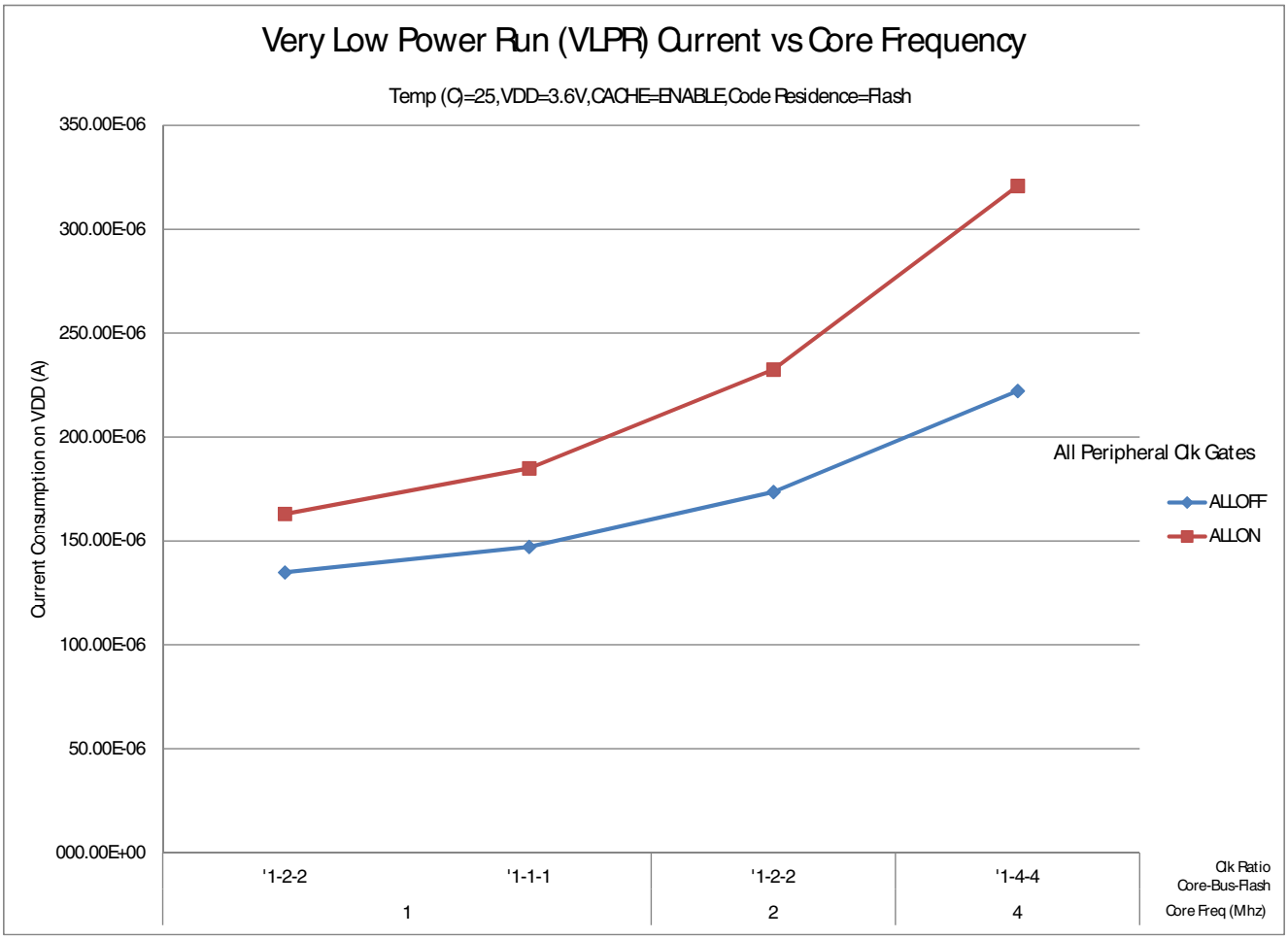


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	15	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	17	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	48	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
High Speed run mode					
f_{SYS}	System and core clock	—	75	MHz	
f_{BUS}	Bus clock	—	25	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FTM}	FTM clock	—	75	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 15 25	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

NOTE

Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA}$ x chip power dissipation.

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	48 LQFP	32 LQFP	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	81	85	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	57	57	34	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	68	72	82	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	51	50	28	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	33	14	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	25	25	2.5	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	7	7	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

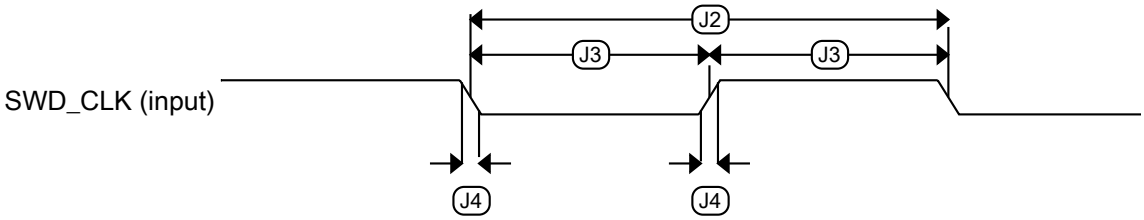


Figure 5. Serial wire clock input timing

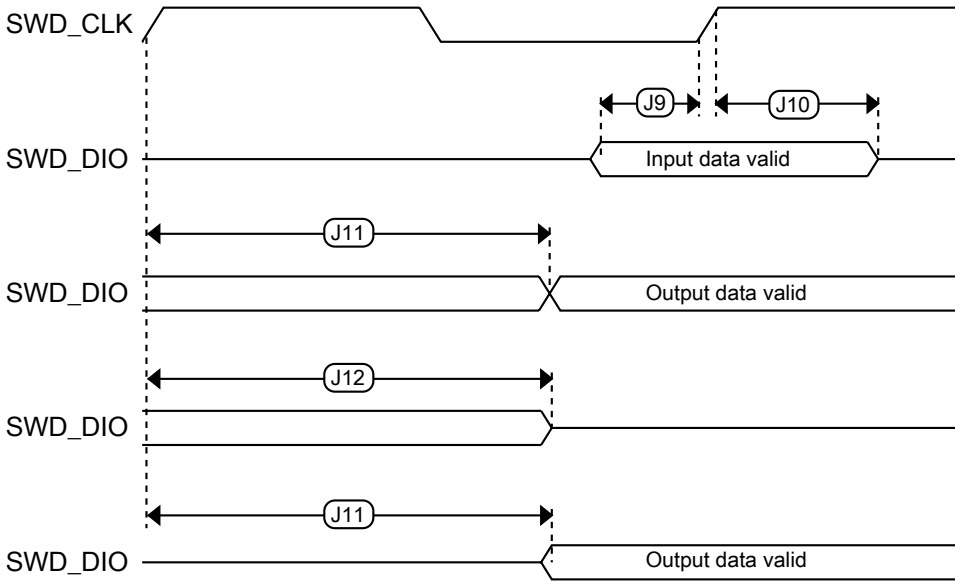


Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	±2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00, DMX32 = 0) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01, DMX32 = 0) 1280 × f_{fll_ref}	40	41.94	48	MHz	
		Mid range (DRS = 10, DMX32 = 0) 1920 x f_{fll_ref}	60	62.915	75	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00, DMX32 = 1) 732 × f_{fll_ref}	—	23.99	—	MHz	5 6
		Mid range (DRS = 01, DMX32 = 1) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid range (DRS = 10, DMX32 = 1) 2197 × f_{fll_ref}	–	71.991	–	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 75 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.

4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or there is a change from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	500	—	µA	
	• 8 MHz	—	600	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

Table 16. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.