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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Kinetis KV30F 64 KB/128 KB Flash

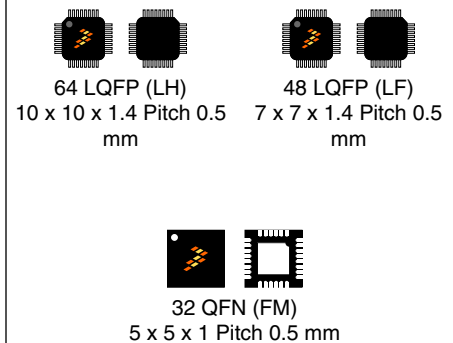
## 100 MHz ARM® Cortex®-M4 Based Microcontroller with FPU

The KV30 MCU family is a highly scalable member of the Kinetis V series and provides a high-performance, cost-competitive motor-control solution. Built on the ARM® Cortex®-M4 core running at 100 MHz, combined with floating point and DSP capability, it delivers a highly capable platform enabling customers to build a highly scalable solution portfolio.

Additional features include:

- Dual 16-bit ADCs sampling at up to 1.2 MS/s in 12-bit mode
- Highly accurate and flexible motor control timers
- Excellent processing efficiency, 100 MHz ARM® Cortex®-M4-based device with Floating-Point Unit in a tiny form factor
- Enabled to support Kinetis Motor Suite (KMS), a bundled hardware and software solution that enables rapid configuration of BLDC and PMSM motor drive systems.

**MKV30F128Vxx10**  
**MKV30F64Vxx10**  
**MKV30F128Vxx10P**  
**MKV30F64Vxx10P**



### Performance

- 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

### Memories and memory interfaces

- Up to 128 KB of embedded flash and 16 KB of RAM
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

### System peripherals

- 4-channel DMA controller
- Independent External and Software Watchdog monitor

### Clocks

- Crystal oscillator: 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz
- Multi-purpose clock generator with FLL

### Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Flash access control to protect proprietary software

### Human-machine interface

- Up to 46 general-purpose I/O (GPIO)

### Analog modules

- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- One 12-bit DAC
- Two analog comparators (CMP) with 6-bit DAC
- Accurate internal voltage reference (not available in 32-pin QFN package)

### Communication interfaces

- One SPI module
- Two UART modules
- One I2C: Support for up to 1 Mbps operation

### Timers

- One 6-channel motor-control general-purpose/PWM timer
- Two 2-channel motor-control general-purpose timers with quadrature decoder functionality

### Operating Characteristics

- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

### Kinetis Motor Suite

- Supports Velocity and Position control of BLDC & PMSM motors



- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

### Ordering Information

Part Number	Memory		Number of GPIOs
	Flash (KB)	SRAM (KB)	
MKV30F128VLH10	128	16	46
MKV30F128VLF10	128	16	35
MKV30F128VFM10	128	16	26
MKV30F64VLH10	64	16	46
MKV30F64VLF10	64	16	35
MKV30F64VFM10	64	16	26
MKV30F128VLF10P	120	16	35
MKV30F64VLH10P <sup>1</sup>	56	16	46
MKV30F64VLF10P <sup>1</sup>	56	16	35

1. This part number is subject to removal

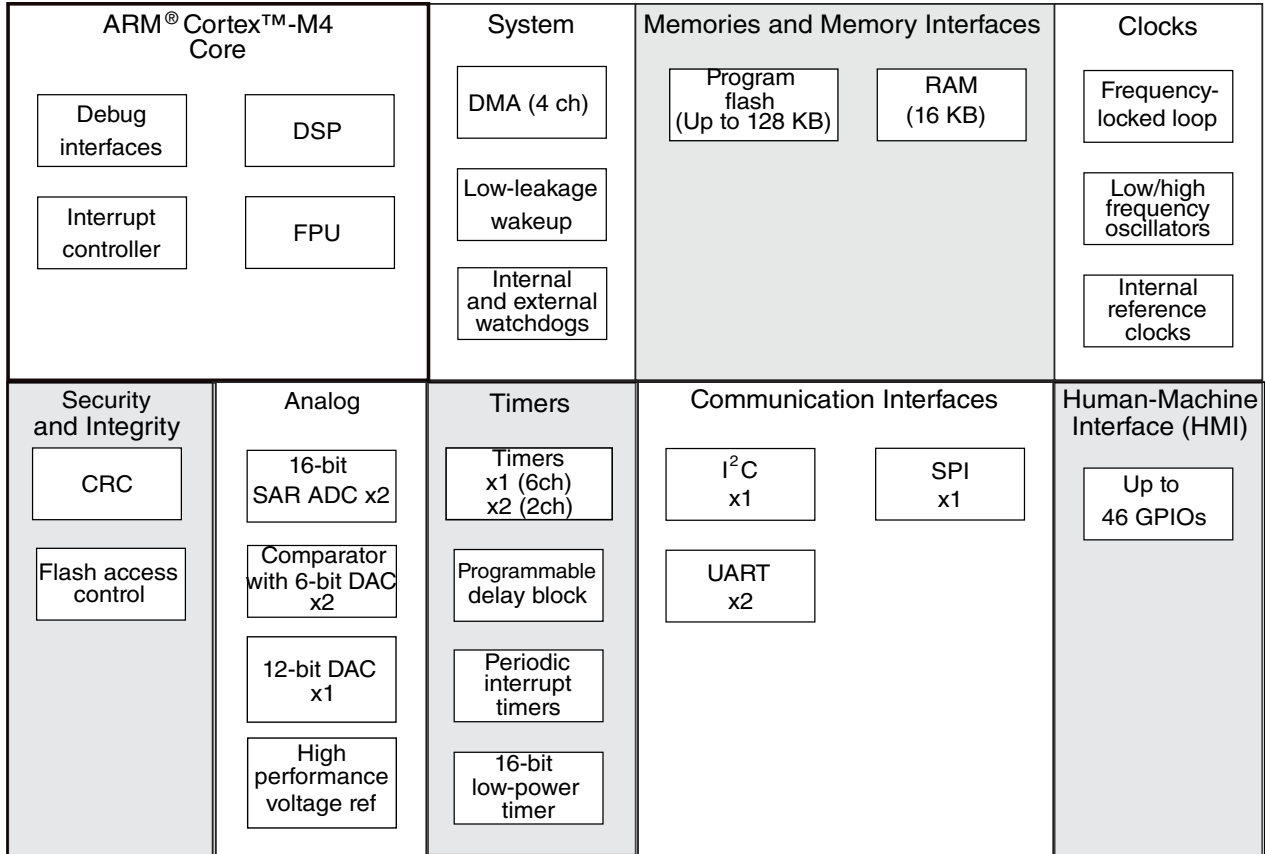
### Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Product Selector</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	<a href="#">KV30FKV31FPB</a>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	<a href="#">KV30P64M100SFARM</a>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
KMS User Guide	The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution.	Kinetis Motor Suite User's Guide (KMS100UG) <sup>1</sup>
KMS API Reference Manual	The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks.	Kinetis Motor Suite API Reference Manual (KMS100RM) <sup>1</sup>
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	<a href="#">Kinetis_V_0N36M</a>
Package drawing	Package dimensions are provided by the part number: <ul style="list-style-type: none"> <li>• MKV30F64VLF10P</li> <li>• MKV30F64VLH10P</li> <li>• MKV30F128VLH10</li> <li>• MKV30F128VLF10</li> <li>• MKV30F128VFM10</li> <li>• MKV30F128VLF10P</li> </ul>	<ul style="list-style-type: none"> <li>• <a href="#">98ASH00962A</a></li> <li>• <a href="#">98ASS23234W</a></li> <li>• <a href="#">98ASS23234W</a></li> <li>• <a href="#">98ASH00962A</a></li> <li>• <a href="#">98ARE10566D</a></li> <li>• <a href="#">98ASH00962A</a></li> </ul>

1. To find the associated resource, go to [freescale.com](http://freescale.com) and perform a search using Document ID



Figure 1 shows the functional modules in the chip.



**Figure 1. Functional block diagram**

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# 1 Ratings

## 1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

## General

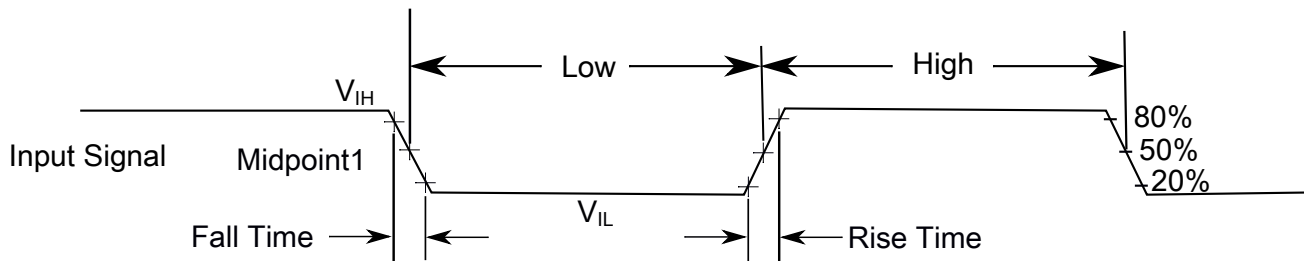
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	145	mA
$V_{DIO}$	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup>	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

### 2.2 Nonswitching electrical specifications

#### 2.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	

*Table continues on the next page...*

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> – V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	–0.1	0.1	V	
V <sub>SS</sub> – V <sub>SSA</sub>	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	–0.1	0.1	V	
V <sub>IH</sub>	Input high voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub>	—	V	
		0.75 × V <sub>DD</sub>	—	V	
V <sub>IL</sub>	Input low voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	—	0.35 × V <sub>DD</sub>	V	
		—	0.3 × V <sub>DD</sub>	V	
V <sub>HYS</sub>	Input hysteresis	0.06 × V <sub>DD</sub>	—	V	
I <sub>ICIO</sub>	Analog and I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> </ul>	-3	—	mA	1
I <sub>ICcont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> </ul>	-25	—	mA	
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	2
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	

1. All analog and I/O pins are internally clamped to V<sub>SS</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>IO\_MIN</sub> or greater than V<sub>IO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V<sub>IO\_MIN</sub>-V<sub>IN</sub>)/|I<sub>ICIO</sub>|.
2. Open drain outputs must be pulled to V<sub>DD</sub>.

## 2.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling V <sub>DD</sub> POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub> V <sub>LVW2H</sub> V <sub>LVW3H</sub> V <sub>LVW4H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	2.62	2.70	2.78	V	1
		2.72	2.80	2.88	V	
		2.82	2.90	2.98	V	
		2.92	3.00	3.08	V	

Table continues on the next page...



**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -5 mA	V <sub>DD</sub> - 0.5	—	—	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -2.5 mA	V <sub>DD</sub> - 0.5	—	—	V	
V <sub>OH</sub>	Output high voltage — High drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -20 mA	V <sub>DD</sub> - 0.5	—	—	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -10 mA	V <sub>DD</sub> - 0.5	—	—	V	
I <sub>OHT</sub>	Output high current total for all ports	—	—	100	mA	
V <sub>OL</sub>	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 2.5 mA	—	—	0.5	V	
V <sub>OL</sub>	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 10 mA	—	—	0.5	V	
V <sub>OL</sub>	Output low voltage — RESET_B					

Table continues on the next page...

**Table 3. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 3\text{ mA}$	—	—	0.5	V	
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 1.5\text{ mA}$	—	—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	$\mu\text{A}$	1, 2
	High drive port pins	—	0.004	0.5	$\mu\text{A}$	
$I_{IN}$	Input leakage current (total all pins) for full temperature range	—	—	1.0	$\mu\text{A}$	2
$R_{PU}$	Internal pullup resistors	20	—	50	$\text{k}\Omega$	3
$R_{PD}$	Internal pulldown resistors	20	—	50	$\text{k}\Omega$	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD}=3.6\text{V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$
4. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{DD}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz
- MCG mode: FEI

**Table 4. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	$\mu\text{s}$	1
	• $VLLS0 \rightarrow \text{RUN}$	—	—	135	$\mu\text{s}$	
	• $VLLS1 \rightarrow \text{RUN}$	—	—	135	$\mu\text{s}$	
	• $VLLS2 \rightarrow \text{RUN}$	—	—	75	$\mu\text{s}$	

Table continues on the next page...

**Table 4. Power mode transition operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS3 → RUN	—	—	75	μs	
	• VLPS → RUN	—	—	5.7	μs	
	• STOP → RUN	—	—	5.7	μs	

1. Normal boot (FTFA\_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 5. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_HSRUN</sub>	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	18.70 18.71	19.37 19.38	mA mA	2, 3, 4
I <sub>DD_HSRUN</sub>	High Speed Run mode current - all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	18.13 18.19	18.80 18.86	mA mA	4
I <sub>DD_HSRUN</sub>	High Speed Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V	— —	22.2 22.4	22.87 23.07	mA mA	5
I <sub>DD_RUN</sub>	Run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	12.74 12.82	13.41 13.49	mA mA	2, 3, 6

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_RUN</sub>	Run mode current in Compute operation — code executing from flash					
	@ 1.8V	—	12.10	13.10	mA	6
	@ 3.0V	—	12.20	13.37	mA	
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	12.8	13.47	mA	7
	@ 3.0V	—	12.9	13.57	mA	
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	14.8	15.47	mA	8
	@ 3.0V					
	• @ 25°C	—	14.9	15.57	mA	
	• @ 70°C	—	14.9	15.57	mA	
	• @ 85°C	—	14.9	15.57	mA	
	• @ 105°C	—	15.5	16.20	mA	
I <sub>DD_RUN</sub>	Run mode current — Compute operation, code executing from flash					
	@ 1.8V	—	12.1	12.77	mA	9
	@ 3.0V					
	• @ 25°C	—	12.2	12.87	mA	
	• @ 70°C	—	12.2	12.87	mA	
	• @ 85°C	—	12.2	12.87	mA	
	• @ 105°C	—	12.7	13.37	mA	
I <sub>DD_WAIT</sub>	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	5.5	6.17	mA	7
I <sub>DD_WAIT</sub>	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	3.5	4.17	mA	10
I <sub>DD_VLPR</sub>	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	0.58	0.86	mA	2, 11, 3
	@ 3.0V	—	0.59	0.87	mA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current in Compute operation, code executing from flash					
	@ 1.8V	—	0.47	0.75	mA	11
	@ 3.0V	—	0.47	0.75	mA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.62	0.90	mA	12

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.76	1.04	mA	13
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.28	0.56	mA	14
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	@ -40°C to 25°C	—	0.26	0.33	mA	
	@ 70°C	—	0.30	0.47	mA	
	@ 85°C	—	0.35	0.52	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	@ -40°C to 25°C	—	2.80	8.30	μA	
	@ 70°C	—	13.30	29.90	μA	
	@ 85°C	—	26.90	46.45	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	—	1.3	1.71	μA	
	@ 70°C	—	3.8	5.35	μA	
	@ 85°C	—	7.6	8.50	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	1.3	1.55	μA	
	@ 70°C	—	3.1	4.05	μA	
	@ 85°C	—	7.2	8.60	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	—	0.63	0.87	μA	
	@ 70°C	—	1.70	2.35	μA	
	@ 85°C	—	2.8	3.40	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.35	0.46	μA	
	@ 70°C	—	1.38	1.94	μA	
	@ 85°C	—	2.4	2.95	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.07	0.16	μA	
	@ 70°C	—	1.05	1.78	μA	
	@ 85°C	—	2.1	2.80	μA	

Table continues on the next page...



**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 105°C	—	6.9	8.25	μA	

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- Cache on and prefetch on, low compiler optimization
- CoreMark benchmark compiled using IAR 7.2 with optimization level low
- 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
- 100 MHz core and system clock, 50 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 72 MHz core and system clock, 36 MHz bus clock and 24 MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled. Compute operation.
- 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 72 MHz core and system clock, 36 MHz bus clock, and 24 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 72MHz core and system clock, 36MHz bus clock, and 24MHz flash clock. MCG configured for FEI mode. Compute operation.
- 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode.
- 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
- 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash.
- 4 MHz core, system, and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

**Table 6. Low power mode peripheral adders—typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHZ</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHZ</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>EREFSTEN4MHZ</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I <sub>EREFSTEN32KHZ</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	

Table continues on the next page...

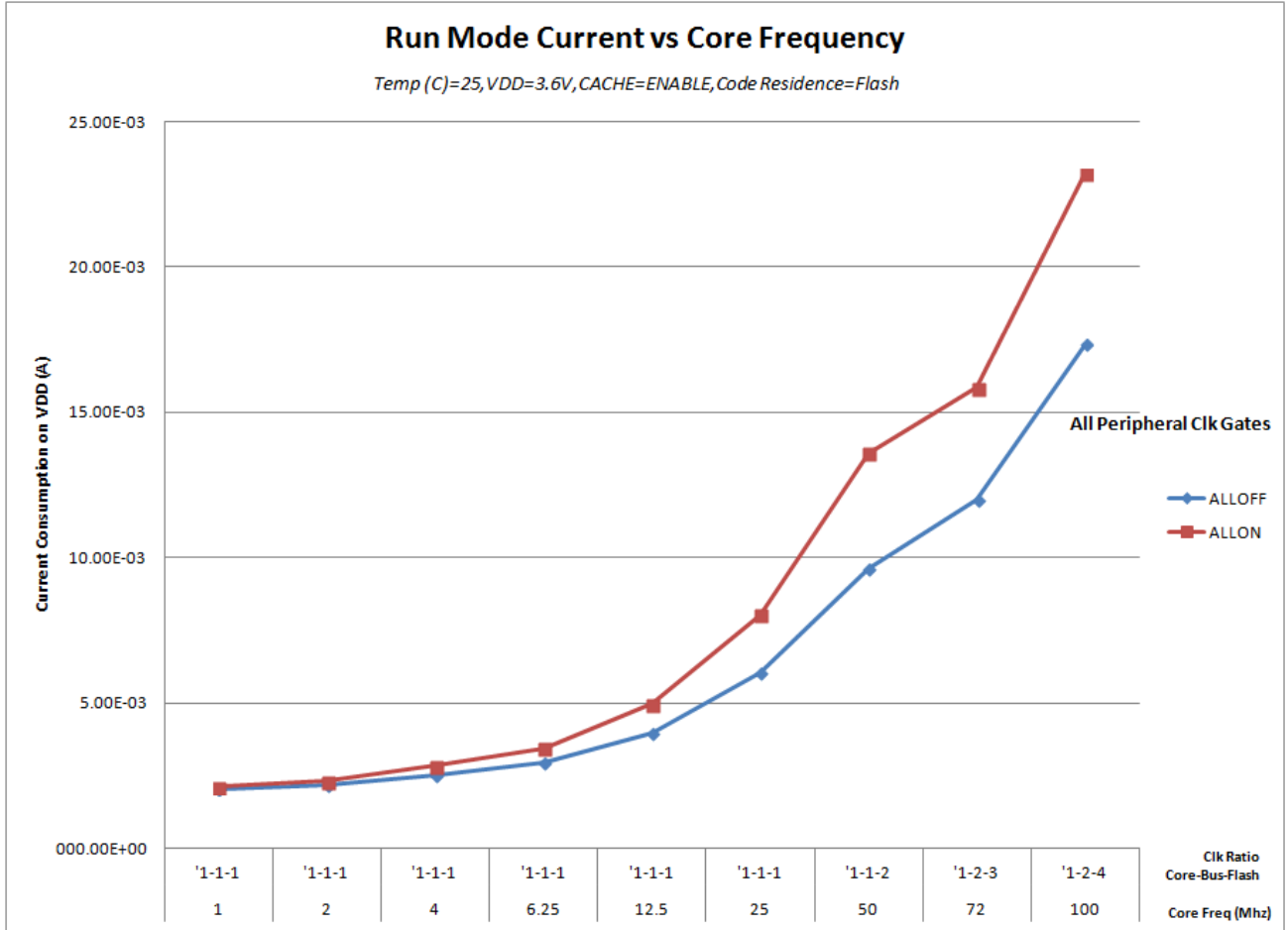
**Table 6. Low power mode peripheral adders—typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I <sub>48MIRC</sub>	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 3. Run mode supply current vs. core frequency**

General

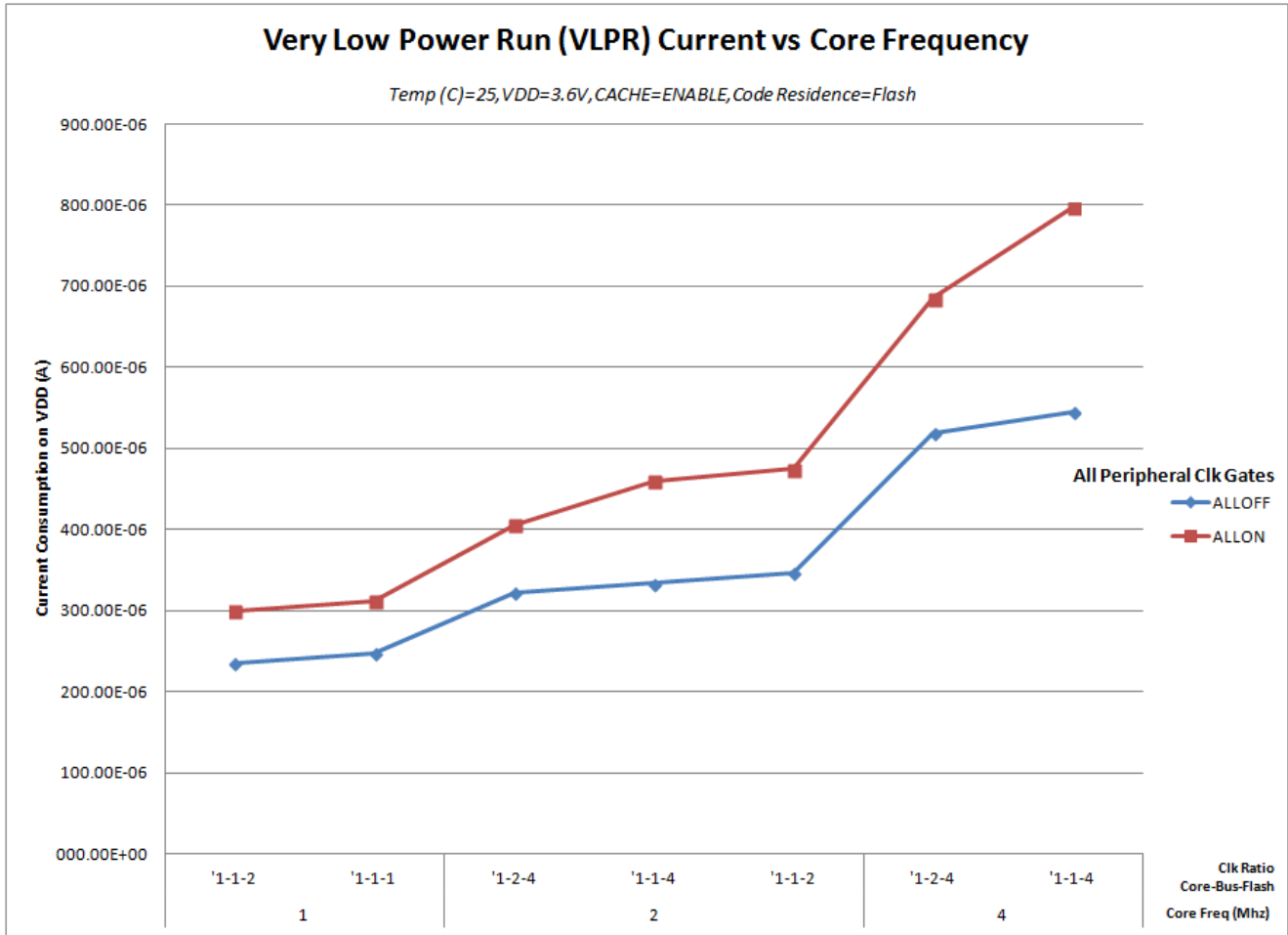


Figure 4. VLPR mode supply current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V <sub>EME</sub>	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltage: VDD = 3.3 V Temp = 25°C	FSYS = 100 MHz FBUS = 50 MHz External crystal = 10 MHz	150 kHz–50 MHz	11	dBuV	1, 2, 3
			50 MHz–150 MHz	12		
			150 MHz–500 MHz	11		
			500 MHz–1000 MHz	8		
		IEC level	N		4	

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MKV30F128VLH10.
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV .

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

**Table 9. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f <sub>SYS</sub>	System and core clock	—	100	MHz	
f <sub>BUS</sub>	Bus clock	—	50	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f <sub>SYS</sub>	System and core clock	—	72	MHz	
f <sub>BUS</sub>	Bus clock	—	50	MHz	
f <sub>FLASH</sub>	Flash clock	—	25	MHz	
f <sub>LPTMR</sub>	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	—	4	MHz	
f <sub>BUS</sub>	Bus clock	—	4	MHz	
f <sub>FLASH</sub>	Flash clock	—	1	MHz	
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	

*Table continues on the next page...*



**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$f_{LPTMR\_pin}$	LPTMR clock	—	25	MHz	
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Port rise and fall time				5
	<ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—			
		—	10	ns	
		—	5	ns	
		—			
		—	30	ns	
		—	16	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

## 2.4 Thermal specifications

## 2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>J</sub>	Die junction temperature	-40	125	°C	
T <sub>A</sub>	Ambient temperature	-40	105	°C	1

1. Maximum T<sub>A</sub> can be exceeded only if the user ensures that T<sub>J</sub> does not exceed maximum T<sub>J</sub>. The simplest method to determine T<sub>J</sub> is:  $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$ .

## 2.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	32 QFN	Unit	Notes
Single-layer (1s)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	66	79	97	°C/W	1
Four-layer (2s2p)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	48	55	33	°C/W	1
Single-layer (1s)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	54	67	81	°C/W	1
Four-layer (2s2p)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	41	49	28	°C/W	1
—	R <sub>θJB</sub>	Thermal resistance, junction to board	30	33	13	°C/W	2
—	R <sub>θJC</sub>	Thermal resistance, junction to case	17	23	2.0	°C/W	3

Table continues on the next page...

## Peripheral operating requirements and behaviors

Board type	Symbol	Description	64 LQFP	48 LQFP	32 QFN	Unit	Notes
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	3	5	6	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

#### 3.1.1 SWD electricals

Table 12. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>• Serial wire debug</li> </ul>	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>• Serial wire debug</li> </ul>	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

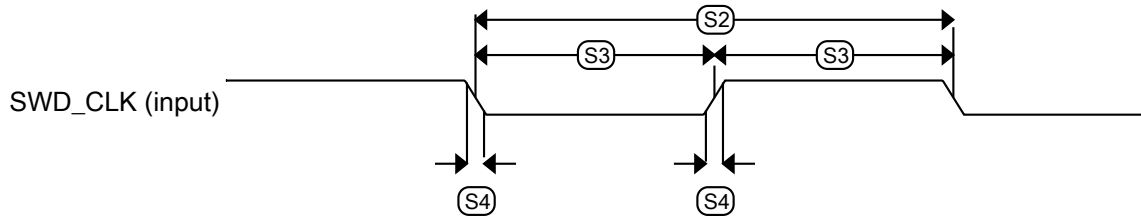


Figure 5. Serial wire clock input timing

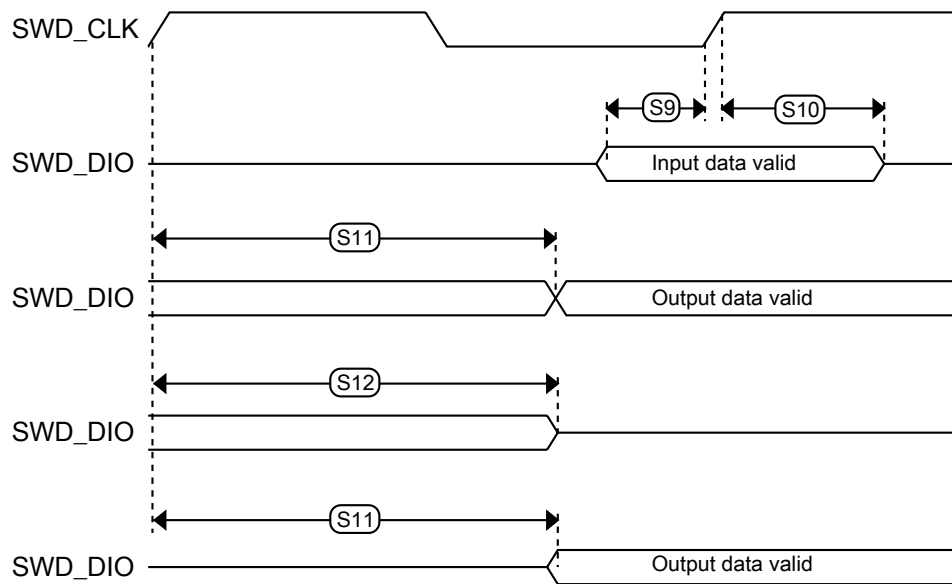


Figure 6. Serial wire data timing

### 3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> </ul>	0	10	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			

Table continues on the next page...

**Table 13. JTAG limited voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

**Table 14. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns



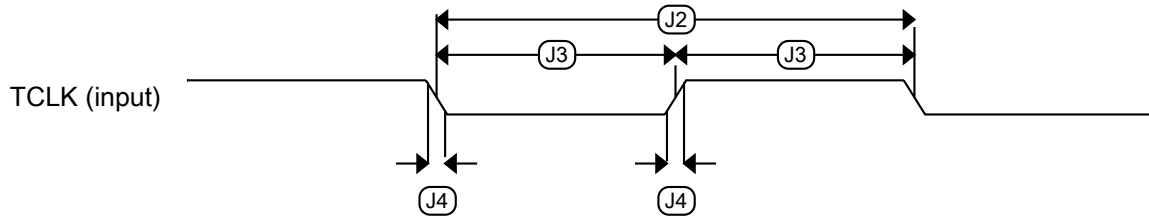


Figure 7. Test clock input timing

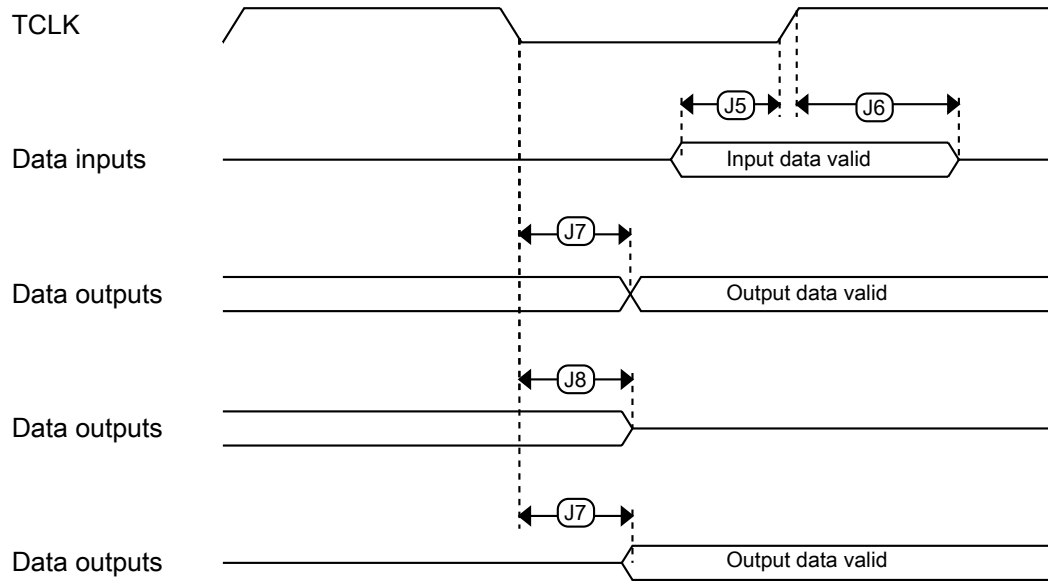
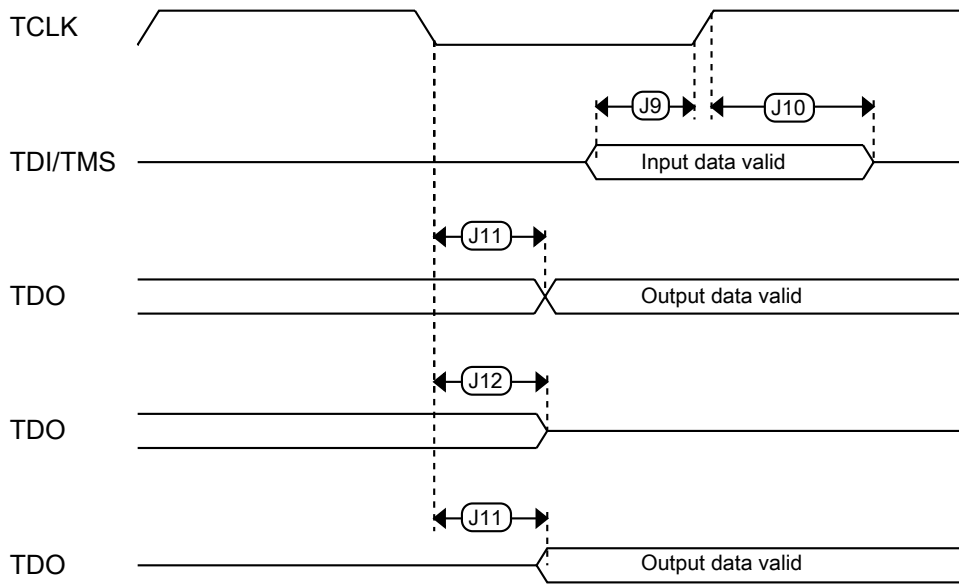
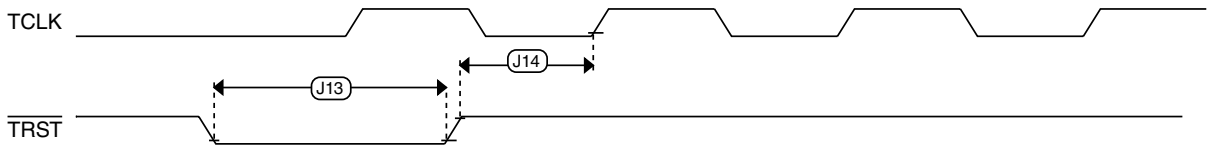


Figure 8. Boundary scan (JTAG) timing



**Figure 9. Test Access Port timing**



**Figure 10. TRST timing**

### 3.2 System modules

There are no specifications necessary for the device's system modules.

### 3.3 Clock modules

### 3.3.1 MCG specifications

**Table 15. MCG specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{\text{ints\_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
$\Delta f_{\text{ints\_t}}$	Total deviation of internal reference frequency (slow clock) over voltage and temperature	—	+0.5/-0.7	± 2	%		
$f_{\text{ints\_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{\text{dco}}$	1	
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 2	% $f_{\text{dco}}$	1, 2	
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1.5	% $f_{\text{dco}}$	1	
$f_{\text{intf\_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz		
$\Delta f_{\text{intf\_ft}}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C	—	+1/-2	± 5	% $f_{\text{intf\_ft}}$		
$f_{\text{intf\_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
$f_{\text{loc\_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints\_t}}$	—	—	kHz		
$f_{\text{loc\_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints\_t}}$	—	—	kHz		
FLL							
$f_{\text{fill\_ref}}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{\text{dco}}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{\text{fill\_ref}}$	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) $1280 \times f_{\text{fill\_ref}}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{\text{fill\_ref}}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{\text{fill\_ref}}$	80	83.89	100	MHz	
$f_{\text{dco\_t\_DMX3}_2}$	DCO output frequency	Low range (DRS=00) $732 \times f_{\text{fill\_ref}}$	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) $1464 \times f_{\text{fill\_ref}}$	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...