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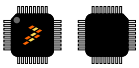
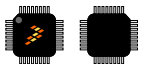
KV4x Data Sheet

168 MHz ARM Cortex-M4 core based Microcontroller with FPU

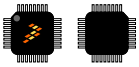
MKV46FxxxVLy16
MKV44FxxxVLy16
MKV42FxxxVLy16



100 LQFP
14 x 14 x 1.4 Pitch 0.5 mm



64 LQFP
10 x 10 x 1.4 Pitch 0.5 mm



48 LQFP
7 x 7 x 1.4 Pitch 0.5 mm

The Kinetis KV4x MCU family is a member of the Kinetis V series and provides a high-performance solution for motor control and Digital Power Conversion. Built upon the ARM® Cortex®-M4 core operating at up to 168 MHz with DSP and floating point unit, features include; dual 12-bit analog-to-digital converters with 240ns conversion time, up to 30 PWM channels for support of multi-motor systems, eFlexPWM module with 312 ps resolution for digital power conversion applications, programmable delay block, memory protection unit, dual FlexCAN modules and 64 to 256 KB of flash memory. KV4x MCUs are offered in 48LQFP, 64LQFP, and 100LQFP packages. All Kinetis V series MCUs are supported by a comprehensive enablement suite from NXP and third-party resources including reference designs, software libraries and motor configuration tools. KV4x MCUs are enabled to support Kinetis Motor Suite (KMS), a bundled hardware and software solution that enables rapid configuration of BLDC and PMSM motor drive systems.

Core

- ARM® Cortex®-M4 core up to 168 MHz with single precision Floating Point Unit (FPU)

Memories

- Up to 256 KB of program flash memory
- Up to 32 KB of RAM

System peripherals

- 16-channel DMA controller
- Low-leakage wakeup unit
- SWD interface and Micro Trace buffer
- Advanced independent clocked watchdog

Clocks

- 32 to 40 kHz or 3 to 32 MHz crystal oscillator
- Multipurpose clock generator (MCG) with frequency-locked loop and phase-locked loop referencing either internal or external reference clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Human-machine interface

- General-purpose input/output

Communication interfaces

- Two Universal Asynchronous Receiver/Transmitter (UART) / FlexSCI modules with programmable 8- or 9-bit data format
- One 16-bit SPI module
- One I2C module
- Two FlexCAN modules

Analog Modules

- Two 12-bit cyclic ADCs
- Four analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- One 12-bit DAC

Timers

- One eFlexPWM with 4 sub-modules, providing 12 PWM outputs
- Two 8-channel FlexTimers (FTM0 and FTM3)
- One 2-channel FlexTimers (FTM1)
- Four Periodic interrupt timers (PIT)
- Two Programmable Delay Blocks (PDB)
- Quadrature Encoder/Decoder (ENC)
- Ratio of timer input clock frequency vs. core frequency is 1:2 when core frequency is 168 Mhz, and 1:1 when core frequency is less than or equal to 100 Mhz

Kinetis Motor Suite

- Supports velocity and position control of BLDC and PMSM motors
- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

Security and integrity modules

- Hardware CRC module to support fast cyclic redundancy checks
- External Watchdog Monitor (EWM)

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Orderable part numbers summary[1]

NXP part number	CPU frequency (MHz)	Pin count	Total flash memory (KB)	SRAM (KB)	ADC		eFlexPWM		PWM Nano-Edge	Flex Timers			DAC	FlexCAN	
					ADCA	ADCB	PWMA PWMB	PWMX		FTM0	FTM3	FTM1		CAN0	CAN1
MKV46F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV44F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLF16[2]	168	48	128	24	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV44F64VLH16	168	64	64	16	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F64VLF16[2]	168	48	64	16	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV42F256VLL16	168	100	256	32	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F256VLH16	168	64	256	32	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F128VLL16	168	100	128	24	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1

Table continues on the next page...

Orderable part numbers summary[1] (continued)

NXP part number	CPU frequency (MHz)	Pin count	Total flash memory (KB)	SRAM (KB)	ADC		eFlexPWM		PWM Nano-Edge	Flex Timers			DAC	FlexCAN	
					ADCA	ADCB	PWMA PWMB	PWMX		FTM0	FTM3	FTM1		CAN0	CAN1
MKV42F128VLH16	168	64	128	24	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F128VLF16[2]	168	48	128	24	11ch	10ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	—
MKV42F64VLH16	168	64	64	16	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F64VLF16[2]	168	48	64	16	11ch	10ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	—

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.
2. Package Your Way.

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV4XP100M168RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KV4XP100M168[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_V_1N72K[1]
KMS User Guide	The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution.	Kinetis Motor Suite User's Guide (KMS100UG)[1]
KMS API Reference Manual	The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks.	Kinetis Motor Suite API Reference Manual (KMS100RM)[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 100-pin: 98ASS23308W[1] • LQFP 64-pin: 98ASS23234W[1] • LQFP 48-pin: 98ASH00962A[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

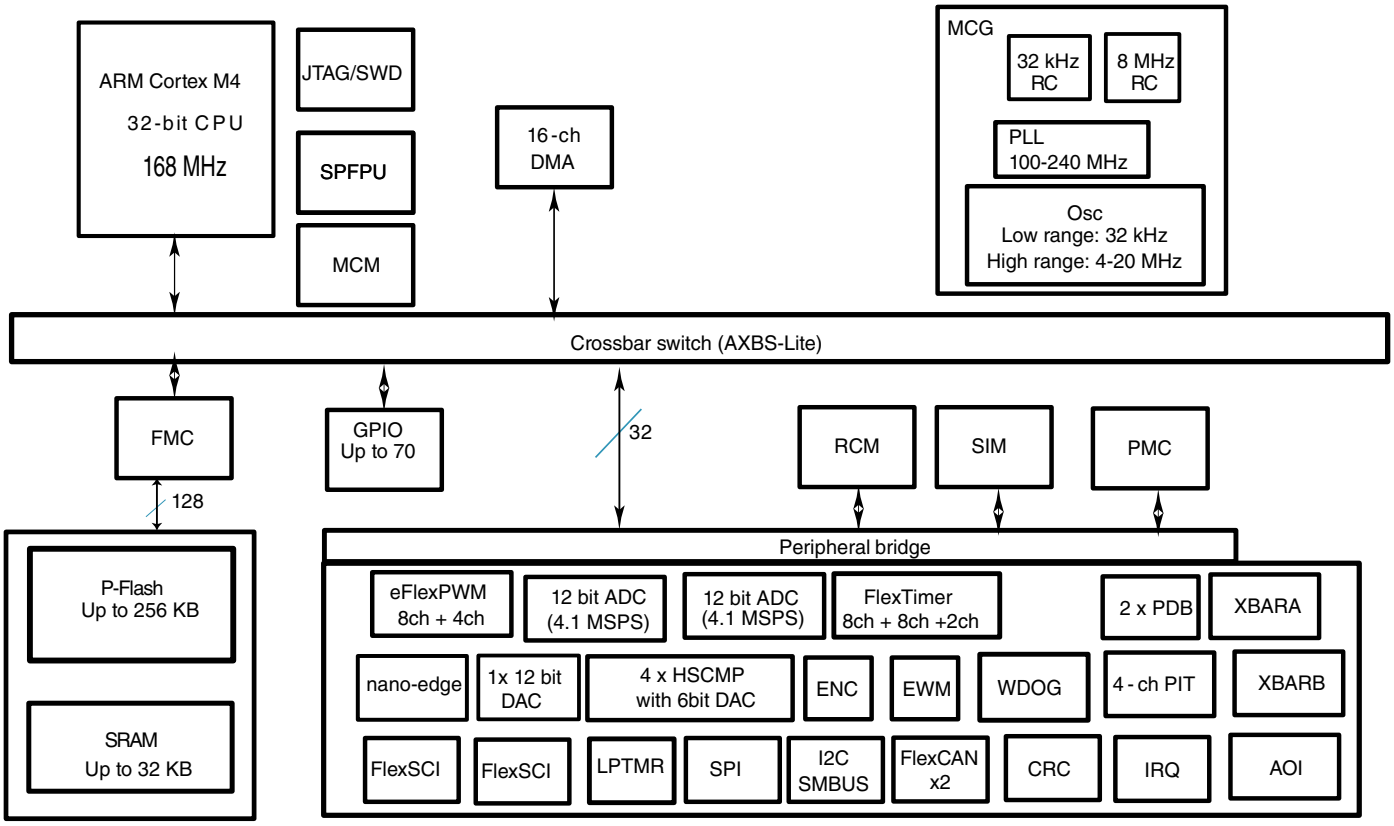


Figure 1. KV4x block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	–0.3	VDD + 0.3[1]	V
	Open drain pins (PTC6 and PTC7)	–0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 1. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Symbol	Description	Notes[1]	Min	Max	Unit
V_{DD}	Supply Voltage Range		-0.3	4.0	V
V_{DDA}	Analog Supply Voltage Range		-0.3	4.0	V
V_{REFHx}	ADC High Voltage Reference		-0.3	4.0	V
V_{REFLx}	ADC Low Voltage Reference		-0.3	0.3	V
ΔV_{DD}	Voltage difference V_{DD} to V_{DDA}		-0.3	0.3	V
ΔV_{SS}	Voltage difference V_{SS} to V_{SSA}		-0.3	0.3	V
V_{IN}	Digital Input Voltage Range	Pin Groups 1, 2	-0.3	4.0	V
V_{OSC}	Oscillator Input Voltage Range	Pin Group 4	-0.4	4.0	V
V_{INA}	Analog Input Voltage Range	Pin Group 3	-0.3	4.0	V
I_{IC}	Input clamp current, per pin (V_{IN} < 0)		—	-20.0	mA
I_{OC}	Output clamp current, per pin (V_O < 0)[2]		—	-20.0	mA
V_{OUT}	Output Voltage Range (Normal Push-Pull mode)	Pin Group 1	-0.3	4.0	V
V_{OUTOD}	Output Voltage Range (Open Drain mode)	Pin Group 2	-0.3	5.5	V
V_{OUT_DAC}	DAC Output Voltage Range	Pin Group 5	-0.3	4.0	V
T_A	Ambient Temperature Industrial		-40	105	°C
T_{STG}	Storage Temperature Range (Extended Industrial)		-55	150	°C

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$, PORTC6, and PORTC7
   - Pin Group 3: ADC and Comparator Analog Inputs

- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. Continuous clamp current per pin is -2.0 mA

2 General

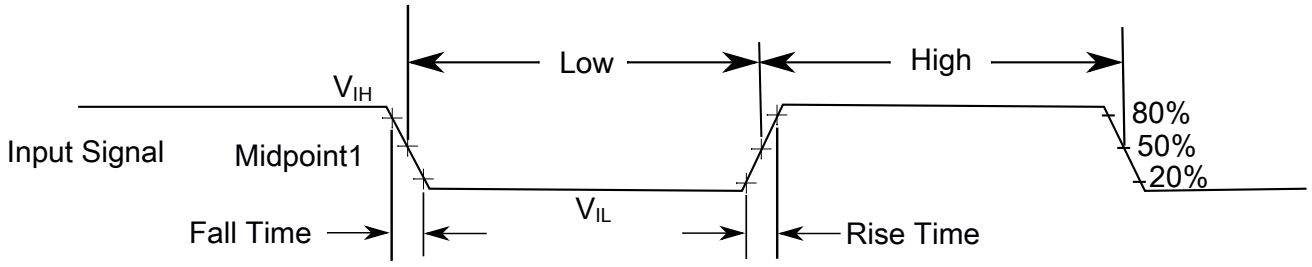
Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on nxp.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Recommended Operating Conditions

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 2. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Symbol	Description	Notes[1]	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Digital	2, 3	1.71		3.6	V
V_{DDA}	Supply voltage (analog)	2, 3	2.7	3.0	3.6	V
V_{REFHx}	ADC (Cyclic) Reference Voltage High		2.7		V_{DDA}	V
ΔVDD	Voltage difference V_{DD} to V_{DDA}		-0.1	0	0.1	V
ΔVSS	Voltage difference V_{SS} to V_{SSA}		-0.1	0	0.1	V
F_MCGOUT	Device Clock Frequency • using internal RC oscillator • using external clock source		0.04 0		168 168	MHz
V_{IH}	Input Voltage High (digital inputs)	Pin Groups 1, 2	0.7 x V_{DD}		3.6	V
V_{IL}	Input Voltage Low (digital inputs)	Pin Groups 1, 2			0.35 x V_{DD}	V
V_{IHOSC}	Oscillator Input Voltage High XTAL driven by an external clock source	Pin Group 4	2.0		V_{DD} + 0.3	V
V_{ILOSC}	Oscillator Input Voltage Low	Pin Group 4	-0.3		0.8	V
C_{out}	DAC Output Current Drive Strength	Pin Group 5			1	mA
T_A	Ambient Operating Temperature		-40		105	°C

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
   - Pin Group 6: PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. have high output current capability
   - Pin Group 7: PTC6 and PTC7 are true open drain pins and have no P-chanl transistor. A external pull-up resistor is required when these pins are outputs.

2. If the ADC is enabled, minimum V_{DD} is 2.7 V and minimum V_{DDA} is 2.7 V. ADCA and ADCB are not guaranteed to operate below 2.7 V. All other analog modules besides the ADC and Nano-edge will operate down to 1.71 V.
3. If the Nano-edge is enabled, minimum V_{DD} is 3.0 V and minimum V_{DDA} is 3.0 V. Nano-edge is not guaranteed to operate below 3.0 V. All other analog modules besides the ADC and Nano-edge will operate down to 1.71 V.

2.2.2 LVD and POR operating requirements

Table 3. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad					
		V_{DD} – 0.5	—	—	V	
		V_{DD} – 0.5	—	—	V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤V_{DD} ≤ 2.7 V, I_{OH} = -5mA					
	Output high voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 — —	 V V	1
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — open drain pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 3 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 1 mA	— —	— —	0.5 0.5	V V	2
V_{OL}	Output low voltage — normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	— —	— —	0.5 0.5	V V	
	Output low voltage — high drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	— —	— —	0.5 0.5	V V	1
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current, analog and digital pins • V_{SS} ≤ V_{IN} ≤ V_{DD}	—	0.002	0.5	µA	3
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	kΩ	4
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	5

1. High drive pads are PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6 and PTD7.
2. Open drain pads are PTC6 and PTC7.
3. Measured at VDD=3.6V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
5. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	—	173	µs	
	• VLLS1 → RUN	—	—	172	µs	
	• VLLS2 → RUN	—	—	96	µs	
	• VLLS3 → RUN	—	—	96	µs	
	• VLPS → RUN	—	—	5.4	µs	
	• STOP → RUN	—	—	5.4	µs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3σ)

Table 6. Power consumption operating behaviors (All IDDs are Target values)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 25 MHz.
	• @ 1.8V	—	6.8	17.2	mA	
	• @ 3.0V	—	6.9	17.4	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 50 MHz.
	• @ 1.8V • @ 3.0V	—	9.9	19.7	mA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		—	10.0	19.8	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 100 MHz.
	• @ 1.8V	—	17.0	25.9	mA	
	• @ 3.0V	—	17.2	26.1	mA	
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 168 MHz.
	• @ 1.8V	—	26.3	45.3	mA	
	• @ 3.0V	—	26.5	45.5	mA	
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash,excludes IDDA					Core frequency of 168 MHz. Nanoedge module at 84 MHz.
	• @ 3.0V					
	• @ 25°C	—	34.0	45.5	mA	
	• @ 105°C	—	39.0	53.2	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	8.9	—	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.58	—	mA	Core frequency of 4 Mhz.
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.83	—	mA	Core frequency of 4 Mhz.
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.34	—	mA	Bus frequency of 2 MHz.
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.43	2.03	mA	
	• @ 70°C	—	1.16	4.27	mA	
	• @ 105°C	—	3.05	10.13	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	58	218	µA	
	• @ 70°C	—	280	1340	µA	
	• @ 105°C	—	924	2870	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	2.8	5.3	µA	
	• @ 70°C	—	9.6	35.1	µA	
	• @ 105°C	—	37.4	134.8	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25°C	—	2.7	3.3	µA	
	• @ 70°C	—	6.6	12.2	µA	
	• @ 105°C	—	25.9	50.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	740	1200	nA	
	• @ 70°C	—	2.5	10.6	µA	
	• @ 105°C	—	11.1	26.5	µA	
I_{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	420	832	nA	
	• @ 70°C	—	1.9	9.4	µA	
	• @ 105°C	—	10.8	26.3	µA	
I_{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	200	599	nA	
	• @ 70°C	—	1.8	10.5	µA	
	• @ 105°C	—	10.8	26.3	µA	

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	VLPS	440	490	540	560	570	580	
	STOP	510	560	560	560	610	680	

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
		510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

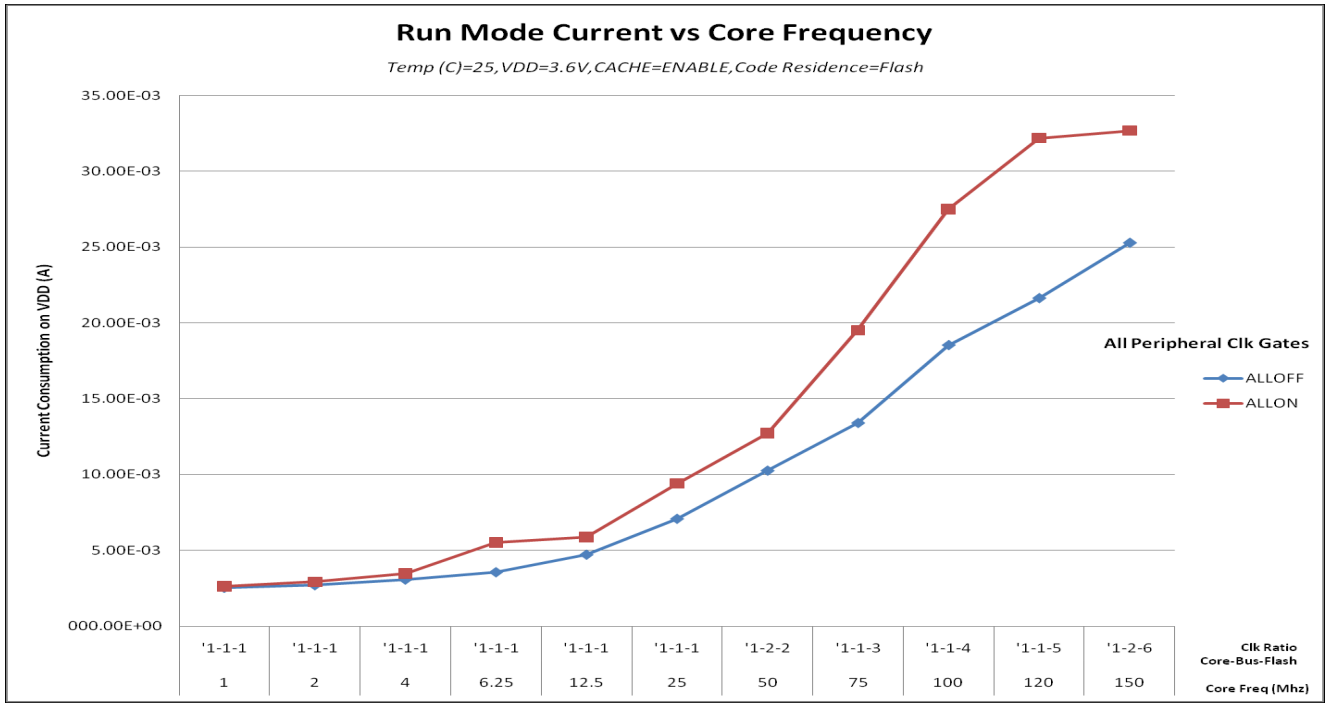


Figure 3. Run mode supply current vs. core frequency

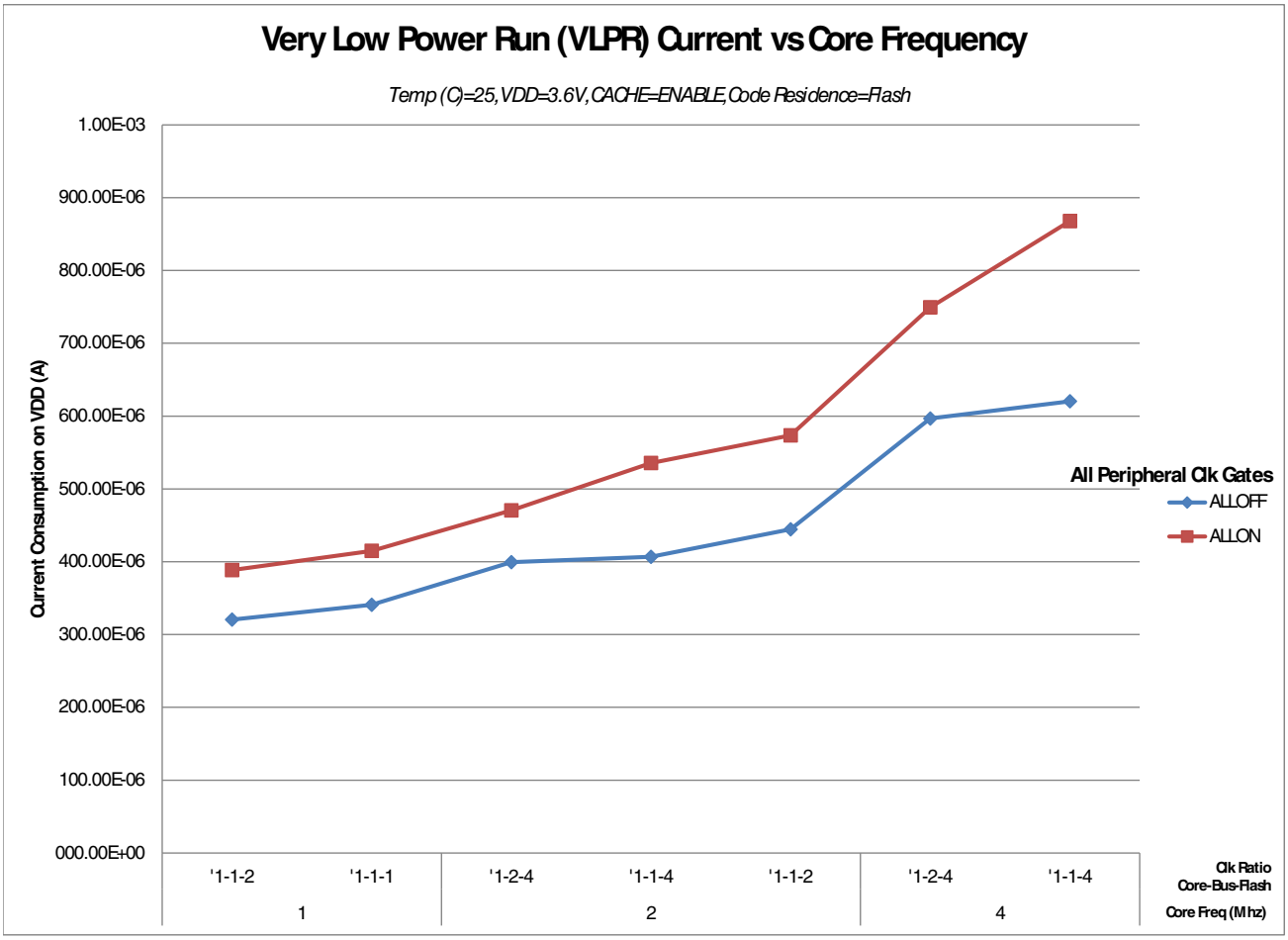


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

NOTE

EMC measurements to IC-level IEC standards are available from NXP on request.

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	18	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	14	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	8	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Typical device clock specifications

Table 10. Typical device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus and Flash clock	—	24	MHz	
f_{FPCK}	Fast peripheral clock	—	84	MHz	
f_{NANO}	Nano-edge clock	—	168	MHz	
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	

Table continues on the next page...

Table 10. Typical device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FPCK}	Fast peripheral clock	—	100	MHz	
f_{NANO}	Nano-edge clock	—	200	MHz	
Low Speed RUN mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	
f_{FPCK}	Fast peripheral clock	—	100	MHz	
f_{NANO}	Nano-edge clock	—	200	MHz	

NOTE

When NaneEdge circuit is enabled, the following clock set must be followed:

1. NanoEdge clock source must be from the PLL output
2. NanoEdge clock must be 2x the fast peripheral clock
3. NanoEdge clock must in the range of 164 Mhz ~232 Mhz

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 25 15	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	48 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	62	64	71	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	49	46	47	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	58	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	39	41	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	24	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	15	18	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.

4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 14. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	 20	 —	 ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

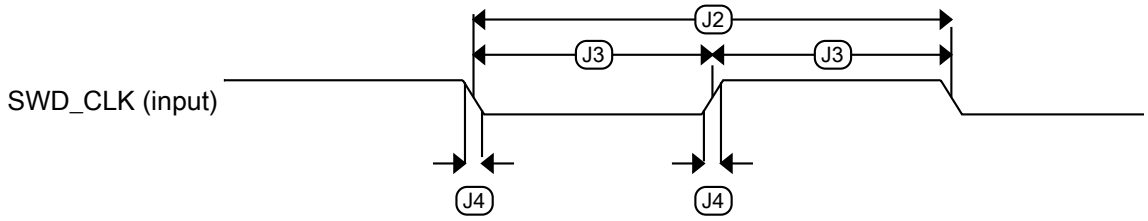


Figure 5. Serial wire clock input timing

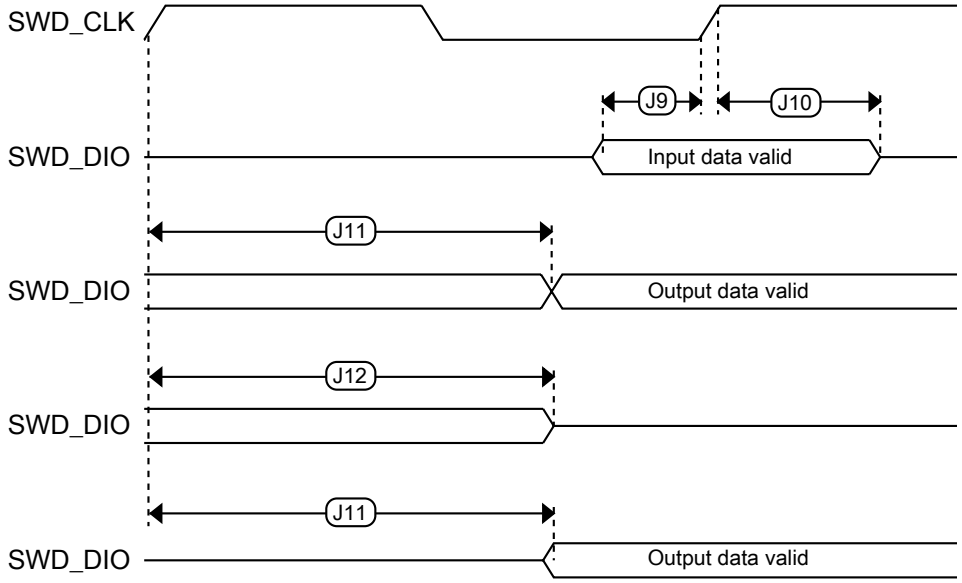


Figure 6. Serial wire data timing

3.1.2 Debug trace timing specifications

Table 15. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	1.5	ns
T_h	Data hold	2	1.0	ns

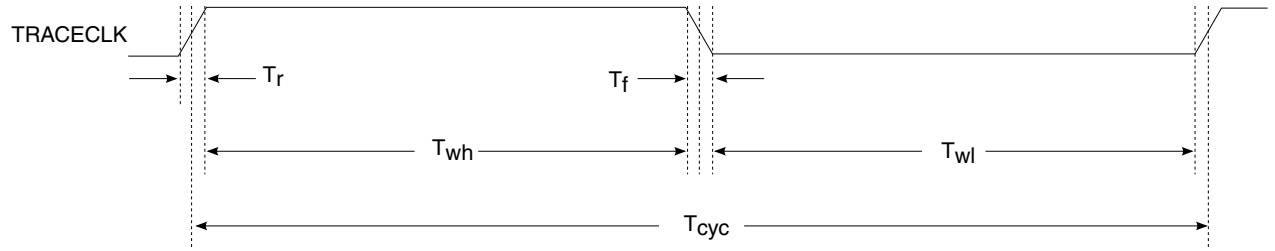


Figure 7. TRACE_CLKOUT specifications

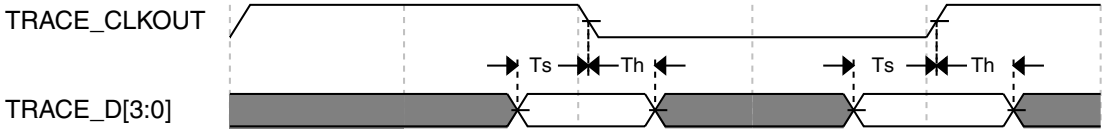


Figure 8. Trace data specifications

3.1.3 JTAG electricals

Table 16. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 16. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 17. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

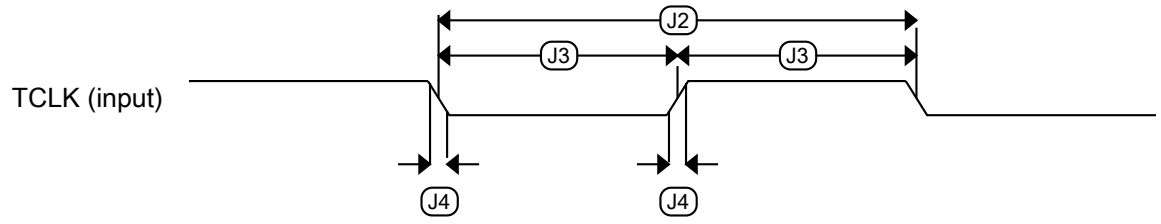


Figure 9. Test clock input timing

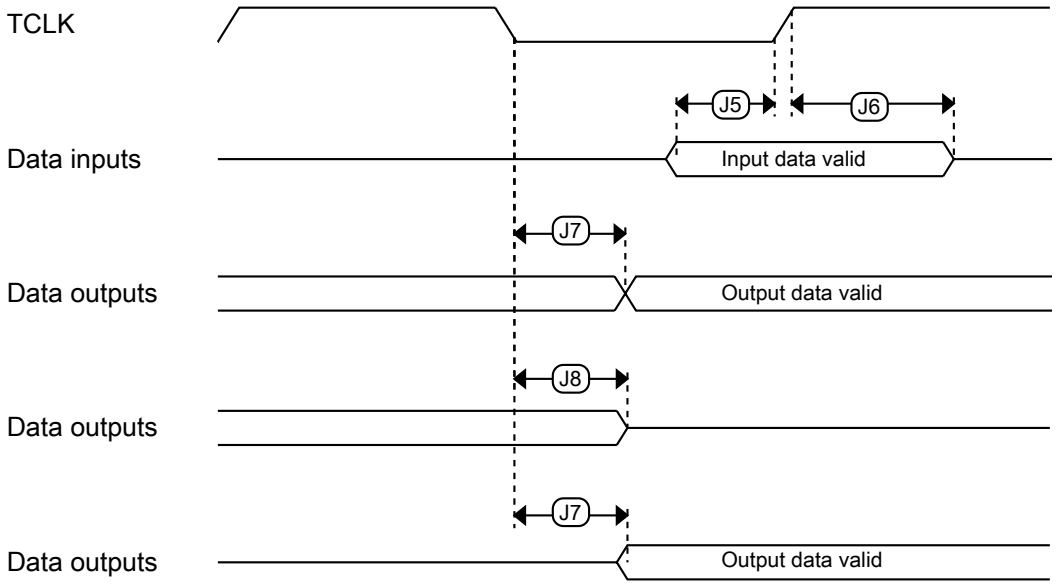


Figure 10. Boundary scan (JTAG) timing

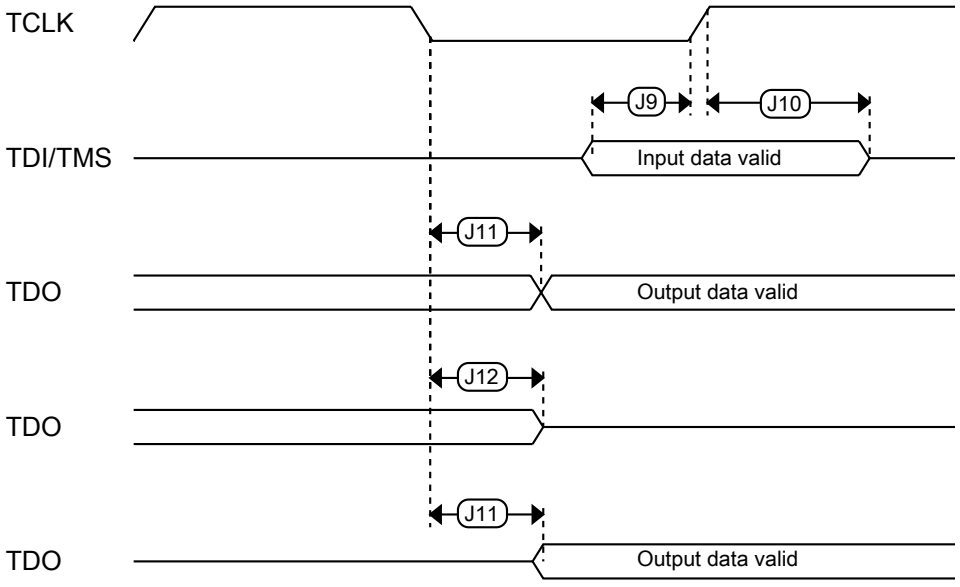


Figure 11. Test Access Port timing