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MKW2xD Data Sheet

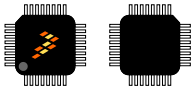
Supports MKW24D512V, MKW22D512V, MKW21D512V, and MKW21D256V Products

MKW2xDxxxVHA5

The MKW2xD is a low power, compact integrated device consisting of:

- A high-performance 2.4 GHz IEEE 802.15.4 compliant radio transceiver
- A powerful ARM Cortex-M4 MCU system with connectivity
- Precision mixed signal analog peripherals

The MKW2xD family of devices are used to easily enable connectivity based on the IEEE 802.15.4 Standard.



64 LQFP
8.0x8.0x0.91 mm P 0.5 mm

Core Processor and Memories

- 50 MHz Cortex-M4 CPU with DSP capabilities
- Up to 512 KB of flash memory
- Up to 64 KB of SRAM

Typical Applications

- Smart Energy 1.x
- ZigBee Home Automation
- ZigBee Healthcare
- ZigBee RF4CE
- ZigBee Light Link
- Thread
- Home Area Networks consisting of
  - Meters
  - Gateways
  - In-home displays
  - Connected appliances
- Networked Building Control and Home Automations with
  - Lighting Control
  - HVAC
  - Security

Peripherals

- USB
- Cryptographic Acceleration
- 16-bit ADC
- 12-bit DAC
- Flexible timers

Radio transceiver performance

- Up to –102 dBm receiver sensitivity
- +8 dBm maximum transmit output power
- Up to 58 dBm channel rejection
- Current consumption is minimized with peak transmit current of 17 mA at 0 dBm output power, and peak receive current of 15 mA in Low Power Preamble Search mode.

Package and Operating Characteristics

- Packaged in an 8 x 8 mm LGA with 56 contacts
- Voltage range: 1.8 V to 3.6 V
- Ambient temperature range: –40°C to 105°C

Ordering Information

Device	Operating Temp Range (T_A)	Package	Memory Options	Description
MKW21D256VHA5(R)	-40 to 105°C	8x8 LGA (R: tape and reel)	32 KB SRAM, 256 KB flash	Additional FlexMemory with up to 64 KB FlexNVM and up to 4 KB FlexRAM. No USB.
MKW21D512VHA5(R)	-40 to 105°C	8x8 LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports higher memory option and additional GPIO. No USB. No FlexNVM or FlexRAM.
MKW22D512VHA5(R)	-40 to 105°C	8x8 LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports full speed USB 2.0. No FlexNVM or FlexRAM.
MKW24D512VHA5(R)	-40 to 105°C	8x8 LGA (R: tape and reel)	64 KB SRAM, 512 KB flash	Supports Smart Energy 2.0 and full-speed USB 2.0. No FlexNVM or FlexRAM.

Related Resources

Type	Description	Resource
Selector Guide	The Kinetis MCUs Product Selector is a web-based tool that features interactive application wizards and a dynamic product selector.	Product Selector
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	KW2X Fact Sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MKW2xDRM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Package drawing	Package dimensions are provided in package drawings.	98ASA00393D[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

Table of Contents

1 Features

This section provides a simplified block diagram and highlights the device features.

1.1 Block diagram

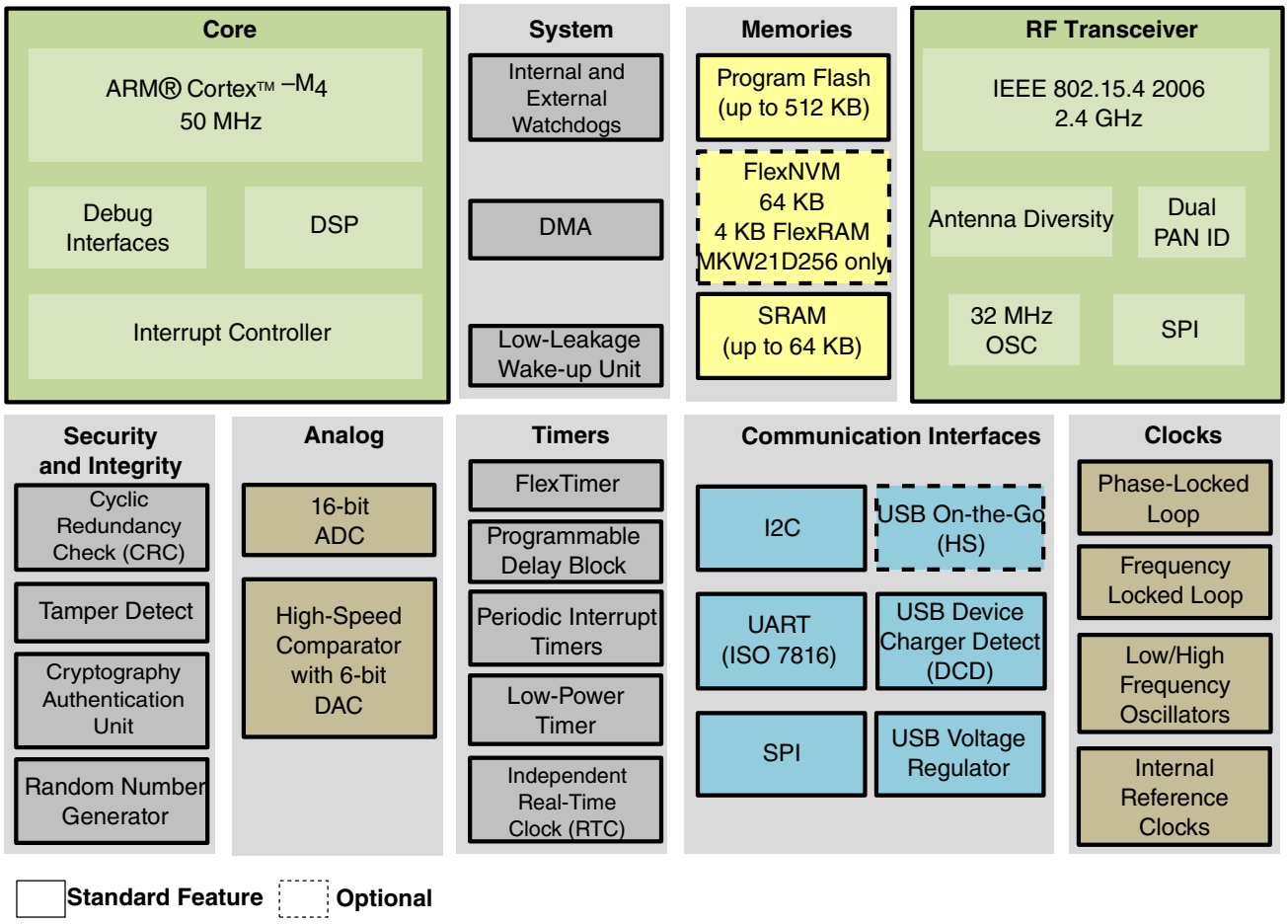


Figure 1. MKW2xD simplified block diagram

1.2 Radio features

- Fully compliant 802.15.4 Standard transceiver supports 250 kbps data rate with O-QPSK modulation in 5.0 MHz channels with direct sequence spread-spectrum (DSSS) encode and decode

- Operates on one of 16 selectable channels in the 2.4 GHz frequency ISM band
- Programmable output power
- Supports 2.36 to 2.4 GHz Medical Band (MBAN) frequencies with same modulation as IEEE 802.15.4
- Hardware acceleration for IEEE® 802.15.4 2006 packet processing
    - Random number generator
    - Support for dual PAN mode
- 32 MHz crystal reference oscillator with on board trim capability to supplement external load capacitors
- Programmable frequency clock output (CLK_OUT)
- Control port for Antenna Diversity mode
- Clocks
    - 32 MHz crystal oscillator
    - Internal 1 kHz low power oscillator
    - DC to 32 MHz external square wave input clock
- Small RF footprint
    - Differential input/output port used with external balun
    - Integrated transmit/receive switch
    - Supports single ended and antenna diversity options
    - Low external components count
    - Supports external PA and LNA

1.3 Microcontroller features

- Core:
    - ARM Cortex-M4 Core at 50 MHz (1.25 MIPS/MHz)
    - Supports DSP instructions

    - Nested vectored interrupt controller (NVIC)
    - Asynchronous wake-up interrupt controller (AWIC)
    - Debug and trace capability
    - 2-pin serial wire debug (SWD)
    - IEEE 1149.1 Joint Test Action Group (JTAG)
    - IEEE 1149.7 compact JTAG (cJTAG)
    - Trace port interface unit (TPIU)
    - Flash patch and breakpoint (FPB)
    - Data watchpoint and trace (DWT)
    - Instrumentation trace macrocell (ITM)
    - Enhanced trace macrocell (ETM)
- System and power management:
    - Software and hardware watchdog with external monitor pin
    - DMA controller with 16 channels
    - Low-leakage wake-up unit (LLWU)
    - Power management controller with 10 different power modes
    - Non-maskable interrupt (NMI)
    - 128-bit unique identification (ID) number per chip
- Memories and memory interfaces:
    - Up to 512 KB Program Flash
    - Up to 64 KB of SRAM
    - In MKW21D256, FlexMemory with up to 64 KB FlexNVM and up to 4 KB FlexRAM can be partitioned.
    - EEPROM has endurance of 10 million cycles over full voltage and temperature range and read-while-write capability
    - Flash security and protection features
    - Serial flash programming interface (EzPort)

- Clocks
  - Multi-purpose clock generator
    - PLL and FLL operation
    - Internal reference clocks (32 kHz or 2 MHz)
  - Three separate crystal oscillators
    - 3 MHz to 32 MHz crystal oscillator for MCU
    - 32 kHz to 40 kHz crystal oscillator for MCU or RTC
    - 32 MHz crystal oscillator for Radio
  - Internal 1 kHz low power oscillator
  - DC to 50 MHz external square wave input clock
- Security and integrity
  - Hardware CRC module to support fast cyclic redundancy checks
  - Tamper detect and secure storage
  - Hardware random-number generator
  - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
  - 128-bit unique identification (ID) number per chip
- Analog
  - 16-bit SAR ADC
  - High-speed Analog comparator (CMP) with 6-bit DAC
- Timers
  - Up to 12 channels; 7 channels support external connections; 5 channels are internal only
  - Carrier modulator timer (CMT)
  - Programmable delay block (PDB)
  - 1x4ch programmable interrupt timer (PIT)

    - Low-power timer (LPT)
    - FlexTimers that support general-purpose PWM for motor control functions
- Communications
    - One SPI
    - Two I^2C with SMBUS support
    - Three UARTs (w/ ISO7816, IrDA, and hardware flow control)
    - One USB On-The-Go Full Speed
- Human-machine interface
    - GPIO with pin interrupt support, DMA request capability, digital glitch filter, and other pin control options
- Operating characteristics
    - Voltage range 1.8 V - 3.6 V
    - Flash memory programming down to 1.8 V
    - Temperature range (TA) -40 to 105°C

2 Transceiver description

2.1 Key specifications

MKW2xD meets or exceeds all IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specifications for MKW2xD are:

- ISM band:
    - RF operating frequency: 2405 MHz to 2480 MHz (center frequency range)
    - 5 MHz channel spacing
- MBAN band:
    - RF operating frequency: 2360 MHz to 2400 MHz (center frequency range)
    - MBAN channel page 9 is (2360 MHz-2390 MHz band)

        - Fc = 2363.0 + 1.0 * k in MHz for k = 0, 1, 2, ...26
    - MBAN channel page 10 is (2390 MHz-2400 MHz band)
        - Fc = 2390.0 + 1.0 * k in MHz for k = 0, 1, 2, ...8
- IEEE 802.15.4 Standard 2.4 GHz modulation scheme
    - Chip rate: 2000 kbps
    - Data rate: 250 kbps
    - Symbol rate: 62.5 kbps
    - Modulation: OQPSK
- Receiver sensitivity: -102 dBm, typical (@1% PER for 20 byte payload packet)
- Differential bidirectional RF input/output port with integrated transmit/receive switch
- Programmable output power from -35 dBm to +8 dBm.

2.2 RF interface and usage

The MKW2xD RF output ports are bidirectional (diplexed between receive/transmit modes) and differential enabling interfaces with numerous off-chip devices such as a balun. When using a balun, this device provides an interface to directly connect between a single-ended antenna and the MKW2xD RF ports. In addition, MKW2xD provides four output driver ports that can have both drive strength and slew rate configured to control external peripheral devices. These signals designated as ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH when enabled are switched via an internal hardware state machine. These ports provide control features for peripheral devices such as:

- Antenna diversity modules
- External PAs
- External LNAs
- T/R switches

2.2.1 Clock output feature

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from the reference 32 MHz (see Table 2). The CLK_OUT pin will be enabled upon POR. The frequency CLK_OUT default to 4 MHz (32 MHz/8).

2.3 Transceiver functions

2.3.1 Receive

The receiver has the functionality to operate in either normal run state or low power run state that can be considered as a partial power down mode. Low power run state can save a considerable amount of current by duty-cycling some sections of the receiver lineup during preamble search and is referred to as Low Power Preamble Search mode (LPPS).

The radio receiver path is based upon a near zero IF (NZIF) architecture incorporating front end amplification, one mixed signal down conversion to IF that is programmably filtered, demodulated and digitally processed. The RF front end (FE) input port is differential that shares the same off chip matching network with the transmit path.

2.3.2 Transmit

MKW2xD transmits OQPSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RFOUTP, RFOUTN) are converted as single ended (SE) signals with off chip components as required.

2.3.3 Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)

The MKW2xD supports three clear channel assessment (CCA) modes of operation including energy detection (ED) and link quality indicator (LQI). Functionality for each of these modes is as follows.

2.3.3.1 CCA mode 1

CCA mode 1 has two functions:

- To estimate the energy in the received baseband signal. This energy is estimated based on receiver signal strength indicator (RSSI).
- To determine whether the energy is greater than a set threshold.

The estimate of the energy can also be used as the Link Quality metric. In CCA Mode 1, the MKW2xD must warm up from Idle to Receive mode where RSSI averaging takes place.

2.3.3.2 CCA mode 2

CCA mode 2 detects whether there is any 802.15.4 signal transmitting in the frequency band that an 802.15.4 transmitter intends to transmit. From the definition of CCA mode 2 in the 802.15.4 standard, the requirement is to detect an 802.15.4 complied signal. Whether the detected energy is strong or not is not important for CCA mode 2.

2.3.3.3 CCA mode 3

CCA mode 3 as defined by 802.15.4 standard is implemented using a logical combination of CCA mode 1 and CCA mode 2. Specifically, CCA mode 3 operates in one of two operating modes:

- CCA mode 3 is asserted if both CCA mode 1 and CCA mode 2 are asserted.
- CCA mode 3 is asserted if either CCA mode 1 or CCA mode 2 is asserted.

This mode setting is available through a programmable register.

2.3.3.4 Energy detection (ED)

Energy detection (ED) is based on receiver signal strength indicator (RSSI) and correlator output for the 802.15.4 standard. ED is an average value of signal strength. The magnitude from this measurement is calculated from the digital RSSI value that is averaged over a 128 μs duration.

2.3.3.5 Link quality indicator (LQI)

Link quality indicator (LQI) is based on receiver signal strength indicator (RSSI) or correlator output for the 802.15.4 standard. In this mode, the RSSI measurement is done during normal packet reception. LQI computations for the MKW2xD are based on either digital RSSI or correlator peak values. This setting is executed through a register bit where the final LQI value is available 64 μs after preamble is detected. If a continuous update of LQI based on RSSI throughout the packet is desired, it can be read in a separate 8-bit register by enabling continuous update in a register bit.

2.3.4 Packet processor

The MKW2xD packet processor performs sophisticated hardware filtering of the incoming received packet to determine if the packet is both PHY- and MAC-compliant, is addressed to this device, if the device is a PAN coordinator and whether a message is pending for the sending device. The packet processor greatly reduces the packet filtering burden on software allowing it to tend to higher-layer tasks with a lower latency and smaller software footprint.

2.3.4.1 Features

- Aggressive packet filtering to enable long, uninterrupted MCU sleep periods
- Fully compliant with both 2003 and 2006 versions of the 802.15.4 wireless standard
- Supports all frame types, including reserved types
- Supports all valid 802.15.4 frame lengths
- Enables auto-Tx acknowledge frames (no MCU intervention) by parsing of frame control field and sequence number
- Supports all source and destination address modes, and also PAN ID compression
- Supports broadcast address for PAN ID and short address mode

- Supports “promiscuous” mode, to receive all packets regardless of address- and rules-checking
- Allows frame type-specific filtering (e.g., reject all but beacon frames)
- Supports SLOTTED and non-SLOTTED modes
- Includes special filtering rules for PAN coordinator devices
- Enables minimum-turnaround Tx-acknowledge frames for data-polling requests by automatically determining message-pending status
- Assists MCU in locating pending messages in its indirect queue for data-polling end devices
- Makes available to MCU detailed status of frames that fail address- or rules-checking.
- Supports Dual PAN mode, allowing the device to exist on 2 PAN's simultaneously
- Supports 2 IEEE addresses for the device
- Supports active promiscuous mode

2.3.5 Packet buffering

The packet buffer is a 128-byte random access memory (RAM) dedicated to the storage of 802.15.4 packet contents for both TX and RX sequences. For TX sequences, software stores the contents of the packet buffer starting with the frame length byte at packet buffer address 0 followed by the packet contents at the subsequent packet buffer addresses. For RX sequences the incoming packet's frame length is stored in a register external to the packet buffer. Software will read this register to determine the number of bytes of packet buffer to read. This facilitates DMA transfer through the SPI. For receive packets, an LQI byte is stored at the byte immediately following the last byte of the packet (frame length +1). Usage of the packet buffer for RX and TX sequences is on a time-shared basis; receive packet data will overwrite the contents of the packet buffer. Software can inhibit receive-packet overwriting of the packet buffer contents by setting the PB_PROTECT bit. This will block RX packet overwriting, but will not inhibit TX content loading of the packet buffer via the SPI.

2.3.5.1 Features

- 128 byte buffer stores maximum length 802.15.4 packets
- Same buffer serves both TX and RX sequences
- The entire Packet Buffer can be uploaded or downloaded in a single SPI burst.
- Automatic address auto-incrementing for burst accesses
- Single-byte access mode supported.
- Entire packet buffer can be accessed in hibernate mode
- Under-run error interrupt supported

2.4 Dual PAN ID

In the past, radio transceivers designed for IEEE 802.15.4 applications allowed a device to associate to one and only one PAN (Personal Area Network) at any given time. The MKW2xD represents a high-performance SiP that includes hardware support for a device to reside in two networks simultaneously. In optional Dual PAN mode, the device alternates between the two (2) PANs under hardware or software control. Hardware support for Dual PAN operation consists of two (2) sets of PAN and IEEE addresses for the device, two (2) different channels (one for each PAN) and a programmable timer to automatically switch PANs (including on-the-fly channel changing) without software intervention. There are control bits to configure and enable Dual PAN mode, and read only bits to monitor status in Dual PAN mode. A device can be configured to be a PAN coordinator on either network, both networks or neither.

For the purpose of defining PAN in the context of Dual PAN mode, two (2) sets of network parameters are maintained; PAN0 and PAN1. PAN0 and PAN1 will be used to refer to the two (2) PANs where each parameter set uniquely identifies a PAN for Dual PAN mode. These parameters are described in Table 1.

Table 1. PAN0 and PAN1 descriptions

PAN0	PAN1
Channel0 (PHY_INT0, PHY_FRAC0)	Channel1 (PHY_INT1, PHY_FRAC1)
MacPANID0 (16-bit register)	MacPANID1 (16-bit register)
MacShortAddrs0 (16-bit register)	MacShortAddrs1 (16-bit register)
MacLongAddrs0 (64-bit registers)	MacLongAddrs1 (64-bit registers)
PANCORDNTR0 (1-bit register)	PANCORDNTR1 (1-bit register)

During device initialization if Dual PAN mode is used, software will program both parameter sets to configure the hardware for operation on two (2) networks.

3 System and power management

The MKW2xD is a low power device that also supports extensive system control and power management modes to maximize battery life and provide system protection.

3.1 Modes of operation

The transceiver modes of operation include:

- Idle mode
- Doze mode
- Low power (LP) / hibernate mode
- Reset / powerdown mode
- Run mode

3.2 Power management

The MKW2xD power management is controlled through programming the modes of operation. Different modes allow for different levels of power-down and RUN operation. For the receiver, programmable power modes available are:

- Preamble search
- Preamble search sniff
- Low Power Preamble Search (LPPS)
- Fast Antenna Diversity (FAD) Preamble search
- Packet decoding

4 Radio Peripherals

The MKW2xD provides a set of I/O pins useful for suppling a system clock to the MCU, controlling external RF modules/circuitry, and GPIO.

4.1 Clock output (CLK_OUT)

MKW2xD integrates a programmable clock to source numerous frequencies for connection with various MCUs. Package pin 39 can be used to provide this clock source as required allowing the user to make adjustments per their application requirement.

The transceiver CLK_OUT pin is internally connected to the MCU EXTAL pin so that no external connection is needed to drive the MCU clock.

Care must be taken that the clock output signal does not interfere with the reference oscillator or the radio. Additional functionality this feature supports is:

- XTAL domain can be completely gated off (hibernate mode)
- SPI communication allowed in hibernate

Table 2. CLK_OUT

CLK_OUT_DIV [2:0]	CLK_OUT frequency
0	32 MHz[1]
1	16 MHz[1]
2	8 MHz[1]
3	4 MHz
4	2 MHz
5	1 MHz
6	62.5 kHz
7	32.786 kHz

1. May require high drive strength for proper signal integrity.

There is an enable/disable bit for CLK_OUT. When disabling, the clock output will optionally continue to run for 128 clock cycles after disablement. There is also be one (1) bit available to adjust the CLK_OUT I/O pad drive strength.

4.2 General-purpose input output (GPIO)

In addition to the MCU supported GPIOs, the radio supports 2 GPIO pins. All I/O pins will have the same supply voltage and depending on the supply, can vary from 1.8 V up to 3.6 V. When the pin is configured as a general-purpose output or for peripheral use, there will be specific settings required per use case. Pin configuration will be executed by software to adjust input/output direction and drive strength, capability. When the pin is configured as a general-purpose input or for peripheral use, software (see Table 3) can enable a pull-up or pull-down device. Immediately after reset, all pins are configured as high-impedance general-purpose inputs with internal pull-up devices enabled.

Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)

Table 3. Pin configuration summary

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer full drive mode[1]	Source or sink	—	±10	—	mA
I/O buffer partial drive mode[1]	Source or sink	—	±2	—	mA
I/O buffer high impedance[2]	Off state	—	—	10	nA
No slew, full drive	Rise and fall time[3]	2	4	6	ns
No slew, partial drive	Rise and fall time	2	4	6	ns
Slew, full drive	Rise and fall time	6	12	24	ns
Slew, partial drive	Rise and fall time	6	12	24	ns
Propagation delay[4], no slew	Full drive[5]	—	—	11	ns
Propagation delay, no slew	Partial drive[6]	—	—	11	ns
Propagation delay, slew	Full drive	—	—	50	ns
Propagation delay, slew	Partial drive	—	—	50	ns

1. For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
2. Leakage current applies for the full range of possible input voltage conditions.
3. Rise and fall time values in reference to 20% and 80%
4. Propagation Delay measured from/to 50% voltage point.
5. Full drive values provided are in reference to a 75 pF load.
6. Partial drive values provided are in reference to a 15 pF load.

4.3 Serial peripheral interface (SPI)

The MKW2xD SiP uses a SPI interface allowing the MCU to communicate with the radio's register set and packet buffer. The SPI is a slave-only interface; the MCU must drive R_SSEL_B, R_SCLK and R_MOSI. Write and read access to both direct and indirect registers is supported, and transfer length can be single-byte or bursts of unlimited length. Write and read access to the Packet buffer can also be single-byte or a burst mode of unlimited length.

The SPI interface is asynchronous to the rest of the IC. No relationship between R_SCLK and MKW2xD's internal oscillator is assumed. And no relationship between R_SCLK and the CLK_OUT pin is assumed. All synchronization of the SPI interface to the IC takes place inside the SPI module. SPI synchronization takes place in both directions; register writes and register reads. The SPI is capable of operation in all power modes, except Reset. Operation in hibernate mode allows most transceiver registers and the complete packet buffer to be accessed in the lowest-power operating state enabling minimal power consumption, especially during the register-initialization phase of the radio.

The SPI design features a compact, single-byte control word, reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word, with the address embedded in the control word. During control word transfer (the first byte of any SPI access), the contents of the IRQSTS1 register (MKW2xD radio's highest-priority status register) are always shifted out so that the MCU gets access to IRQSTS1, with the minimum possible latency, on every SPI access.

4.3.1 Features

- 4-wire industry standard interface, supported by all MCUs
- SPI R_SCLK maximum frequency 16 MHz (for SPI write accesses)
- SPI R_SCLK maximum frequency 9 MHz (for SPI read accesses)
- Write and read access to all radio registers (direct and indirect)
- Write and read access to packet buffer
- SPI accesses can be single-byte or burst
- Automatic address auto-incrementing for burst accesses

- The entire packet buffer can be uploaded or downloaded in a single SPI burst
- Entire packet buffer and most registers can be accessed in hibernate mode
- Built-in synchronization inside the SPI module to/from the rest of the radio

4.4 Antenna diversity

To improve the reliability of RF connectivity to long range applications, the antenna diversity feature is supported without using the MCU through use of four dedicated control pins (package pins 44, 45, 46, and 47).

Fast antenna diversity (FAD) mode supports this radio feature and, when enabled, will allow the choice of selection between two antennas during the preamble phase. By continually monitoring the received signal, the FAD block will select the first antenna of which the received signal has a correlation factor above a predefined progammable threshold. The FAD accomplishes the antenna selection by sequentially switching between the two antennas testing for the presence of suitably strong s0 symbol where the first antenna to reach this condition is then selected for the reception of the packet.

The antenna's are monitored for a period of 28 µs each. The antenna switching is continued until 1.5 valid s0 symbols are detected. The demodulator then continues with normal preamble search before declaring “Preamble Detect”.

4.5 RF Output Power Distribution

The following figure shows the linear region of the output and the typical power distribution of the radio as a function of PA_PWR [4:0] range. The PA_PWR [4:0] is the lower 5 bits of the PA_PWR 0x23 direct register and has a usable range of 3 to 31 decimal.

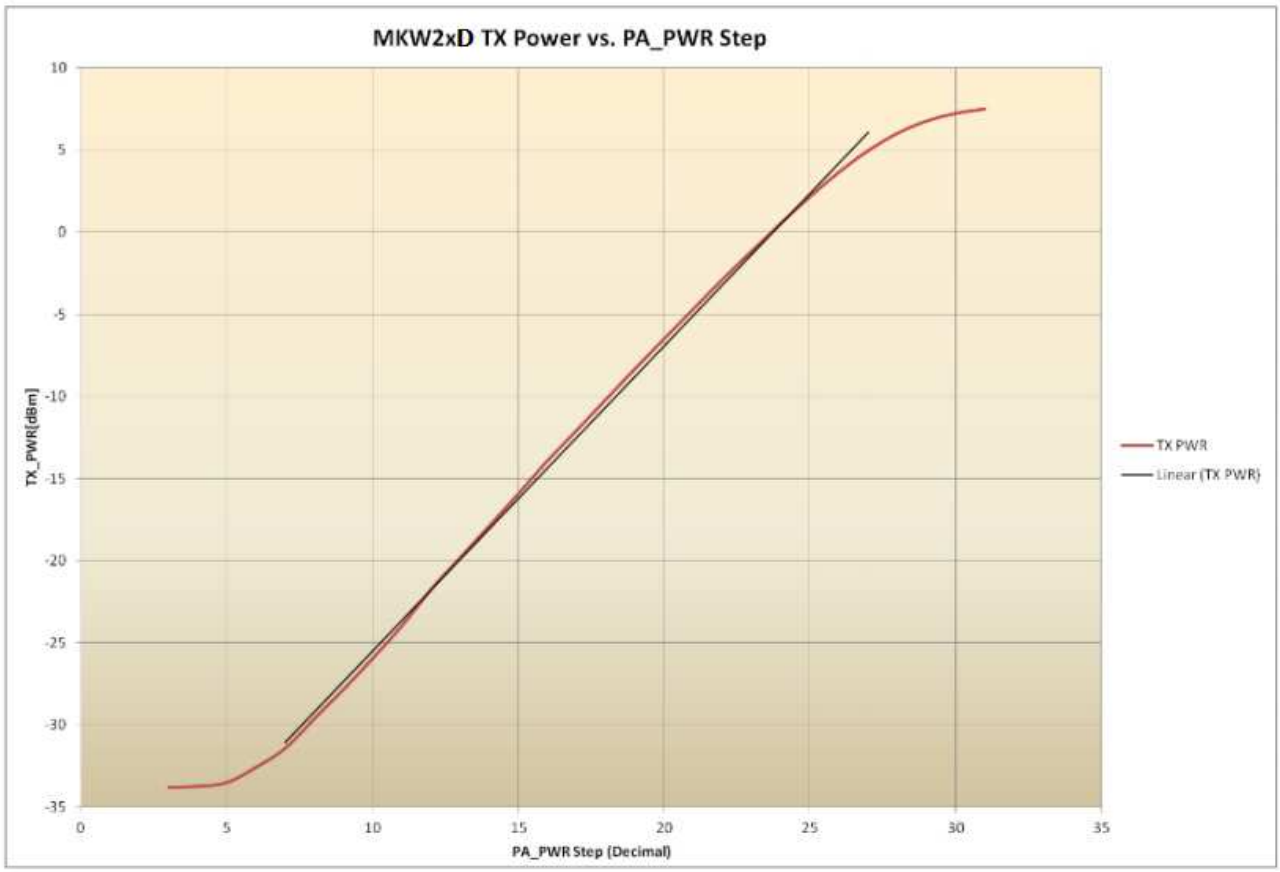


Figure 2. MKW2xD transmit power vs. PA_PWR step

5 MKW2xD operating modes

For the discussion of this topic, the primary radio and MCU operating modes are combined so that overall power consumption can then be derived. Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. Both the radio and MCU's power modes are described as follows.

The radio has 6 primary operating modes:

- Reset / power down
- Low power (LP) / hibernate
- Doze (low power with reference oscillator active)

- Idle
- Receive
- Transmit

Table 4 lists and describes the transceivers power modes and consumption.

Table 4. Transceiver Power Modes

Mode	Definition	Current consumption[1]
Reset / powerdown	All IC functions off, leakage only. $\overline{RST}$ asserted.	< 100 nA
Low power / hibernate	Crystal reference oscillator off. (SPI is functional.)	< 1 µA
Doze[2]	Crystal reference oscillator on but CLK_OUT output available only if selected.	500 µA[3] (no CLK_OUT)
Idle	Crystal reference oscillator on with CLK_OUT output available only if selected.	700 µA[3] (no CLK_OUT)
Receive	Crystal reference oscillator on. Receiver on.	< 19.5 mA [4] 15 mA, LPPS mode
Transmit	Crystal reference oscillator on. Transmitter on.	< 18 mA [5]

1. Conditions: VBAT and VBAT_2 = 2.7 V, nominal process @ 25°C
2. While in Doze mode, 4 MHz max frequency can be selected for CLK_OUT.
3. Typical
4. Signal sensitivity = -102 dBm
5. RF output = 0 dBm

The MCU has a variety of operating modes. For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

5.1 Transceiver Transmit Current Distribution

The following figure shows the relation between the transmit power generated by the radio and its current consumption.

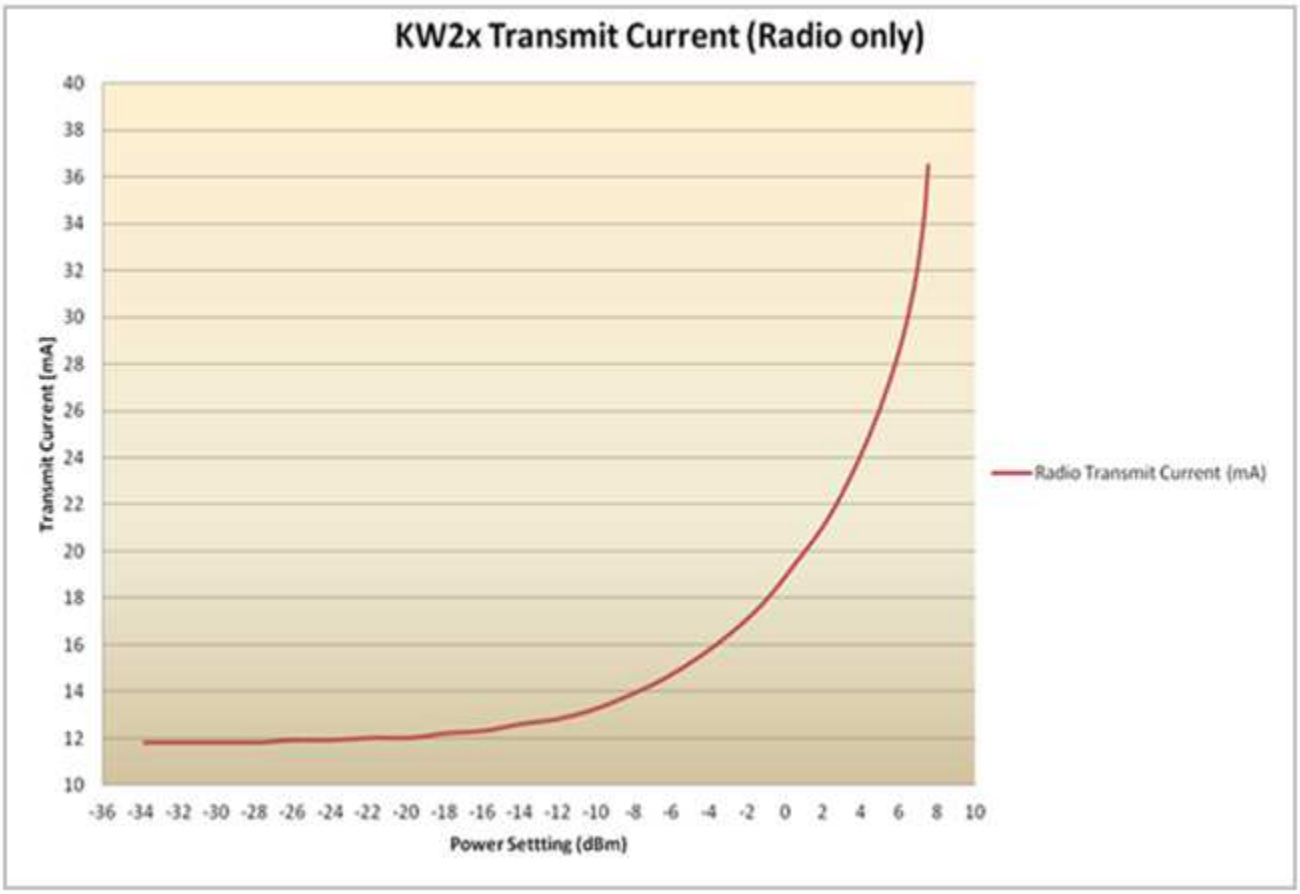


Figure 3. MKW2xD transmit power vs transmit current (Radio Only)

6 MKW2xD electrical characteristics

6.1 Radio recommended operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BAT} = VDD_{INT})	V_{BAT}, VDD_{INT}	1.8	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	-40	25	105	°C

Table continues on the next page...

Table 5. Recommended operating conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic Input Voltage Low	VIL	0	—	30% VDDINT	V
Logic Input Voltage High	VIH	70% VDDINT	—	VDDINT	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

6.2 Ratings

6.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit	Notes
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

6.2.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

7 MCU Electrical characteristics

7.1 Maximum ratings

Table 6. Maximum ratings

Requirement	Description	Symbol	Rating level	Unit
Power Supply Voltage		VBAT, VBAT2	-0.3 to 3.6	Vdc
Digital Input Voltage		Vin	-0.3 to (VDDINT + 0.3)	Vdc
RF Input Power		Pmax	+10	dBm
Note: Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.				
ESD[1]	Human Body Model	HBM	±2000	Vdc
	Machine Model	MM	±200	Vdc

Table continues on the next page...

Table 6. Maximum ratings (continued)

Requirement	Description	Symbol	Rating level	Unit
	Charged Device Model	CDM	±750	Vdc
EMC[2]	Power Electro-Static Discharge / Direct Contact	PESD	No damage / latch up to ±4000	Vdc
			No soft failure / reset to ±1000	
	Power Electro-Static Discharge / Indirect Contact		No damage / latch up to ±6000	Vdc
			No soft failure / reset to ±1000	
	Langer IC / EFT / P201	EFT (Electro Magnetic Fast Transient)	No damage / latch up to ±5	Vdc
			No soft failure / reset to ±5	
	Langer IC / EFT / P201		No damage / latch up to ±300	Vdc
			No soft failure / reset to ±150	
Junction Temperature		T_J	+125	°C
Storage Temperature Range		T_{stg}	-65 to +165	°C

1. Electrostatic discharge on all device pads meet this requirement
2. Electromagnetic compatibility for this product is low stress rating level

Note

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.

7.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.