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MKW40Z160 MKW30Z160 MKW20Z160

MKW40Z/30Z/20Z Data Sheet

A Bluetooth® Low Energy and IEEE® 802.15.4 System on a Chip (SoC)
Supports the following:
MKW40Z160VHT4, MKW30Z160VHM4, MKW20Z160VHT4

Key features

- Multi-Standard Radio
  - 2.4 GHz Bluetooth Low Energy version 4.1 compliant
  - IEEE Standard 802.15.4 2011 compliant
  - Typical Receiver Sensitivity (BLE) = -91 dBm
  - Typical Receiver Sensitivity (802.15.4) = -102 dBm
  - Programmable Transmitter Output Power: -18 dBm to +5 dBm
  - Low external component counts for low cost application
- MCU and Memories
  - Up to 48 MHz ARM® Cortex-M0+ core
  - On-chip 160 KB Flash memory
  - On-chip 20 KB SRAM
- Low Power Consumption
  - Typical Rx Current: 6.5 mA (DCDC in buck mode, 3.6 V supply)
  - Typical Tx Current: 8.4 mA (DCDC in buck mode, 3.6 V supply) for a 0 dBm output
  - Low Power Mode (VLLS0) Current: 206 nA
- Clocks
  - 32 MHz Crystal Oscillator
  - 32 kHz Crystal Oscillator
- System peripherals
  - Nine low-power modes to provide power optimization based on application requirements
  - DCDC Converter supporting Buck, Boost, and Bypass modes
  - DMA Controller
  - COP Software watchdog
  - SWD Interface and Micro Trace buffer
  - Bit Manipulation Engine (BME)
- Human-machine interface
  - Touch Sensing Input
  - General-purpose input/output
- Analog modules
  - 16-bit Analog-to-Digital Converter (ADC)
  - 12-bit Digital-to-Analog Converter (DAC)
  - 6-bit High Speed Analog Comparator (CMP)
- Timers
  - 16-bit low-power timer (LPTMR)
  - 3 Timers Modules(TPM): One 4 channels TPM and Two 2 channels TPMs
  - Programmable Interrupt Timer (PIT)
  - Real-Time Clock (RTC)
- Communication interfaces
  - 2 SPI modules
  - 2 I2C modules
  - Low Power UART module
  - Carrier Modulator Timer (CMT)
- Security
  - AES-128 Accelerator (AESA)
  - True Random Number Generator (TRNG)
- Operating Characteristics
  - DCDC Converter supporting Buck, Boost, and Bypass modes
  - Temperature range (ambient): -40 to 85°C

Table of Contents

Introduction

The KW40Z/30Z/20Z (called KW40Z throughout this document) is an ultra low-power, highly integrated single-chip device that enables Bluetooth low energy (BLE) or IEEE Standard 802.15.4 RF connectivity for portable, extremely low-power embedded systems. Applications include portable health care devices, wearable sports and fitness devices, AV remote controls, computer keyboards and mice, gaming controllers, access control, security systems, smart energy and home area networks.

The KW40Z SoC integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, 160 KB Flash and 20 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications.

The KW40Z SoC's radio frequency transceiver is compliant with Bluetooth version 4.1 for Low Energy (aka Bluetooth Smart), and the IEEE standard 802.15.4-2011 using O-QPSK in the 2.4 GHz ISM band.

The KW40Z SoC can be used in applications as a "BlackBox" modem by simply adding BLE or IEEE Std. 802.15.4 connectivity to an existing embedded controller system, or used as a stand-alone smart wireless sensor with embedded application where no host controller is required.

Freescale provides fully certified protocol stacks and application profiles to support KW40Z. The KW40Z Flash and SRAM memory are available for applications and communication protocols using a choice of Freescale or 3rd party software development tools.

The RF section of the KW40Z SoC is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board.

Extremely long battery life is achieved though efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW40Z SoC. Additionally, an integrated DC-DC converter enables a wide operating range from 0.9 V to 4.2 V. The DC-DC in Buck mode enables KW40Z to operate from a single coin cell battery with a significant reduction of peak Rx and Tx current consumption. The DC-DC in boost mode enables a single alkaline battery to be used throughout its entire useful voltage range of 0.9 V to 1.795 V.

1 Ordering information

Table 1. Orderable parts details

Device	Operating Temp Range (T_A)	Package	Description
MKW20Z160VHT4(R)	-40 to 85°C	48-pin Laminate QFN	IEEE 802.15.4
MKW30Z160VHM4(R)	-40 to 85°C	32-pin Laminate QFN	Bluetooth Low Energy Only
MKW40Z160VHT4(R)	-40 to 85°C	48-pin Laminate QFN	Bluetooth Low Energy or IEEE 802.15.4

2 Feature Descriptions

This section provides a simplified block diagram and highlights the KW40Z SoC features.

2.1 Block diagram

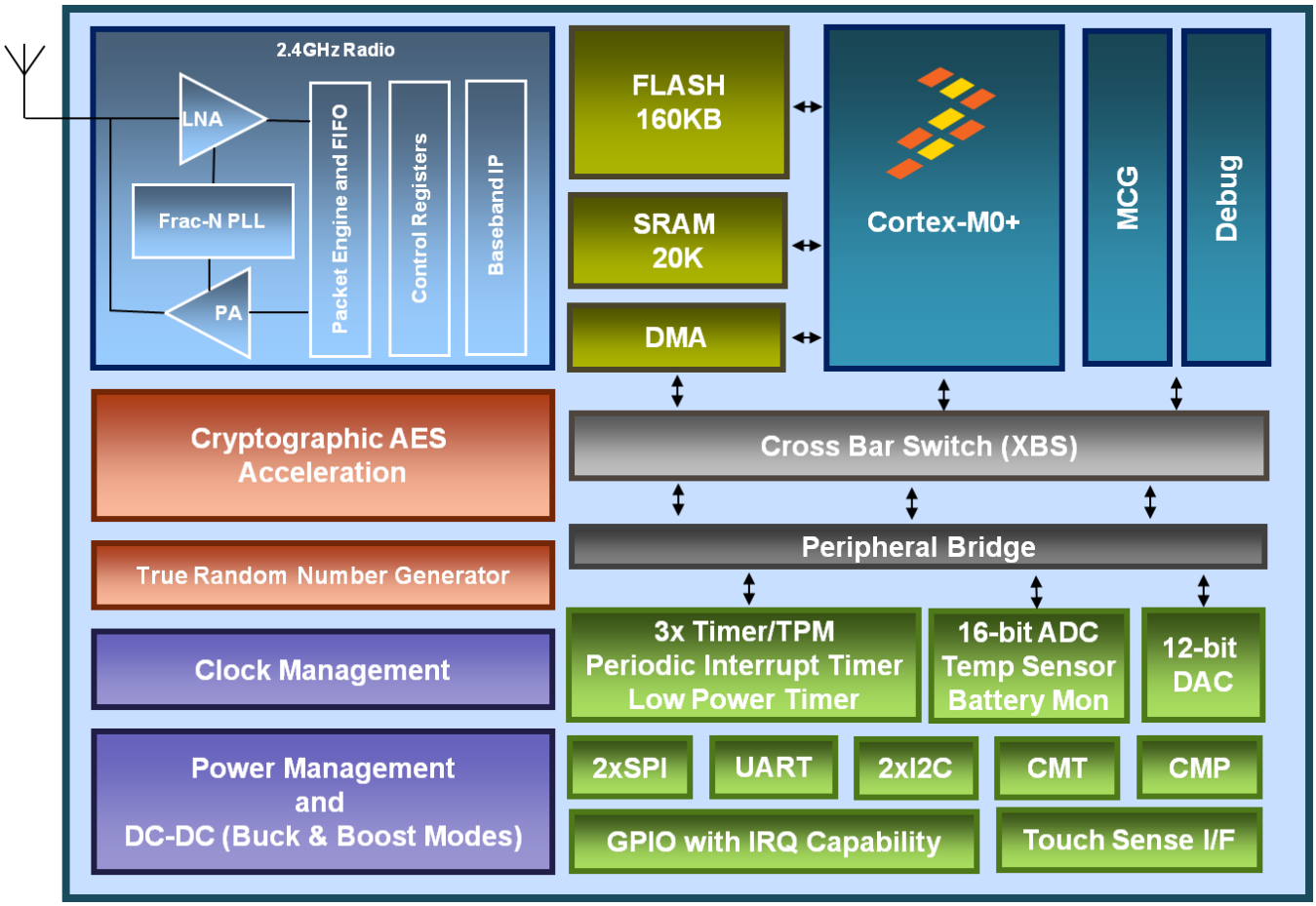


Figure 1. KW40Z/KW30Z/KW20Z simplified block diagram

2.2 Radio features

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- MBAN 2360-2400 MHz

Supported standards:

- Bluetooth v4.1 Low Energy compliant 1 Mbps GFSK modulation
- IEEE Std. 802.15.4-2011 compliant O-QPSK modulation
- Freescale Thread Networking Stack
- Bluetooth Low Energy(BLE) Application Profiles
- ZigBee PRO and application profiles

Receiver performance:

- Receive sensitivity of -91 dBm for BLE
- Receive sensitivity of -102 dBm typical for IEEE Std. 802.15.4

Other features:

- Programmable transmit output power from -18 dBm to +5 dBm with DC/DC bypass and buck modes of operation
- Bluetooth Low Energy Link Layer hardware
- Hardware acceleration for IEEE Std. 802.15.4 packet processing
- 32 MHz crystal reference oscillator
- Supports antenna diversity option for IEEE Std. 802.15.4
- Supports dual PAN for IEEE Std. 802.15.4 with hardware-assisted address matching acceleration
- Differential RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA

2.3 Microcontroller features

ARM Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes

- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

Debug Controller

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

On-Chip Memory

- 160 KB Flash
  - Firmware distribution protection. Flash can be marked execute-only on a per-sector (4 KB) basis to prevent firmware contents from being read by 3rd parties
  - Flash implemented as one 128 KB block and one 32 KB block. Code can execute or read from one block while the other block is being erased or programmed
- 20 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

2.4 System features

Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

DC-DC Converter

- Internal switch mode power supply supporting Buck, Boost, and Bypass operating modes

- Buck operation supports external voltage sources of 2.1 V to 4.2 V. This reduces peak current consumption during Rx and Tx by ~25%, ideal for single coin-cell battery operation (typical CR2032 cell).
- Boost operation supports external voltage sources of 0.9V to 1.795V, which is efficiently increased to the static internal core voltage level, ideal for single battery operation (typical AA or AAA alkaline cell).
- When DCDC is not used, the device supports an external voltage range of 1.45V to 3.6V (1.45 - 3.6V on VDD_RF1, VDD_RF2, VDD_XTAL and VDD_1P45OUT_PMCIN pins. 1.71 - 3.6V on VDD_0, VDD_1 and VDDA pins)
- An external inductor is required to support the Buck or Boost modes
- The DCDC Converter 1.8V output current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
  - Up to 44mA in buck mode with VDD_1P8 = 1.8V
  - Up to 31.4mA in buck mode with VDD_1P8 = 3.0V

DMA Controller

- Four independently programmable DMA controller channels provides the means to directly transfer data between system memory and I/O peripherals
- DMA controller is capable of functioning in run and wait modes of operation
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-, 16-, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation

DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

System Clocks

- 32 MHz crystal reference oscillator provides clock for the radio, and is the main clock option for the MCU
- 32/32.768 kHz crystal reference oscillator used to maintain precise Bluetooth radio time in low power modes
- Multipurpose Clock Generator (MCG)

- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
  - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 2% accuracy across full temperature range
  - On-chip 4MHz oscillator with 5% accuracy across full temperature range
- Frequency-locked loop (FLL) controlled by internal or external reference
  - 20 MHz to 48 MHz FLL output

Unique Identifiers

- 10 bytes of the Unique ID represents a unique identifier for each chip
- 40 bits of unique MAC address can be used to generate BLE or 802.15.4 device address

2.5 Peripheral features

16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in 16-, 12-, 10-, or 8-bit right justified format
- Single or continuous conversion
- Configurable sample time and conversion speed / power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor
- Battery voltage measurement
- Hardware average function
- Selectable voltage reverence
- Self-calibration mode

12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode

- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes

Low Power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency

Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
  - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires MCU POR to enable write access
  - Soft lock requires system reset to enable write/read access
- Capable of waking up the system from low power modes

Inter-Integrated Circuit (I^2C)

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 1 Mbps operation
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

LPUART

- One channel
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup

- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes

Serial Peripheral Interface (DSPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

Carrier Modulator Timer (CMT)

- Four modes of operation
  - Time; with independent control of high and low times
  - Baseband
  - Frequency shift key (FSK)
  - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wakeup events
- Configurable drive strength on some output pins

Touch Sensor Input (TSI)

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes

- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Fully support Freescale touch sensing software (TSS) library
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times
- Support DMA data transfer

Keyboard Interface

- GPIO can be configured to function as a interrupt driven keyboard scanning matrix
  - In the 48pin package there are a total of 28 digital pins
  - In the 32pin package there are a total of 15 digital pins
  - These pins can be configured as needed by the application as GPIO, UART, SPI, I2C, ADC, timer I/O as well as other functions

AES Accelerator (AESA)

- The Advanced Encryption Standard Accelerator (AESA) is a stand-alone symmetric encryption accelerator supporting 128- bit key and data size and the following modes:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Counter (CTR)
  - CTR & CBC-MAC (CCM and CCM*)
  - Cipher-base MAC (CMAC)
  - Extended Cipher Block Chaining Message Authentication Code (XCBC-MAC)
- The AESA supports all BLE and IEEE 802.15.4 packet sizes
- The AESA supports DMA and interrupt-driven operation

True Random Number Generator (TRNG)

- The TRNG is an entropy source
- The TRNG output is intended to be read and used as an input to a deterministic random number generator
- The deterministic random number general will be implemented in software
- A FIPS 180 compliant solution can be realized using the TRNG together with a FIPS compliant determinstic random number generator and SoC-level security

3 Transceiver Description

- Direction Conversion Receiver
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

3.1 Key Specifications

The KW40Z SoC meets or exceeds all Bluetooth Low Energy v4.1 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specification for the KW40Z are:

Frequency Band:

- ISM Band: 2400 to 2483.5MHz
- MBAN Band: 2360 to 2400MHz

Bluetooth Low Energy v4.1 modulation scheme:

- Symbol rate: 1000kbps
- Modulation: GFSK
- Receiver sensitivity: -91 dBm, typical
- Programmable transmitter output power: -18 dBm to +5 dBm

IEEE Standard 802.15.4 2.4 GHz modulation scheme:

- Chip rate: 2000kbps
- Data rate: 250kbps
- Symbol rate: 62.5kbps
- Modulation: OQPSK
- Receiver sensitivity: -102dBm, typical (@1% PER for 20 byte payload packet)
- Differential bidirectional RF input/output port with integrated transmit/receive switch
- Programmable transmitter output power: -18 dBm to +5 dBm

3.2 Frequency Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4GHz ISM Channel numbering:

- Fc=2402 + K * 2 MHz, K=0,.....,39.

MBAN Channel numbering:

- Fc=2363 + 5*K in MHz, for K=0,.....,6)
- Fc=2367 + 5*(K-7) in MHz, for K=7,8.....,13)

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
0	2402	0	2360	28	2390
1	2404	1	2361	29	2391
2	2406	2	2362	30	2392
3	2408	3	2363	31	2393
4	2410	4	2364	32	2394
5	2412	5	2365	33	2395
6	2414	6	2366	34	2396
7	2416	7	2367	35	2397
8	2418	8	2368	36	2398
9	2420	9	2369	0	2402
10	2422	10	2370	1	2404
11	2424	11	2371	2	2406
12	2426	12	2372	3	2408
13	2428	13	2373	4	2410
14	2430	14	2374	5	2412
15	2432	15	2375	6	2414
16	2434	16	2376	7	2416
17	2436	17	2377	8	2418
18	2438	18	2378	9	2420
19	2440	19	2379	10	2422
20	2442	20	2380	11	2424
21	2444	21	2381	12	2426
22	2446	22	2382	13	2428
23	2448	23	2383	14	2430
24	2450	24	2384	15	2432
25	2452	25	2385	16	2434
26	2454	26	2386	17	2436
27	2456	27	2387	18	2438
28	2458	28	2388	19	2440
29	2460	29	2389	20	2442
30	2462	30	2390	21	2444
31	2464	31	2391	22	2446
32	2466	32	2392	23	2448

Table continues on the next page...

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
33	2468	33	2393	24	2450
34	2470	34	2394	25	2452
35	2472	35	2395	26	2454
36	2474	36	2396	27	2456
37	2476	37	2397	37	2476
38	2478	38	2398	38	2478
39	2480	39	2399	39	2480

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, IEEE (R) 802.15.1 and Bluetooth Low Energy V4.0 single mode operation is allowed in these channels.

3.3 Frequency Plan for 802.15.4 and 802.15.4j (MBAN)

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for 802.15.4.

2.4GHz ISM Channel numbering:

- Fc=2402.0 + 5*(K-11) MHz, K=11, 12, ..,26.

MBAN Channel numbering:

- Fc=2363.0 + 5*K in MHz, for K=0,.....,6)
- Fc=2367.0 + 5*(K-7) in MHz, for K=7,.....,14)

Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
11	2405	0	2363
12	2410	1	2368
13	2415	2	2373
14	2420	3	2378
15	2425	4	2383
16	2430	5	2388
17	2435	6	2393
18	2440	7	2367

Table continues on the next page...

Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
19	2445	8	2372
20	2450	9	2377
21	2455	10	2382
22	2460	11	2387
23	2465	12	2392
24	2470	13	2397
25	2475	14	2395
26	2480		

1. Usable channel spacing to assit in co-existence.

3.4 Transceiver Functions

Receive

- The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to a sigma-delta analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing.

Transmit

- The transmitter transmits O-QPSK or GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RF_P, RF_N) are converted as single ended (SE) signals with off chip components as required.

4 System and Power Management

4.1 Power Management

The KW40Z SoC includes internal power management features that can be used to control the power usage. The power management of the KW40Z includes power management controller (PMC) and a DCDC converter which can operate in a buck, boost or bypass configuration. The PMC is designed such that the RF radio will remain in state-retention while the core is in various stop modes. It can make sure the device can stay in low current consumption mode while the RF radio can wakeup quick enough for communication.

4.1.1 DCDC Converter

The features of the DCDC converter include the following:

- Single inductor, multiple outputs
- Buck and boost modes (pin selectable; CFG=VDCDC_IN -> buck; CFG=GND -> boost)
- Continuous or pulsed operation (hardware/software configurable)
- Power switch input to allow external control of power up, and to select bypass mode
- Output signal to indicate power stable. Purpose is for the rest of the chip to use as a POR
- Scaled battery output voltage suitable for SAR ADC utilization
- Internal oscillator for support when the reference oscillator is not present
- 1.8V output is capable to supply external device: max 38.9mA (V1P8 = 1.8V, VDCDC_IN = 3.0V) and 20.9mA (V1P8 = 3.0V, VDCDC_IN = 3.0V), with MCU in RUN mode, peripherals are disabled

4.2 Modes of Operation

The ARM Cortex-M0+ core in the KW40Z SoC has three primary modes of operation: Run, Wait, and Stop modes. For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes are similar to ARM deep sleep modes. The very low power run (VLPR) operation mode can drastically reduce runtime power when the maximum bus frequency is note required to handle the application needs.

The WFI instruction invokes both wait and stop modes for KW40Z. The primary modes are augmented in a number of ways to provide lower power based on application needs.

4.2.1 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 4. Power modes (At 25 deg C)

Power mode	Description	CPU recovery method	Radio
Normal Run (all peripherals clock off)	Allows maximum performance of chip.	—	Radio can be active
Normal Wait - via WFI	Allows peripherals to function, while allowing CPU to go to sleep reducing power.	Interrupt	
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection.	Interrupt	
PStop2 (Partial Stop 2)	Core and system clocks are gated. Bus clock remains active. Masters and slaves clocked by bus clock reamin in Run or VLPRun mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
PStop1 (Partial Stop 1)	Core, system clocks and bus clock are gated. All bus masters and slaves enter Stop mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode.	Interrupt	
VLPR (Very Low Power Run) (all peripherals off)	Reduced frequency (1MHz) Flash access mode, regulator in low power mode, LVD off. Internal oscillator can provide low power 4 MHz source for core. (Values @2MHz core/ 1MHz bus and flash, module off, execution from flash). Biasing is disabled when DCDC is configured for continuous mode in VLPR/W	—	Radio operation is possible only when DCDC is configured for continuous mode.[1] However, there may be insufficient MIPS with a 4MHz MCU to support much in the way of radio operation.
VLPW (Very Low Power Wait) - via WFI (all peripherals off)	Similar to VLPR, with CPU in sleep to further reduce power. (Values @4MHz core/ 1MHz bus, module off) Biasing is disabled when DCDC is configured for continous mode in VLPR/W	Interrupt	

Table continues on the next page...

Table 4. Power modes (At 25 deg C) (continued)

Power mode	Description	CPU recovery method	Radio
VLPS (Very Low Power Stop) via WFI	Places MCU in static state with LVD operation off. Lowest power mode with ADC and all pin interrupts functional. LPTMR, RTC, CMP, TSI can be operational. Biasing is disabled when DCDC is configured for continuous mode in VLPS	Interrupt	
LLS3 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio Sea of Gates(SOG) logic is in state retention	Wakeup Interrupt	Radio SOG is in state retention in LLSx. The BTLL DSM[2] logic can be active using the 32kHz clock
LLS2 (Low Leakage Stop)	State retention power mode. LLWU, LPTMR, RTC, CMP, TSI can be operational. Only 4KBytes of RAM retained.All of the radio SOG logic is in state retention	Wakeup Interrupt	
VLLS3 (Very Low Leakage Stop3)	Full SRAM retention. LLWU, LPTMR, RTC, CMP, TSI can be operational. All of the radio SOG logic is in state retention	Wakeup Reset	Radio SOG is in state retention in VLLS3/2. The BTLL DSM logic can be active using the 32kHz clock
VLLS2 (Very Low Leakage Stop2)	Partial SRAM retention. 4KBytes of RAM retained. LLWU, LPTMR, RTC, CMP, TSI can be operational.All of the radio SOG logic is in state retention	Wakeup Reset	
VLLS1 (Very Low Leakage Stop1) with RTC + 32kHz OSC	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio SOG is power-gated in VLLS1/0. Radio state is lost at VLLS1 and lower power states
VLLS1 (Very Low Leakage Stop1) with LPTMR + LPO	All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP, TSI can be operational.	Wakeup Reset	
VLLS0 (Very Low Leakage Stop0) with Brown-out Detection	VLLS0 is not supported with DCDC The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection enabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	Radio operation not supported. The Radio digital is power-gated in VLLS1/0
VLLS0 (Very Low Leakage Stop0)	VLLS0 is not supported with DCDC buck/boost configuration but is supported with bypass configuration The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection disabled, Pin interrupt only. Radio logic is power gated.	Wakeup Reset	

1. Biasing is disabled, but the Flash is in a low power mode for VLPx, so this configuration can realize some power savings over use of Run/Wait/Stop
2. DSM refers to BTLL's deepsleep mode. DSM does not refer to the ARM sleep deep mode.

5 Transceiver Electrical Characteristics

5.1 Recommended radio operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
RF and Analog Power Supply Voltage	VDD_{RF1}, VDD_{RF2}, VDD_{XTAL}	1.45	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	-40	25	85	°C
Logic Input Voltage Low	VIL	0	—	30% VDD_{INT} [1]	V
Logic Input Voltage High	VIH	70% VDD_{INT}	—	VDD_{INT}	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	0	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

1. VDD_{INT} is the internal LDO regulated voltage supplying various circuit blocks, VDD_{INT}=1.2 V

5.2 Receiver Feature Summary

Table 6. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	1000	nA
Supply current Rx On with DC-DC converter enable (Buck; Vbat = 3.6V)	I_{Rxon}	—	6.5	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass) [2]	I_{Rxon}	—	15.4	—	mA
Input RF Frequency	f_{in}	2.360	—	2.4835	GHz
BLE Rx Sensitivity [3]	$SENS_{BLE}$	—	-91	—	dBm
IEEE 802.15.4 Rx Sensitivity [4]	$SENS_{15.4}$	—	-102	—	dBm
Noise Figure for max gain mode @ typical sensitivity	NF_{HG}	—	6.5	—	dB
Receiver Signal Strength Indicator Range	$RSSI_{Range}$	-96	—	0	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dB

Table continues on the next page...

Table 6. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
BLE Co-channel Interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).			-6		dB
IEEE 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)	$C/I_{CO\text{-}channel}$	—	0	—	dB
Adjacent/Alternate Channel Performance[5]					
BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 1\ MHz}$	—	-4	—	dB
BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 2\ MHz}$	—	28	—	dB
BLE Alternate ≥ +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$C/I_{BLE,\ 3\ MHz}$	—	35	—	dB
IEEE 802.15.4 Adjacent +/- 5 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%)		—	43	—	dB
IEEE 802.15.4 Alternate ≥ +/- 10 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%.)		—	50	—	dB
Blocking Performance[5]					
BLE Out of band blocking from 30 MHz to 2000 MHz (Wanted signal at -67 dBm , BER <0.1%. Interferer continuous wave signal.)	—	—	-30	—	dBm
BLE Out of band blocking from 2003 MHz to 2339 MHz (Wanted signal at -67 dBm, BER <0.1%. Interferer continuous wave signal.)	—	—	-35	—	dBm
BLE Out of band blocking from 2484 MHz to 2997 MHz (Wanted signal at -67 dBm , BER <0.1%. Interferer continuous wave signal.)	—	—	-35	—	dBm
BLE Out of band blocking from 3000 MHz to 12750 MHz (Wanted signal at -67 dBm , PER<1%, Interferer continuous wave signal.)	—	—	-30	—	dBm
IEEE 802.15.4 Out of band blocking for frequency offsets > 10 MHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)		—	-44	—	dBm
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|< 1.6MHz	—	—	-50	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|> 2.5 MHz[6]	—	—	-63	—	dBc

1. All the RX parameters are measured at the KW40 RF pins
2. Transceiver power consumption

3. Measured at 0.1% BER using 37 byte long packets in max gain mode and nominal conditions
4. In max gain mode and nominal conditions
5. BLE Adjacent and Block parameters are measured with modulated interference signals
6. Exceptions allowed for reference frequency multiples

5.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 50 µs
- Reference Frequency: 32 MHz
- Low Integrated Phase Noise: -81 dBVrms (1 kHz to 1 MHz)

Table 7. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	—	nA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter enabled (Buck; Vbat = 3.6V)	I_{Txone}	—	8.4	—	mA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter disabled (Bypass) [2]	I_{Txond}	—	18.5	—	mA
Output Frequency	fin	2.360	—	2.4835	GHz
Maximum RF Output power	$P_{RF,max}$	—	5	—	dBm
Minimum RF Output power [3]	$P_{RF,min}$	—	-18	—	dBm
RF Output power control range	P_{RFCR}	—	23	—	dB
IEEE 802.15.4 Peak Frequency Deviation	$F_{dev15.4}$	—	±500	—	kHz
IEEE 802.15.4 Error Vector Magnitude[4]	$EVM_{15.4}$		8		%
IEEE 802.15.4 Offset Error Vector Magnitude[5]	$OEVM_{15.4}$		2		%
IEEE 802.15.4 TX spectrum level at 3.5MHz offset[4, 6]	$TXPSD_{15.4}$			-30	dBc
BLE TX Output Spectrum 20dB BW	$TXBW_{BLE}$		1.0	—	MHz
BLE average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE}$		250		kHz
BLE average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE}$		210		kHz
BLE Maximum Deviation of the Center Frequency[7]	$F_{cdev,BLE}$	—	±10	—	kHz
BLE Adjacent Channel Transmit Power at 2MHz offset[6]	$P_{RF2MHz,BLE}$	—	—	-35	dBm
BLE Adjacent Channel Transmit Power at >= 3MHz offset[6]	$P_{RF3MHz,BLE}$	—	—	-45	dBm
BLE Frequency Hopping Support			YES		

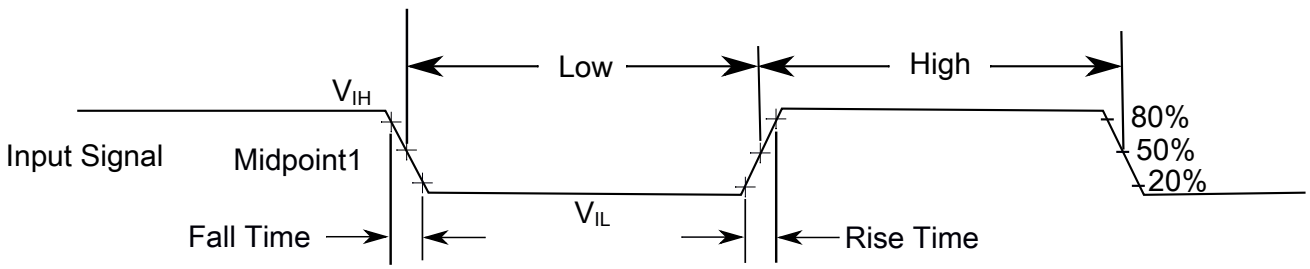
1. All the TX parameters are measured at test hardware SMA connector
2. Transceiver power consumption, Pout = 0 dBm
3. Measured at the KW40 RF pins
4. Measured as per IEEE Std. 802.15.4-2011
5. Offset EVM is computed at one point per symbol, by combining the I value from the beginning of each symbol and the Q value from the middle of each symbol into a single complex value for EVM computations

6. Measured at Pout = 5dBm and recommended TX match
7. Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32MHz reference crystal

6 MCU Electrical Characteristics

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

6.2 Nonswitching electrical specifications

6.2.1 Voltage and current operating requirements

Table 8. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	

Table continues on the next page...

Table 8. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

6.2.2 LVD and POR operating requirements

Table 9. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1

Table continues on the next page...