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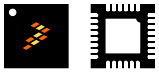
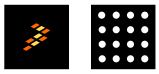
MKW41Z/31Z/21Z Data Sheet

A Bluetooth® Low Energy, IEEE® Standard 802.15.4, Generic FSK System on a Chip (SoC) Supports the following: MKW41Z512VHT4, MKW31Z512VHT4, MKW21Z512VHT4, MKW41Z256VHT4, MKW31Z256VHT4, MKW21Z256VHT4,MKW41Z512CAT4,MKW31Z512CAT4

MKW41Z512
MKW31Z512
MKW21Z512
MKW41Z256
MKW31Z256
MKW21Z256



48 LQFN
7 x 7 x 0.98 mm Pitch 0.5 mm



75 WLCSP
3.893 x 3.797 x 0.564 mm Pitch 0.4 mm

Multi-Standard Radio

- 2.4 GHz Bluetooth Low Energy ver. 4.2 compliant supporting up to 2 simultaneous hardware connections
- IEEE Std. 802.15.4 compliant with dual-PAN support
- Generic FSK modulation
  - Data Rate: 250, 500 and 1000 kbps
  - Modulations: GFSK BT = 0.3, 0.5, 0.7; FSK/MSK
  - Modulation Index: 0.32, 0.5, or 0.7
- Typical Receiver Sensitivity (BLE) = -95 dBm
- Typical Receiver Sensitivity (802.15.4) = -100 dBm
- Typical Receiver Sensitivity (250 kbps GFSK-BT=0.5, h=0.5) = -100 dBm
- Prog Transmitter Output Power: -30 dBm to 3.5 dBm
- Low external component counts for low cost application
- On-chip balun with single ended bidirectional RF port

MCU and Memories

- Up to 48 MHz ARM® Cortex-M0+ core
- On-chip 512/256 KB Flash memory
- On-chip 128/64 KB SRAM

Low Power Consumption

- Transceiver current (DC-DC buck mode, 3.6 V supply)
  - Typical Rx Current: 6.8 mA
  - Typical Tx current: 6.1 mA (0 dBm output)
- Low Power Mode (VLLS0) Current: 182 nA

System peripherals

- Nine MCU low-power modes to provide power optimization based on application requirements
- DC-DC Converter supporting Buck, Boost, and Bypass operating modes
- Direct memory access(DMA) Controller
- Computer operating properly(COP) watchdog
- Serial wire debug(SWD) Interface and Micro Trace buffer
- Bit Manipulation Engine (BME)

Analog Modules

- 16-bit Analog-to-Digital Converter (ADC)
- 12-bit Digital-to-Analog Converter (DAC)
- 6-bit High Speed Analog Comparator (CMP)
- 1.2 V voltage reference (VREF)

Timers

- 16-bit low-power timer (LPTMR)
- 3 Timers Modules(TPM): One 4 channel TPM and two 2 channel TPMs
- Programmable Interrupt Timer (PIT)
- Real-Time Clock (RTC)

Communication interfaces

- 2 serial peripheral interface (SPI) modules
- 2 inter-integrated circuit (I2C) modules

Clocks

- 26 and 32 MHz supported for BLE and FSK modes
- 32 MHz supported for IEEE Standard 802.15.4
- 32.768 kHz Crystal Oscillator

Operating Characteristics

- Voltage range: 0.9 V to 4.2 V
- Temperature range:
  - –40 to 105 °C (Laminate-QFN)
  - –40 to 85 °C (WLCSP)

Human-machine interface

- Touch sensing input
- General-purpose input/output
- Low Power UART module
- Carrier Modulator Timer (CMT)

Security

- AES-128 Hardware Accelerator (AESA)
- True Random Number Generator (TRNG)
- Advanced flash security
- 80-bit unique identification number per chip
- 40-bit unique media access control (MAC) sub-address
- Bluetooth-LE v4.2 Secure Connections
- IEEE Standard 802.15.4-2011 compliant security

Table of Contents

1 Introduction

The KW41Z/31Z/21Z (called KW41Z throughout this document) is an ultra low-power, highly integrated single-chip device that enables Bluetooth low energy (BLE), Generic FSK (at 250, 500 and 1000 kbps) or IEEE Standard 802.15.4 RF connectivity for portable, extremely low-power embedded systems. Applications include portable health care devices, wearable sports and fitness devices, AV remote controls, computer keyboards and mice, gaming controllers, access control, security systems, smart energy and home area networks.

The KW41Z SoC integrates a radio transceiver operating in the 2.36 GHz to 2.48 GHz range supporting a range of FSK/GFSK and O-QPSK modulations, an ARM Cortex-M0+ CPU, up to 512 KB Flash and up to 128 KB SRAM, BLE Link Layer hardware, 802.15.4 packet processor hardware and peripherals optimized to meet the requirements of the target applications.

The KW41Z SoC's radio frequency transceiver is compliant with Bluetooth version 4.2 for Low Energy (aka Bluetooth Smart or BLE), Generic FSK and the IEEE Standard 802.15.4 using O-QPSK in the 2.4 GHz ISM band. NXP provides fully certified Bluetooth Low Energy and IEEE Standard 802.15.4 protocol stacks, including Zigbee 3.0, Thread, and application profiles to support KW41Z.

The KW41Z SoC can be used in applications as a "BlackBox" modem by simply adding BLE or IEEE Standard 802.15.4 connectivity to an existing embedded controller system, or used as a stand-alone smart wireless sensor with embedded application where no host controller is required.

KW41Z has 512/256 KB of on-chip Flash and 128/64 KB of on-chip SRAM memory available to be used by customer applications and chosen communication protocol stack using a choice of either NXP or 3rd party software development tools.

The RF section of the KW41Z SoC is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board.

Extremely long battery life is achieved though efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW41Z SoC. Additionally, an integrated DC-DC converter enables a wide operating range from 0.9 V to 4.2 V. The DC-DC in Buck mode enables KW41Z to operate from a single coin cell battery with a significant reduction of peak Rx and Tx current consumption. The DC-DC in boost mode enables a single alkaline battery to be used throughout its entire useful voltage range of 0.9 V to 1.795 V.

2 Ordering Information

Table 1. Orderable parts details

Device	Part Marking	Memory Configuration	Package	Description
MKW21Z512VHT4(R)	M21W9VT4	512 KB Flash 128 KB SRAM	48-pin Laminate QFN	IEEE 802.15.4
MKW21Z256VHT4(R)	M21W8VT4	256 KB Flash 64 KB SRAM		
MKW31Z512CAT4R	MKW31Z512CAT4	512 KB Flash 128 KB SRAM	75-pin WLCSP	Bluetooth Low Energy and Generic FSK
MKW31Z512VHT4(R)	M31W9VT4	512 KB Flash 128 KB SRAM	48-pin Laminate QFN	Bluetooth Low Energy and Generic FSK
MKW31Z256VHT4(R)	M31W8VT4	256 KB Flash 64 KB SRAM		
MKW41Z512CAT4R	MKW41Z512CAT4	512 KB Flash 128 KB SRAM	75-pin WLCSP	Bluetooth Low Energy and IEEE 802.15.4 and Generic FSK
MKW41Z512VHT4(R)	M41W9VT4	512 KB Flash 128 KB SRAM	48-pin Laminate QFN	Bluetooth Low Energy and IEEE 802.15.4 and Generic FSK
MKW41Z256VHT4(R)	M41W8VT4	256 KB Flash 64 KB SRAM		

3 Feature Descriptions

This section provides a simplified block diagram and highlights the KW41Z features.

3.1 Block Diagram

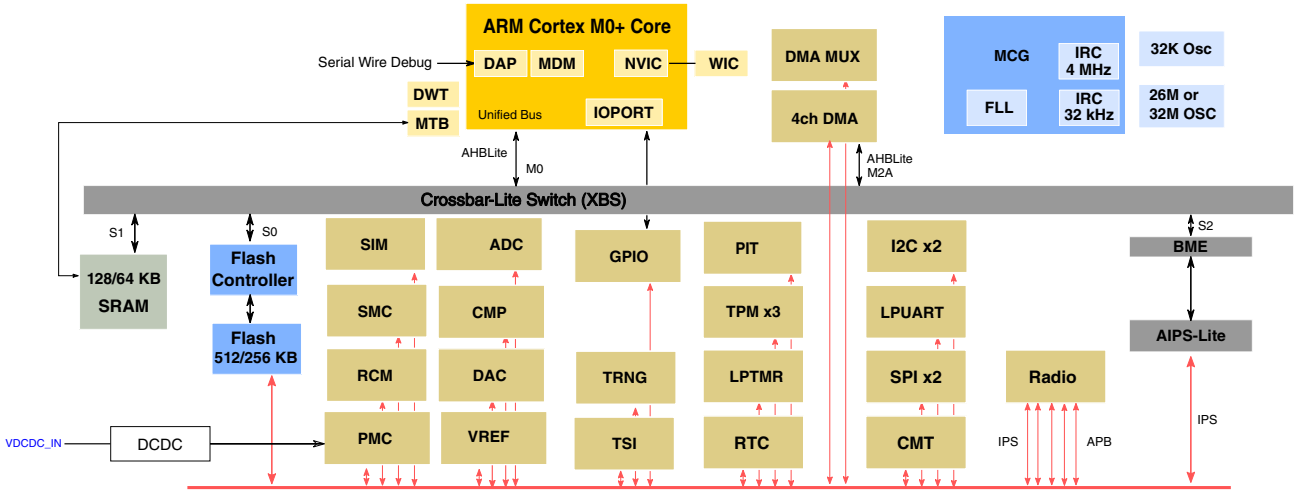


Figure 1. KW41Z Detailed Block Diagram

3.2 Radio features

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- MBAN 2360-2400 MHz

Supported standards:

- Bluetooth v4.2 Low Energy compliant 1 Mbps GFSK modulation supporting up to 2 simultaneous connections in hardware (master-slave, master-master, slave-slave)
- IEEE Standard 802.15.4-2011 compliant O-QPSK modulation and security features
- Zigbee 3.0
- Thread Networking Stack
- Bluetooth Low Energy(BLE) Application Profiles

Receiver performance:

- Receive sensitivity of -95 dBm for BLE
- Receive sensitivity of -100 dBm typical for IEEE Standard 802.15.4
- Receive sensitivity of up to -100 dBm for a 250 kbps GFSK mode with a modulation index of 0.5. Receive sensitivity in generic FSK modes depends on mode selection and data rate.

Other features:

- Programmable transmit output power from -30 dBm to 3.5 dBm
- Integrated on-chip balun
- Single ended bidirectional RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA
- 26 and 32 MHz supported for BLE and FSK modes
- 32 MHz supported for IEEE Standard 802.15.4
- Bluetooth Low Energy ver. 4.2 Link Layer hardware with 2 independent hardware connection engines
- Hardware acceleration for IEEE Standard 802.15.4 packet processing/link layer
- Hardware acceleration for Generic FSK packet processing
- Supports dual PAN for IEEE Standard 802.15.4 with hardware-assisted address matching acceleration
- Generic FSK modulation at 250, 500 and 1000 kbps
- Supports antenna diversity option for IEEE Std. 802.15.4

3.3 Microcontroller features

ARM Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes

- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

Debug Controller

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

On-Chip Memory

- 512/256 KB
  - Firmware distribution protection. Program flash can be marked execute-only on a per-sector (8 KB) basis to prevent firmware contents from being read by third parties
  - Flash implemented as two equal blocks each of 256 KB block. Code can execute or read from one block while the other block is being erased or programmed.
- 128/64 KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

3.4 System features

Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

DC-DC Converters

- Internal switched mode power supply supporting Buck, Boost, and Bypass operating modes
- Buck operation supports external voltage sources of 2.1 V to 4.2 V. This reduces peak current consumption during Rx and Tx by ~25%, ideal for single coin-cell battery operation (typical CR2032 cell).
- Boost operation supports external voltage sources of 0.9 V to 1.795 V, which is efficiently increased to the static internal core voltage level, ideal for single battery operation (typical AA or AAA alkaline cell).
- When DC-DC is not used, the device supports an external voltage range of 1.5 V to 3.6 V (1.5 - 3.6 V on VDD_RF1, VDD_RF2, VDD_XTAL and VDD_1P5OUT_PMCIN pins. 1.71 - 3.6 V on VDD_0, VDD_1 and VDDA pins)
- An external inductor is required to support the Buck or Boost modes
- The DC-DC Converter 1.8 V output current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
  - Up to 44 mA in buck mode with VDD_1P8 = 1.8 V
  - Up to 31.4 mA in buck mode with VDD_1P8 = 3.0 V

Direct Memory Access (DMA) Controller

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses and transfer size
- Support for enhanced addressing modes
- 4-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
- Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests

- One interrupt per channel, optionally asserted at completion of major iteration count
- Optional error terminations per channel and logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing
- Support for complex data structures

DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

System Clocks

- Both 26 MHz and 32 MHz crystal reference oscillator supported for BLE and FSK radio modes
- 32 MHz crystal reference oscillator supported for IEEE 802.15.4 radio mode
- MCU can derive its clock either from the crystal reference oscillator or the frequency locked loop (FLL)[1]
- 32.768 kHz crystal reference oscillator used to maintain precise Bluetooth radio time in low power modes
- Multipurpose Clock Generator (MCG)
- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
  - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 2% accuracy across full temperature range
  - On-chip 4MHz oscillator with 5% accuracy across full temperature range
- Frequency-locked loop (FLL) controlled by internal or external reference
  - 20 MHz to 48 MHz FLL output

Unique Identifiers

- 10 bytes(or 80-bits) of the Unique ID represents a unique identifier for each chip
- 40 bits of unique media access control (MAC) address, which can be used to build a unique 48-bit Bluetooth-LE or 64-bit IEEE 802.15.4 device address

1. Clock options can have restrictions based on the chosen SoC configuration.

3.5 Peripheral features

16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in differential-ended 16-, 13-, 11-, and 9-bit mode
- Output formatted in single-ended 16-, 12-, 10-, and 8-bit mode
- Single or continuous conversion
- Configurable sample time and conversion speed / power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor
- Battery voltage measurement
- Hardware average function
- Selectable voltage reverence
- Self-calibration mode

12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1 μs conversion rate for high speed, 2 μs for low speed
- Power-down mode
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output

- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except VLLS0 mode

Voltage Reference(VREF1)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
  - Off
  - Bandgap enabled/standby (output buffer disabled)
  - High power buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- VREF_OUT output signal

Low Power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency

Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
  - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires MCU POR to enable write access
  - Soft lock requires POR or software reset to enable write/read access
- Capable of waking up the system from low power modes

Inter-Integrated Circuit (I^2C)

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 400 kHz operation
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

LPUART

- One channel
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:

    - Idle line wakeup
    - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes

Serial Peripheral Interface (DSPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

Carrier Modulator Timer (CMT)

- Four modes of operation
    - Time; with independent control of high and low times
    - Baseband
    - Frequency shift key (FSK)
    - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wakeup events
- Configurable drive strength on some output pins

Touch Sensor Input (TSI)

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes
- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times
- Support DMA data transfer

Keyboard Interface

- GPIO can be configured to function as a interrupt driven keyboard scanning matrix
  - In the 48-pin package there are a total of 26 digital pins
  - These pins can be configured as needed by the application as GPIO, LPUART, SPI, I2C, ADC, timer I/O as well as other functions

3.6 Security Features

Advanced Encryption Standard Accelerator(AES-128 Accelerator)

The advanced encryption standard accelerator (AESA) module is a standalone hardware coprocessor capable of accelerating the 128-bit advanced encryption standard (AES) cryptographic algorithms.

The AESA engine supports the following cryptographic features.

LTC includes the following features:

- Cryptographic authentication
  - Message authentication codes (MAC)
    - Cipher-based MAC (AES-CMAC)
    - Extended cipher block chaining message authentication code (AES-XCBC-MAC)
  - Auto padding
  - Integrity Check Value(ICV) checking
- Authenticated encryption algorithms
  - Counter with CBC-MAC (AES-CCM)
  - Galois counter mode (AES-GCM)

- Symmetric key block ciphers
  - AES (128-bit keys)
  - Cipher modes:
    - AES-128 modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Counter (CTR)
    - DES modes
      - Electronic codebook (ECB)
      - Cipher block chaining (CBC)
      - Cipher feedback (CFB)
      - Output Feedback (OFB)
- Secure scan

True Random Number Generator (TRNG)

True Random Number Generator (TRNG) is a hardware accelerator module that constitutes a high-quality entropy source.

- TRNG generates a 512-bit (4x 128-bit) entropy as needed by an entropy-consuming module, such as a deterministic random number generator.
- TRNG output can be read and used by a deterministic pseudo-random number generator (PRNG) implemented in software.
- TRNG-PRNG combination achieves NIST compliant true randomness and cryptographic-strength random numbers using the TRNG output as the entropy source.
- A fully FIPS 180 compliant solution can be realized using the TRNG together with a FIPS compliant deterministic random number generator and the SoC-level security.

Flash Memory Protection

The on-chip flash memory controller enables the following useful features:

- Program flash protection scheme prevents accidental program or erase of stored data.
- Program flash access control scheme prevents unauthorized access to selected code segments.
- The flash can be protected from mass erase even when the MCU is not secured.
- Automated, built-in, program and erase algorithms with verify.
- Read access to one program flash block is possible while programming or erasing data in the other program flash block.

4 Transceiver Description

- Direct Conversion Receiver
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

4.1 Key Specifications

The KW41Z SoC meets or exceeds all Bluetooth Low Energy v4.2 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specification for the KW41 are:

Frequency Band:

- ISM Band: 2400 to 2483.5MHz
- MBAN Band: 2360 to 2400MHz

Bluetooth Low Energy v4.2 modulation scheme:

- Symbol rate: 1000 kbps
- Modulation: GFSK
- Receiver sensitivity: -95 dBm, typical
- Programmable transmitter output power: -30 dBm to 3.5 dBm

IEEE Standard 802.15.4 2.4 GHz modulation scheme:

- Chip rate: 2000 kbps
- Data rate: 250 kbps
- Symbol rate: 62.5 kbps
- Modulation: OQPSK
- Receiver sensitivity: -100 dBm, typical (@1% PER for 20 byte payload packet)
- Single ended bidirectional RF input/output port with integrated transmit/receive switch
- Programmable transmitter output power: -30 dBm to 3.5 dBm

Generic FSK modulation scheme:

- Symbol rate: 250, 500 and 1000 kbps

- Modulation(s): GFSK (modulation index = 0.32, 0.5, and 0.7, BT =0.5, 0.3 and 0.7), MSK
- Receiver Sensitivity: Mode and data rate dependant. -100 dBm typical for GFSK (r=250 kbps, BT = 0.5, h = 0.5)

4.2 Channel Map Frequency Plans

4.2.1 Channel Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4 GHz ISM Channel numbering:

- Fc=2402 + k * 2 MHz, k=0,.....,39.

MBAN Channel numbering:

- Fc=2363 + 5*k in MHz, for k=0,.....,6
- Fc=2367 + 5*(k-7) in MHz, for k=7,8.....,13)

where k is the channel number.

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
0	2402	0	2360	28	2390
1	2404	1	2361	29	2391
2	2406	2	2362	30	2392
3	2408	3	2363	31	2393
4	2410	4	2364	32	2394
5	2412	5	2365	33	2395
6	2414	6	2366	34	2396
7	2416	7	2367	35	2397
8	2418	8	2368	36	2398
9	2420	9	2369	0	2402
10	2422	10	2370	1	2404

Table continues on the next page...

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
11	2424	11	2371	2	2406
12	2426	12	2372	3	2408
13	2428	13	2373	4	2410
14	2430	14	2374	5	2412
15	2432	15	2375	6	2414
16	2434	16	2376	7	2416
17	2436	17	2377	8	2418
18	2438	18	2378	9	2420
19	2440	19	2379	10	2422
20	2442	20	2380	11	2424
21	2444	21	2381	12	2426
22	2446	22	2382	13	2428
23	2448	23	2383	14	2430
24	2450	24	2384	15	2432
25	2452	25	2385	16	2434
26	2454	26	2386	17	2436
27	2456	27	2387	18	2438
28	2458	28	2388	19	2440
29	2460	29	2389	20	2442
30	2462	30	2390	21	2444
31	2464	31	2391	22	2446
32	2466	32	2392	23	2448
33	2468	33	2393	24	2450
34	2470	34	2394	25	2452
35	2472	35	2395	26	2454
36	2474	36	2396	27	2456
37	2476	37	2397	37	2476
38	2478	38	2398	38	2478
39	2480	39	2399	39	2480

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, IEEE (R) 802.15.1 and Bluetooth Low Energy single mode operation is allowed in these channels.

4.2.2 Channel Plan for IEEE 802.15.4 in 2.4GHz ISM and MBAN frequency bands

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for IEEE 802.15.4.

2.4GHz ISM Channel numbering:

- Fc=2405 + 5*(k-11) MHz, k=11, 12, ..,26.

MBAN Channel numbering:

- Fc=2363.0 + 5*k in MHz, for k=0,.....,6
- Fc=2367.0 + 5*(k-7) in MHz, for k=7,.....,14

where k is the channel number.

Table 3. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
11	2405	0	2363
12	2410	1	2368
13	2415	2	2373
14	2420	3	2378
15	2425	4	2383
16	2430	5	2388
17	2435	6	2393
18	2440	7	2367
19	2445	8	2372
20	2450	9	2377
21	2455	10	2382
22	2460	11	2387
23	2465	12	2392
24	2470	13	2397
25	2475	14	2395
26	2480		

1. Usable channel spacing to assit in co-existence.

4.2.3 Other Channel Plans

The RF synthesizer can be configured to use any channel frequency between 2.36 and 2.487 GHz.

4.3 Transceiver Functions

Receive

The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing/link-layer processing.

Transmit

The transmitter transmits O-QPSK or GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RF_P, RF_N) are converted to a single ended(SE) output signal by an on-chip balun.

5 Transceiver Electrical Characteristics

5.1 Radio operating conditions

Table 4. Radio operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Input Frequency	f_{in}	2.360	—	2.480	GHz
Ambient Temperature Range	T_A	-40	25	105	°C
Logic Input Voltage Low	V_{IL}	0	—	30% VDD_{INT} [1]	V

Table continues on the next page...

Table 4. Radio operating conditions (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic Input Voltage High	V_{IH}	70% VDD_{INT}	—	VDD_{INT}	V
SPI Clock Rate	f_{SPI}	—	—	12.0	MHz
RF Input Power	P_{max}	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	f_{ref}	26 MHz or 32 MHz			

1. VDD_{INT} is the internal LDO regulated voltage supplying various circuit blocks, VDD_{INT}=1.2 V

5.2 Receiver Feature Summary

Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	1000	nA
Supply current Rx On with DC-DC converter enable (Buck; VDD_{DCDC_in} = 3.6 V) [2]	I_{Rxon}	—	6.76	—	mA
Supply current Rx On with DC-DC converter disabled (Bypass) [2]	I_{Rxon}	—	16.2	—	mA
Input RF Frequency	f_{in}	2.360	—	2.4835	GHz
GFSK Rx Sensitivity(250 kbps GFSK-BT=0.5, h=0.5)	$SENS_{GFSK}$	—	-100	—	dBm
BLE Rx Sensitivity [3]	$SENS_{BLE}$	—	-95	—	dBm
IEEE 802.15.4 Rx Sensitivity [4]	$SENS_{15.4}$	—	-100	—	dBm
Noise Figure for max gain mode @ typical sensitivity	NF_{HG}	—	7.5	—	dB
Receiver Signal Strength Indicator Range[5]	$RSSI_{Range}$	-100	—	5	dBm
Receiver Signal Strength Indicator Resolution	$RSSI_{Res}$	—	1	—	dBm
Typical RSSI variation over frequency		-2	—	2	dB
Typical RSSI variation over temperature		-2	—	2	dB
Narrowband RSSI accuracy[6]	$RSSI_{Acc}$	-3	—	3	dB
BLE Co-channel Interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).	$BLE_{co\text{-}channel}$		-7		dB
IEEE 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)	$15.4_{co\text{-}channel}$	—	-2	—	dB
Adjacent/Alternate Channel Performance[7]					
BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 1\ MHz}$	—	2	—	dB

Table continues on the next page...

Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE, 2\ MHz}$	—	40	—	dB
BLE Alternate ≥ +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE, 3\ MHz}$	—	50	—	dB
IEEE 802.15.4 Adjacent +/- 5 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%)	$SEL_{15.4,5\ MHz}$	—	45	—	dB
IEEE 802.15.4 Alternate ≥ +/- 10 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%.)	$SEL_{15.4,5\ MHz}$	—	60	—	dB
Intermodulation Performance					
BLE Intermodulation with continuous wave interferer at ± 3MHz and modulated interferer is at ± 6MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-42	—	dBm
BLE Intermodulation with continuous wave interferer at ±5MHz and modulated interferer is at ±10MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-35	—	dBm
Blocking Performance[7]					
BLE Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[8]	—	—	-5	—	dBm
BLE Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	—	-12	—	dBm
BLE Out of band blocking from 2001 MHz to 2339MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	—	-20	—	dBm
BLE Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[8]	—	—	0	—	dBm
IEEE 802.15.4 Out of band blocking for frequency offsets > 10 MHz and <= 80 MHz(Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)[9]		—	-36	—	dBm
IEEE 802.15.4 Out of band blocking from carrier frequencies in 1GHz to 4GHz range excluding frequency offsets < ±80 MHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)		—	-25	—	dBm
IEEE 802.15.4 Out of band blocking frequency from carrier frequencies < 1 GHz and > 4 GHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.[8]		—	-15	—	dBm

Table continues on the next page...

Table 5. Top Level Receiver Specifications (TA=25°C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|< 1.6 MHz	—	—	-54	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|> 2.5 MHz[10]	—	—	-70	—	dBc

1. All the RX parameters are measured at the KW41 RF pins
2. Transceiver power consumption
3. Measured at 0.1% BER using 37 byte long packets in max gain mode and nominal conditions
4. In max gain mode and nominal conditions
5. RSSI performance in narrowband mode
6. With one point calibration over frequency and temperature
7. BLE Adjacent and Block parameters are measured with modulated interference signals
8. Exceptions allowed for carrier frequency harmonics.
9. Exception to the 10 MHz > freq offset <= 80 MHz out-of-band blocking limit allowed for frequency offsets of twice the reference frequency(fref).
10. Exceptions allowed for twice the reference clock frequency(fref) multiples.

Table 6. Receiver Specifications with Generic FSK Modulations

				Adjacent/Alternate Channel Selectivity (dB)[1]					
Modulation Type	Data Rate (kbps)	Channel BW (kHz)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+1* channel BW offset	Interferer at -/+ 2* channel BW offset	Interferer at -/+ 3* channel BW offset	Interferer at -/+ 4* channel BW offset	Co-channel
GFSK BT = 0.5, h=0.5	1000	2000	-95	-67	45	50	52	52	-7
	500	1000	-97	-85	33	44	49	51	-7
	250	500	-100	-85	20	33	42	46	-7
GFSK, BT = 0.5, h=0.3	1000	1000	-89	-67	30	36	41	42	-7
	500	800	-91	-85	25	36	37	43	-13
	250	500	-93	-85	25	25	37	37	-13
GFSK, BT = 0.5, h=0.7	1000	2000	-96	-85	35	45	50	55	-7
	500	1000	-98	-85	32	44	47	50	-7
	250	600	-99	-85	30	34	46	45	-7
GMSK BT=0.3	1000	1600	-91	-85	35	40	45	50	-8
	500	800	-93	-85	30	40	40	45	-7
	250	500	-95	-85	20	32	32	40	-7
GMSK, BT = 0.7	1000	2000	-96	-85	35	45	50	55	-7
	500	1000	-97	-85	30	45	48	50	-7

Table continues on the next page...

Table 6. Receiver Specifications with Generic FSK Modulations (continued)

				Adjacent/Alternate Channel Selectivity (dB)[1]					
Modulation Type	Data Rate (kbps)	Channel BW (kHz)	Typical Sensitivity (dBm)	Desired signal level (dBm)	Interferer at -/+1* channel BW offset	Interferer at -/+ 2* channel BW offset	Interferer at -/+ 3* channel BW offset	Interferer at -/+ 4* channel BW offset	Co-channel
Generic MSK	250	600	-99	-85	30	33	45	45	-7
	1000	3000	-96	-85	39	50	58	63	-7
	500	1600	-98	-85	38	47	50	55	-7
	250	800	-99	-85	30	46	45	50	-7

1. Selectivity measured with an unmodulated blocker

5.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 25 µs
- Reference Frequency:
  - 26 and 32 MHz supported for BLE and FSK modes
  - 32 MHz supported for IEEE Standard 802.15.4

Table 7. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	—	nA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter enabled (Buck; VDD_{DCDC_in} = 3.6 V) [2]	I_{Txone}	—	6.08	—	mA
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass) [2]	I_{Txond}	—	14.7	—	mA
Output Frequency	f_c	2.360	—	2.4835	GHz
Maximum RF Output power [3]	$P_{RF,max}$	—	3.5	—	dBm
Minimum RF Output power [3]	$P_{RF,min}$	—	-30	—	dBm
RF Output power control range	P_{RFCR}	—	34	—	dB
IEEE 802.15.4 Peak Frequency Deviation	$F_{dev15.4}$	—	±500	—	kHz
IEEE 802.15.4 Error Vector Magnitude[4]	$EVM_{15.4}$		4.5	8	%
IEEE 802.15.4 Offset Error Vector Magnitude[5]	$OEVM_{15.4}$		0.5	2	%
IEEE 802.15.4 TX spectrum level at 3.5MHz offset[4, 6]	$TXPSD_{15.4}$			-40	dBc
BLE TX Output Spectrum 20dB BW	$TXBW_{BLE}$	1.0		—	MHz

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