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ML610Q407/ML610Q408/ML61Q0409

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610Q407/ML610Q408/ML610Q409 is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor-original 8-bit CPU nX-U8/100. ML610Q407/ML610Q408/ML610Q409 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

The short TAT are entertained by offering MTP version ML610Q407(P)/ML610Q408(P)/ML610Q409(P).

ML610Q407P/ ML610Q408P/ML610Q409P support industrial temperature -40°C to +85°C, are added to the product lineup.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function (MTP version only)
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    2μs (@500kHz system clock)
    0.5μs(@2MHz system clock)

- Internal memory
  - Internal 16KByte Flash ROM (8K×16 bits) (including unusable 1K Byte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt sources
    Internal source: 1 (Watch dog timer)
  - 27 maskable interrupt sources
    Internal sources: 14 (SSIO0, SSIO1, Timer0, Timer1, Timer2, Timer3, UART0, Melody0, RC-A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External sources: 13 (P00, P01, P02, P03, P04, P50, P51, P52, P53, P54, P55, P56, P57)
    (One interrupt request is generated from P50 to P57 interrupt sources.)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. −488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable × 2 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 16-bit counter
  - Time division × 2 channels

- General-purpose ports
  - Input-only port × 5 channels (including secondary functions)
  - Output-only port
    ML610Q407: × 12 channels (including secondary functions)
    ML610Q408: × 8 channels (including secondary functions)
    ML610Q409: × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)

- LCD driver
  - The number of segments
    ML610Q407: 145 dots max. (29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable)
    ML610Q408: 165 dots max. (33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable)
    ML610Q409: 185 dots max. (37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable)
  - 1/1 to 1/5 duty
  - 1/2(*), 1/3 bias (built-in bias generation circuit)
  - Frame frequency selecable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function
  (*) 1/2 bias is supported by A version and D version

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected (Not supported in A version)
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock: Crystal oscillation (32.768 kHz)
    (This LSI can not guarantee the operation withoug low-speed crystal oscillation clock)
  - High-speed clock: Built-in RC oscillation (500 kHz, 2MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Guaranteed operating range
  - Operating temperature: −20°C to +70°C (P version: −40°C to +85°C)
  - Operating voltage: V_{DD} = 1.25V to 3.6V

● Product name – Supported Function

- Chip (Die) -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610Q407-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q408-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q409-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q407P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q408P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q409P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q407A- x x x WA	Yes	Yes	-	-20°C to +70°C	Yes
ML610Q408A-xxxWA	Yes	Yes	-	-20°C to +70°C	-
ML610Q409A-xxxWA	Yes	Yes	-	-20°C to +70°C	Yes
ML610Q407D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	Yes
ML610Q408D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q409D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q407PA-xxxWA	Yes	Yes	-	-40°C to +85°C	Yes
ML610Q408PA-xxxWA	Yes	Yes	-	-40°C to +85°C	-
ML610Q409PA-xxxWA	Yes	Yes	-	-40°C to +85°C	-
ML610Q407PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q408PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q409PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-

-100-pin plastic TQFP -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610Q407-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q408-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q409-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q407P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q408P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q409P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q407A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q408A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q409A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q407D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q408D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q409D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q407PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q408PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q409PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q407PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q408PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q409PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-

xxx: ROM code number (xxx of the blank product is NNN)
Q: MTP version
P: Wide range temperature version (P version)
A: Low-speed clock oscillation stop detection reset is disabled always and LCD 1/2 bias supported version.(A version)
D: LCD 1/2 bias supported version (D version)
WA: Chip (Die),   TB: TQFP

BLOCK DIAGRAM
ML610Q407/ML610Q408/ML610Q409 Block Diagram

Figure 1 show the block diagram of the ML610Q407/ML610Q408/ML610Q409.

"*" indicates the secondary function of each port.

"(*1)": 29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable

"(*2)": 33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable

"(*3)": 37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable
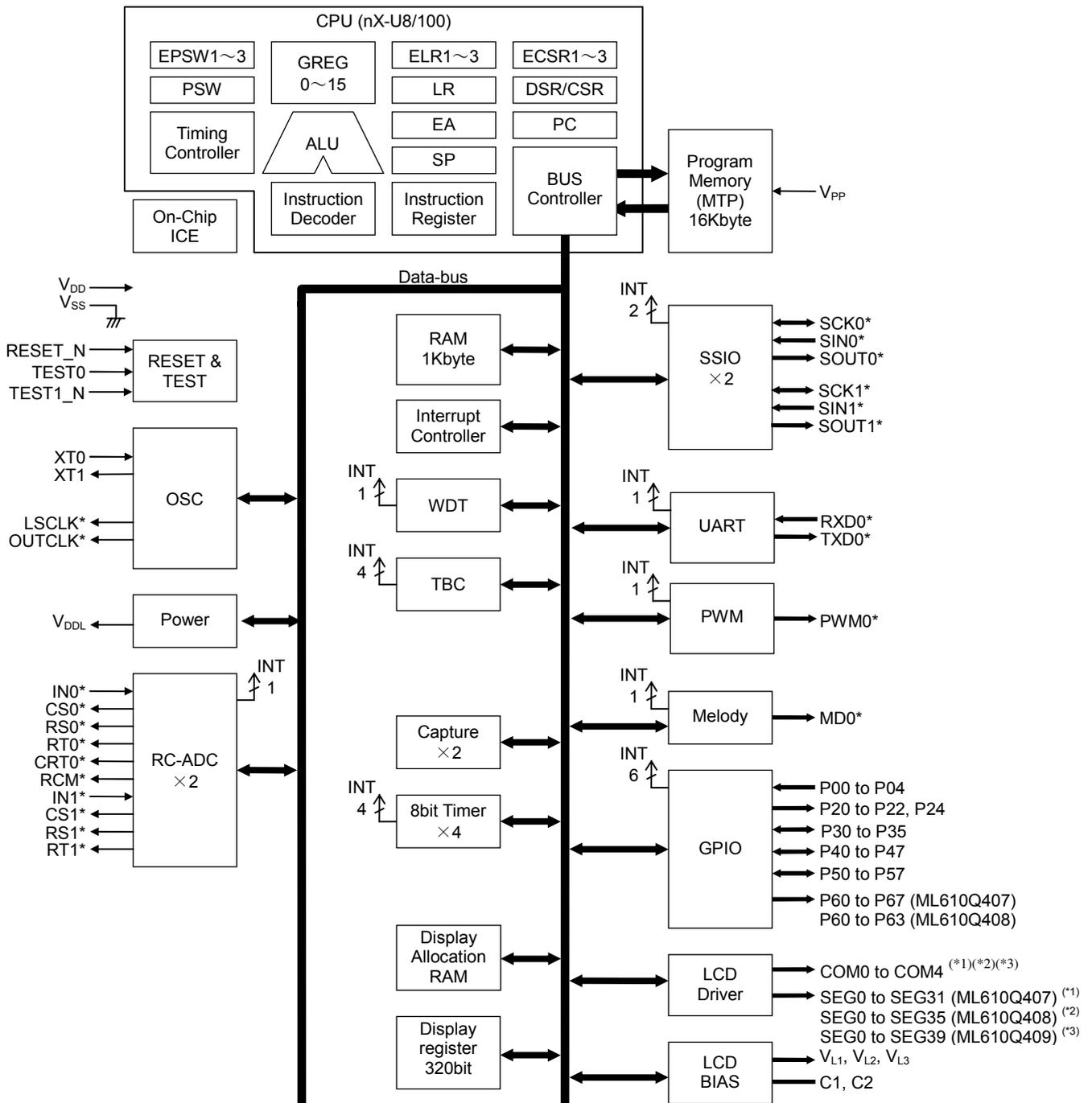
Figure 1 ML610Q407/ML610Q408/ML610Q409 Block Diagram

PIN CONFIGURATION

ML610Q407 TQFP100 Pin Layout
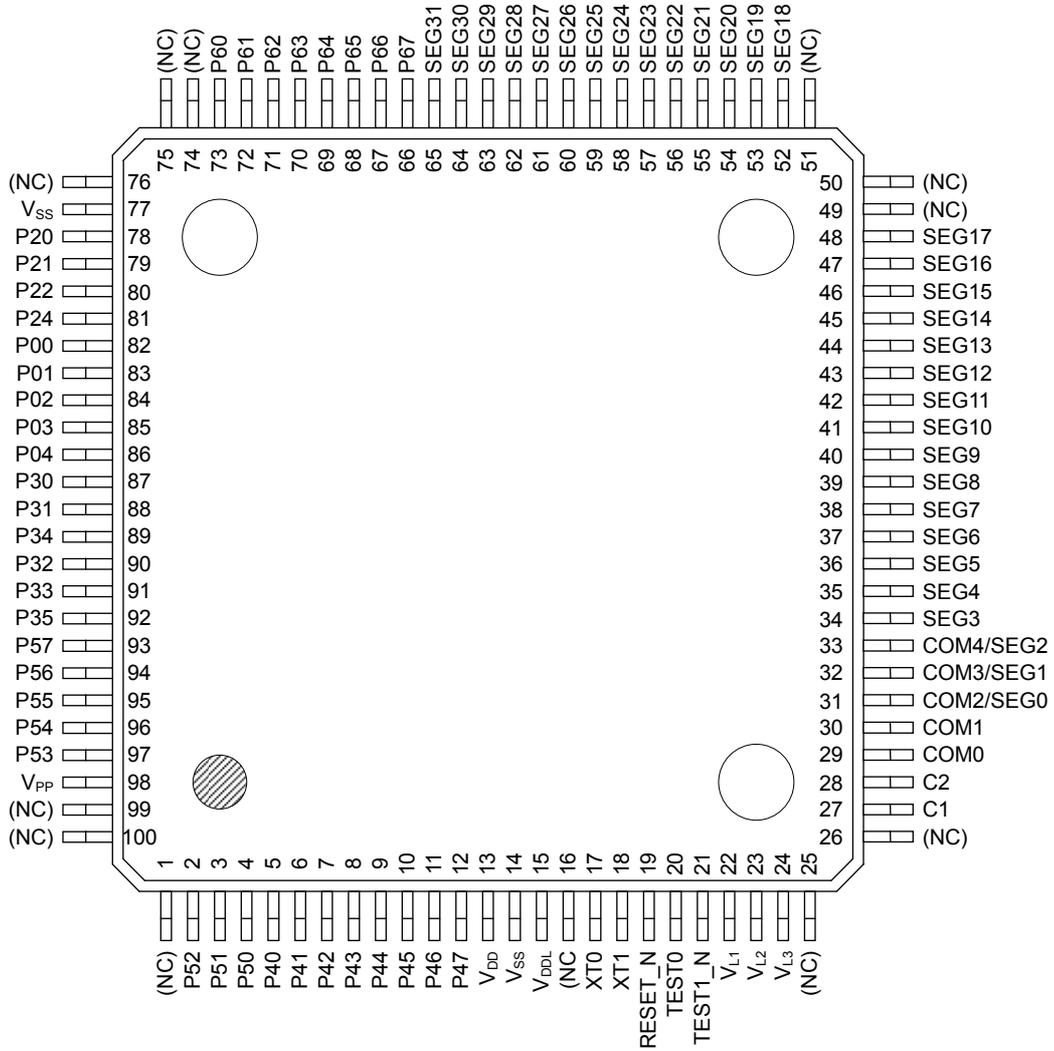
Note:
The assignment of the P30 to P35 are not in order.

Figure 2 ML610Q407 TQFP100 Pin Configuration

ML610Q408 TQFP100 Pin Layout
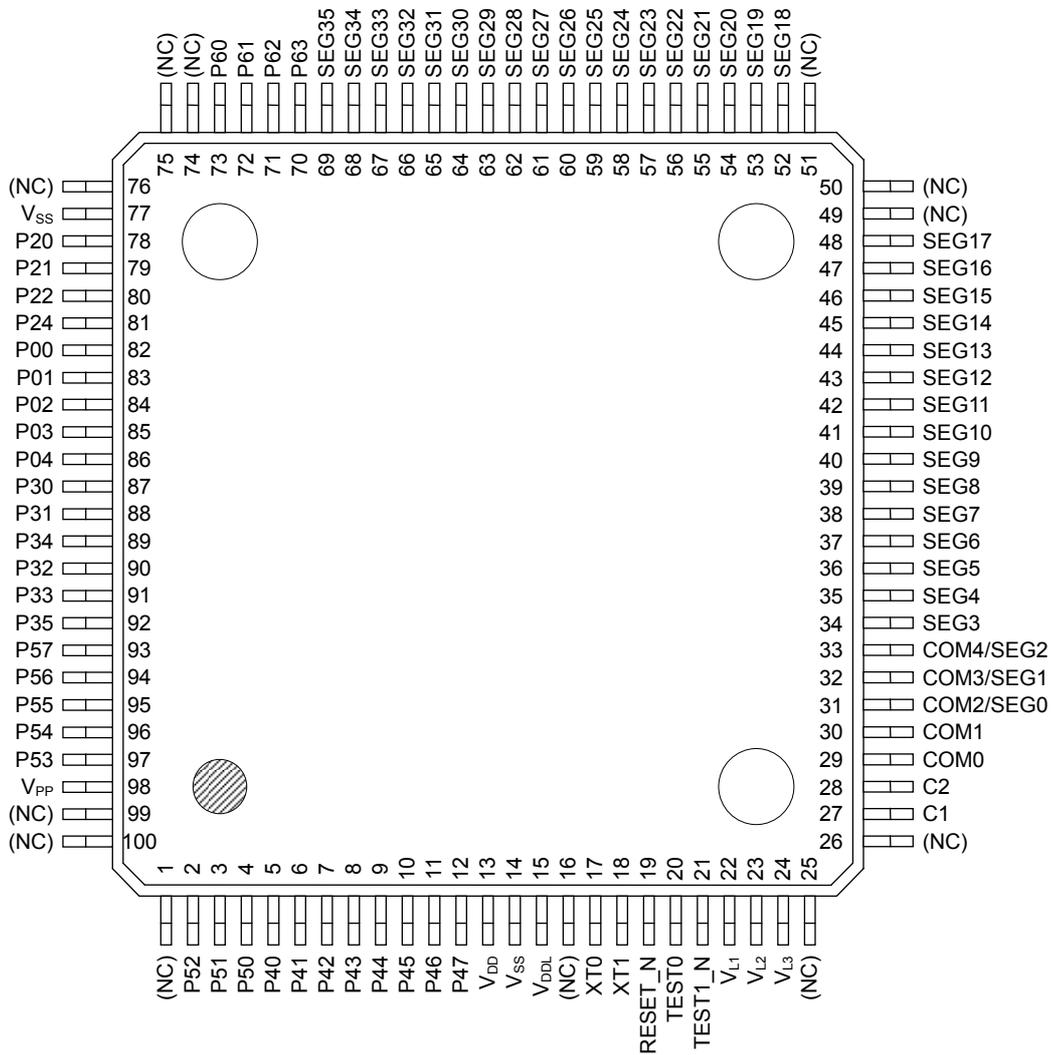
Note:
The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q408 TQFP100 Pin Configuration

ML610Q409 TQFP100 Pin Layout
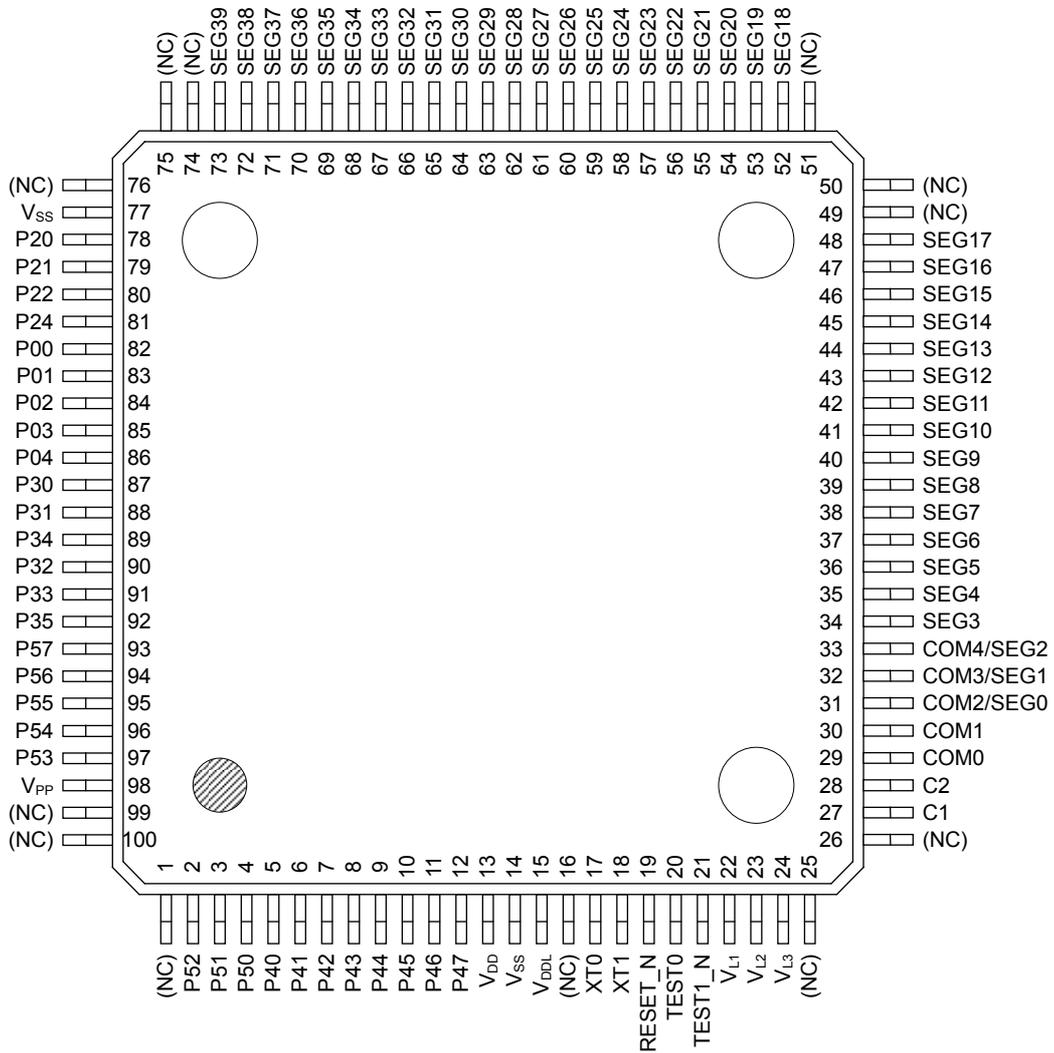
Note:
The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q409 TQFP100 Pin Configuration

ML610Q407 Chip Pin Layout & Dimension
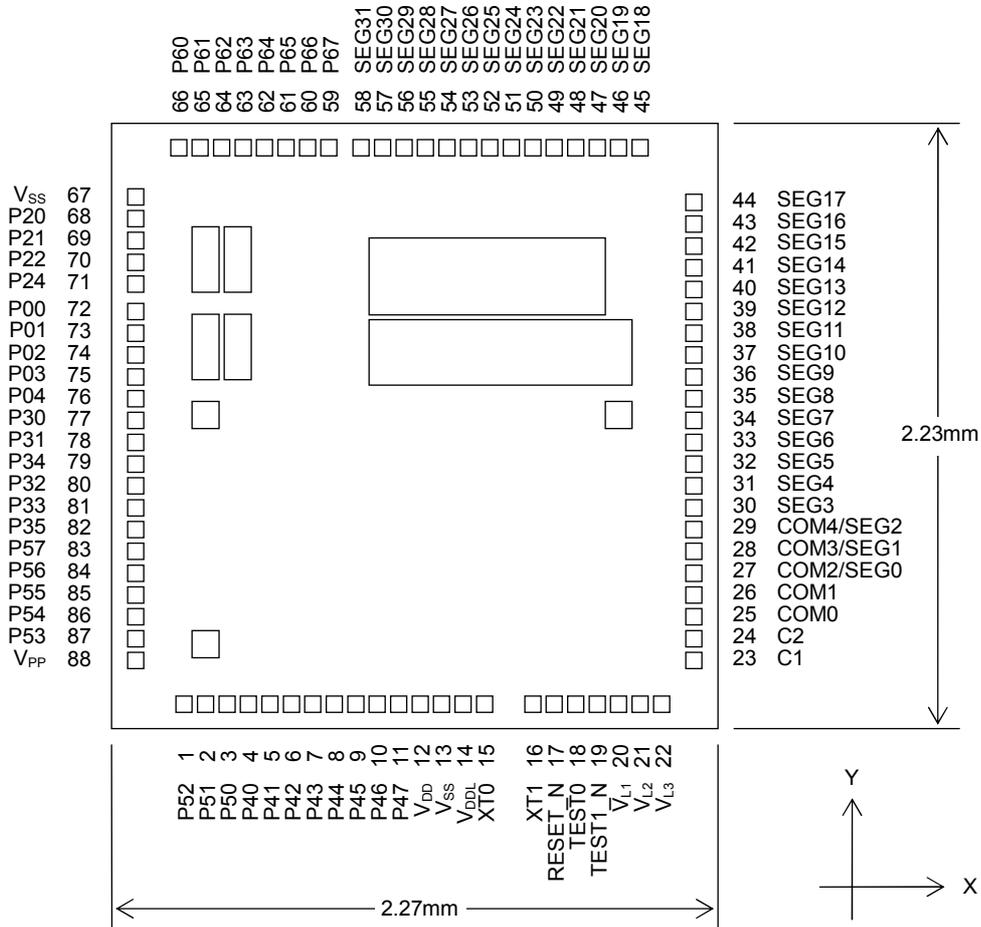
Figure 5 ML610Q407 Chip Layout & Dimension

Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm
PAD count: 88 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

ML610Q408 Chip Pin Layout & Dimension
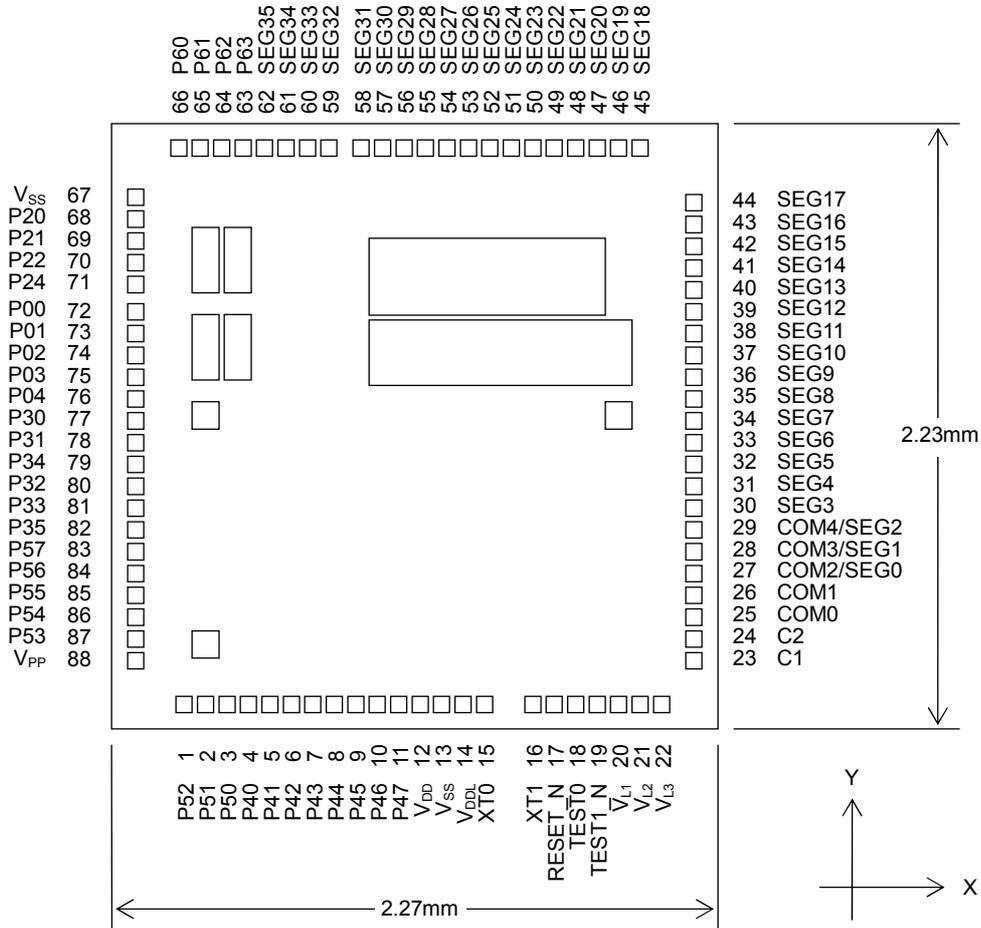
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm
PAD count: 88 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 6 ML610Q408 Chip Layout & Dimension

ML610Q409 Chip Pin Layout & Dimension
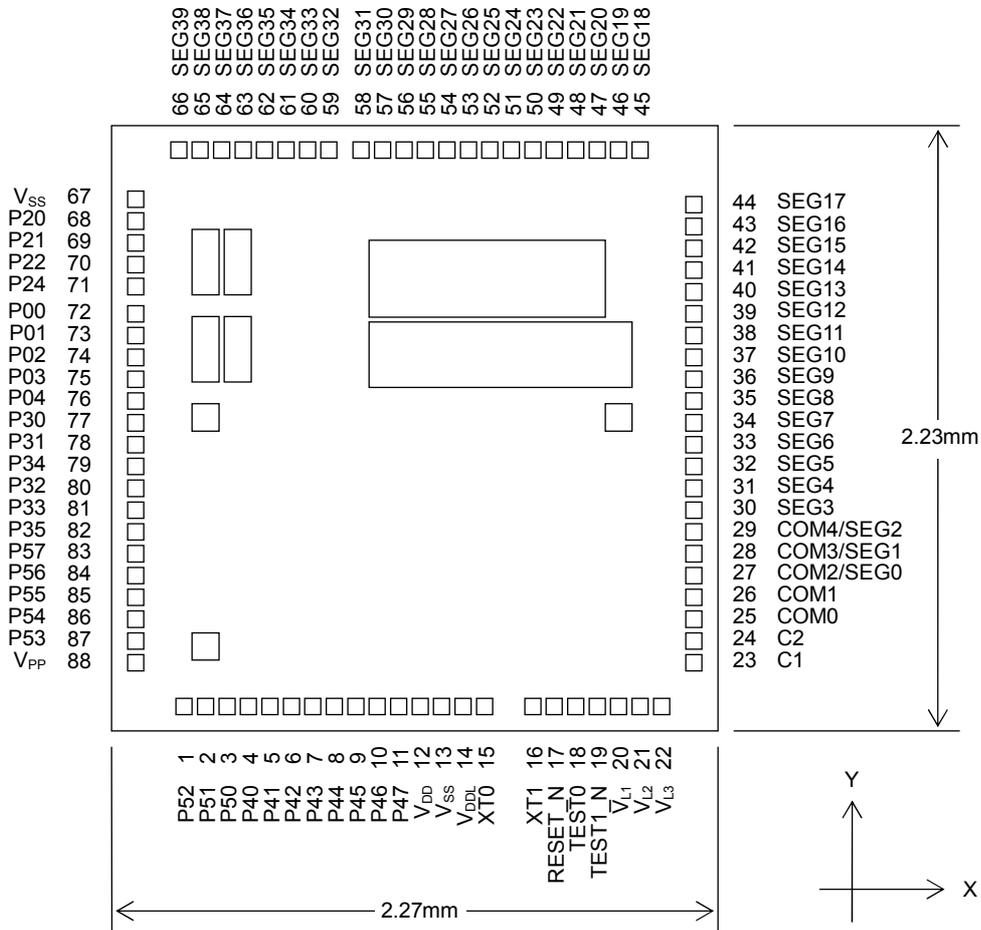
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm
PAD count: 88 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm×70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: V_{SS} level.

Figure 7 ML610Q409 Chip Layout & Dimension

ML610Q407/ML610Q408/ML610Q409 Pad Coordinates

Table 1 ML610Q407/ML610Q408/ML610Q409 Pad Coordinates

Chip Center: X=0,Y=0

| PAD No.	Pad Name	ML610Q407/8/9 X (μm)	ML610Q407/8/9 Y (μm)	PAD No.	Pad Name	ML610Q407/8/9 X (μm)	ML610Q407/8/9 Y (μm)
1	P52	-853	-1009	49	SEG22	535	1009
2	P51	-773	-1009	50	SEG23	455	1009
3	P50	-693	-1009	51	SEG24	375	1009
4	P40	-613	-1009	52	SEG25	295	1009
5	P41	-533	-1009	53	SEG26	215	1009
6	P42	-453	-1009	54	SEG27	135	1009
7	P43	-373	-1009	55	SEG28	55	1009
8	P44	-293	-1009	56	SEG29	-25	1009
9	P45	-213	-1009	57	SEG30	-105	1009
10	P46	-133	-1009	58	SEG31	-185	1009
11	P47	-53	-1009	59	P67 [*1] / SEG32 [*2][*3]	-295	1009
12	VDD	27	-1009	60	P66 [*1] / SEG33 [*2][*3]	-375	1009
13	VSS	107	-1009	61	P65 [*1] / SEG34 [*2][*3]	-455	1009
14	VDDL	187	-1009	62	P64 [*1] / SEG35 [*2][*3]	-535	1009
15	XT0	267	-1009	63	P63 [*1][*2] / SEG36 [*3]	-615	1009
16	XT1	427	-1009	64	P62 [*1][*2] / SEG37 [*3]	-695	1009
17	RESET_N	507	-1009	65	P61 [*1][*2] / SEG38 [*3]	-775	1009
18	TEST0	587	-1009	66	P60 [*1][*2] / SEG39 [*3]	-885	1009
19	TEST1_N	667	-1009	67	VSS	-1029	850
20	VL1	747	-1009	68	P20	-1029	770
21	VL2	827	-1009	69	P21	--1029	690
22	VL3	907	-1009	70	P22	-1029	610
23	C0	1029	-840	71	P24	-1029	530
24	C1	1029	-760	72	P00	-1029	430
25	COM0	1029	-680	73	P01	-1029	350
26	COM1	1029	-600	74	P02	-1029	270
27	COM2/SEG0	1029	-520	75	P03	-1029	190
28	COM3/SEG1	1029	-440	76	P04	-1029	110
29	COM4/SEG2	1029	-360	77	P30	-1029	30
30	SEG3	1029	-280	78	P31	-1029	-50
31	SEG4	1029	-200	79	P34	-1029	-130
32	SEG5	1029	-120	80	P32	-1029	-210
33	SEG6	1029	-40	81	P33	-1029	-290
34	SEG7	1029	40	82	P35	-1029	-370
35	SEG8	1029	120	83	P57	-1029	-450
36	SEG9	1029	200	84	P56	-1029	-530
37	SEG10	1029	280	85	P55	-1029	-610
38	SEG11	1029	360	86	P54	-1029	-690
39	SEG12	1029	440	87	P53	-1029	-770
40	SEG13	1029	520	88	VPP	-1029	-850
41	SEG14	1029	600				
42	SEG15	1029	680				
43	SEG16	1029	760				
44	SEG17	1029	840				
45	SEG18	855	1009				
46	SEG19	775	1009				
47	SEG20	695	1009				
48	SEG21	615	1009				

[*1] ML610Q407 pad name, [*2] ML610Q408 pad name, [*3] ML610Q409 pad name

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
14,77	13,67	Vss	—	Negative power supply pin	—	—	—	—
13	12	V_{DD}	—	Positive power supply pin	—	—	—	—
15	14	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
98	88	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—
22	20	V_{L1}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)[*2]	—	—	—	—
23	21	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)[*2]	—	—	—	—
24	22	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
27	23	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
28	24	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
20	18	TEST0	I/O	Test pin	—	—	—	—
21	19	TEST1_N	I	Test pin	—	—	—	—
19	17	RESET_N	I	Reset input pin	—	—	—	—
17	15	XT0	I	Low-speed clock oscillation pin	—	—	—	—
18	16	XT1	O	Low-speed clock oscillation pin	—	—	—	—
82	72	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—
83	73	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—
84	74	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—
85	75	P03/EXI3	I	Input port, External interrupt	—	—	—	—
86	76	P04/EXI4/ T02P0CK	I	Input port, Timer 0/Timer 2/PWM0 external clock input External interrupt	—	—	—	—
78	68	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
79	69	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
80	70	P22/LED2	O	Output port	Secondary	MD0	O	Melody 0 output
81	71	P24/LED4	O	Output port	Secondary	PWM0	O	PWM0 output
87	77	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
88	78	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
89	79	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
90	80	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
91	81	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 measurement resistor sensor connection pin
92	82	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
5	4	P40	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SIN0	I	SSIO0 data input
6	5	P41	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
7	6	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
					Tertiary	SOUT0	O	SSIO0 data output
8	7	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
					Tertiary	PWM0	O	PWM0 output
9	8	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
					Tertiary	SIN0	I	SSIO0 data input
10	9	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
11	10	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
					Tertiary	SOUT0	O	SSIO0 data output
12	11	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 measurement resistor sensor connection pin
4	3	P50/EXI8	I/O	Input/output port, External interrupt	Secondary	MD0	O	Melody 0 output
					Tertiary	SIN1	I	SSIO1 data input
3	2	P51/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
2	1	P52/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
97	87	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—	—
96	86	P54/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SIN1	I	SSIO1 data input
95	85	P55/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
94	84	P56/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
93	83	P57/EXI8	I/O	Input/output port, External interrupt	—	—	—	—

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
29	25	COM0	O	LCD common pin	—	—	—	—
30	26	COM1	O	LCD common pin	—	—	—	—
31	27	COM2/ SEG0	O	LCD common/segment pin	—	—	—	—
32	28	COM3/ SEG1	O	LCD common/segment pin	—	—	—	—
33	29	COM4/ SEG2	O	LCD common/segment pin	—	—	—	—
34	30	SEG3	O	LCD segment pin	—	—	—	—
35	31	SEG4	O	LCD segment pin	—	—	—	—
36	32	SEG5	O	LCD segment pin	—	—	—	—
37	33	SEG6	O	LCD segment pin	—	—	—	—
38	34	SEG7	O	LCD segment pin	—	—	—	—
39	35	SEG8	O	LCD segment pin	—	—	—	—
40	36	SEG9	O	LCD segment pin	—	—	—	—
41	37	SEG10	O	LCD segment pin	—	—	—	—
42	38	SEG11	O	LCD segment pin	—	—	—	—
43	39	SEG12	O	LCD segment pin	—	—	—	—
44	40	SEG13	O	LCD segment pin	—	—	—	—
45	41	SEG14	O	LCD segment pin	—	—	—	—
46	42	SEG15	O	LCD segment pin	—	—	—	—
47	43	SEG16	O	LCD segment pin	—	—	—	—
48	44	SEG17	O	LCD segment pin	—	—	—	—
52	45	SEG18	O	LCD segment pin	—	—	—	—
53	46	SEG19	O	LCD segment pin	—	—	—	—
54	47	SEG20	O	LCD segment pin	—	—	—	—
55	48	SEG21	O	LCD segment pin	—	—	—	—
56	49	SEG22	O	LCD segment pin	—	—	—	—
57	50	SEG23	O	LCD segment pin	—	—	—	—
58	51	SEG24	O	LCD segment pin	—	—	—	—
59	52	SEG25	O	LCD segment pin	—	—	—	—
60	53	SEG26	O	LCD segment pin	—	—	—	—
61	54	SEG27	O	LCD segment pin	—	—	—	—
62	55	SEG28	O	LCD segment pin	—	—	—	—
63	56	SEG29	O	LCD segment pin	—	—	—	—
64	57	SEG30	O	LCD segment pin	—	—	—	—
65	58	SEG31	O	LCD segment pin	—	—	—	—
66	59	P67[*2]	O	Output port	—	—	—	—
		SEG32[*3]	O	LCD segment pin	—	—	—	—
67	60	P66[*2]	O	Output port	—	—	—	—
		SEG33[*3]	O	LCD segment pin	—	—	—	—
68	61	P65[*2]	O	Output port	—	—	—	—
		SEG34[*3]	O	LCD segment pin	—	—	—	—
69	62	P64[*2]	O	Output port	—	—	—	—
		SEG35[*3]	O	LCD segment pin	—	—	—	—
70	63	P63[*4]	O	Output port	—	—	—	—
		SEG36[*5]	O	LCD segment pin	—	—	—	—
71	64	P62[*4]	O	Output port	—	—	—	—
		SEG37[*5]	O	LCD segment pin	—	—	—	—
72	65	P61[*4]	O	Output port	—	—	—	—
		SEG38[*5]	O	LCD segment pin	—	—	—	—
73	66	P60[*4]	O	Output port	—	—	—	—
		SEG39[*5]	O	LCD segment pin	—	—	—	—

(*1) Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see "Chapter 22   LCD Drivers. In the user's manual"
(*2) Pin for ML610Q407/ML610Q408.
(*3) Pin for ML610Q409.
(*4) Pin for ML610Q407.
(*5) Pin for ML610Q408/ML610Q409.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} .	—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P04	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22,P24	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P57	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	O	General-purpose input/output port. These pins are for the ML610Q407/ ML610Q408, but are not provided in the ML610Q409.	Primary	Positive
P64-P67	O	General-purpose input/output port. These pins are for the ML610Q407, but are not provided in the ML610Q409.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. This pin is used as the secondary function of the P51 or P55 pin.	Secondary	—
SIN1	I	Synchronous serial data input pin. This pin is used as the secondary function of the P50 or P54.	Secondary	Positive
SOUT1	O	Synchronous serial data output pin. This pin is used as the secondary function of the P52 or P56pin.	Secondary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P04 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P57 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/ negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for Timer 0 and Timer 2. The clock for this timer is selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13CK	I	External clock input pin used both Timer 1 and Timer 3. The clock for this timer is selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/Buzzer signal output pin. This pin is used as the secondary function of the P22 pin and P50 pin.	Secondary	Positive/ negative
LED drive				
LED0-2,4	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-4	O	Common output pins.	—	—
SEG0-31	O	Segment output pins.	—	—
SEG32-35	O	Segment output pin. These pins are for the ML610Q408/ML610Q409, but are not provided in the ML610Q407.	—	—
SEG36-39	O	Segment output pin. These pins are for the ML610Q409, but are not provided in the ML610Q407/ML610Q408.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated or positive power supply pin connected). Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see user's manual.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see Appendix C measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2   Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
V_{L1}, V_{L2}, V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
TEST1_N	Open
P00 to P04	V_{DD} or V_{SS}
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P57	Open
P60 to P67	Open
COM0 to 4	Open
SEG0 to 39	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

$(V_{SS} = 0V)$

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta = 25°C	−0.3 to +2.0	V
Power supply voltage 5	V_{L2}	Ta = 25°C	−0.3 to +4.0	V
Power supply voltage 6	V_{L3}	Ta = 25°C	−0.3 to +6.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–6, Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

$(V_{SS} = 0V)$

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	non-P version	−20 to +70	°C
		P version	−40 to +85	
Operating voltage	V_{DD}	f_{OP} = 30k to 625kHz	1.25 to 3.6	V
		f_{OP} = 30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.25 to 3.6V	30k to 625k	Hz
		V_{DD} = 1.8 to 3.6V	30k to 2.5M	
Capacitor externally connected to V_{DDL} pin	C_L	—	0.47±30%	μF
Capacitors externally connected to $V_{L1, 2, 3}$ pins	$C_{a, b, c}$	—	0.1±30%	μF
Capacitors externally connected across C1 and C2 pins	C_{12}	—	0.47±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

$(V_{SS} = 0V)$

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation	—	12	—	pF
		C_L=9pF of crystal oscillation	—	18	—	
		C_L=12pF of crystal oscillation	—	24	—	

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase[*1]	2.75 to 3.6	V
	V_{DDL}	At write/erase[*1]	2.5 to 2.75	
	V_{PP}	At write/erase[*1]	7.7 to 8.3	
erase/program cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

[*1]: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM.
  V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (1/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +70°C, Ta = −40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
500kHz/2MHz RC oscillation frequency	f_{RC}	V_{DD} = 1.25 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			[*3]	Typ. −25%	500	Typ. +25%		
		V_{DD} = 1.80 to 3.6V	Ta = 25°C	Typ. −10%	2.0	Typ. +10%	MHz	
			[*3]	Typ. −25%	2.0	Typ. +25%		
Low-speed crystal oscillation start time[*2]	T_{XTL}	—		—	0.6	2	s	
500kHz/2MHz RC oscillation start time	T_{RC}	—		—	—	0.3	μs	
Low-speed oscillation stop detect time[*1]	T_{STOP}	—		12	16.4	41	ms	
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

[*1]: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.
[*2] : 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used ($C_{GL}=C_{DL}$=6pF).
[*3] : Recommended operating temperature (Ta = −20 to +70°C, Ta = −40 to +85°C for P version)

RESET_N   VIL1   VIL1

P_{RST}

Reset pulse width (P_{RST})

VDD   0.9xV_{DD}

0.1xV_{DD}
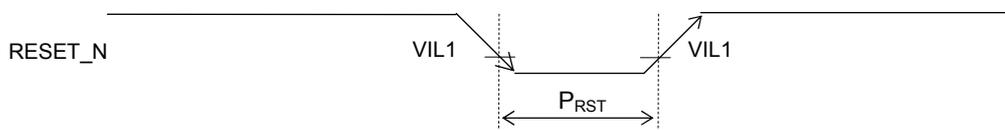
T_{POR}

Power-on reset activation power rise time (T_{POR})

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = -20 to $+70°C$, Ta = -40 to $+85°C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	f_{OP} = 30k to 625kHz	1.1	1.2	1.3		1
		f_{OP} = 30k to 2.5MHz	1.35	1.5	1.65		
V_{DDL} temperature deviation *[1]	ΔV_{DDL}	V_{DD} = 3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *[1]	ΔV_{DDL}	—	—	5	20	mV/V	

*[1]:V_{DDL} can not exceed V_{DD} level. The maximum V_{DDL} becomes V_{DD} level when the V_{DDL} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

DC CHARACTERISTICS (3/5)

$(V_{DD} = 3.0V, V_{SS} = 0V, Ta = -20$ to $+70°C, Ta = -40$ to $+85°C$ for P version)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz/2MHz oscillation: stopped.	Ta= 25°C	—	0.4	0.8	µA	1
			*5	—	—	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating).*3*4 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *6	Ta= 25°C	—	0.9	1.8	µA	
			*5	—	—	9		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	5	8	µA	
			*5	—	—	15		
Supply current 4-1	IDD4-1	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	70	100	µA	
			*5	—	—	120		
Supply current 4-2	IDD4-2	CPU: In RC 2MHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	280	350	µA	
			*5	—	—	400		

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used ($C_{GL}=C_{DL}$=6pF)
*4 : Significant bits of BLKCON0~BLKCON4 registers except DLCD bit on BLKCON4 are all "1".
*5 : Recommended operating temperature (Ta = -20 to $+70°C$, Ta = -40 to $+85°C$ for P version)
*6: LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +70°C, Ta = −40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22,P24/ 2nd function is selected) (P30–P36) (P40–P47) (P50–P57) [1][2] (P60-P63) [1] (P64-P67)	VOH1	IOH1 = −0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} −0.5	—	—	V	2
		IOH1 = -0.03mA, V_{DD} = 1.25 to 3.6V	V_{DD} −0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P22,P24/ 2nd function is Not selected)	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0–4) (SEG0–31) [1] (SEG0–35) [2] (SEG0–39) [3]	VOH3	IOH4 = −0.05mA, VL1=1.2V	V_{L3} −0.2	—	—		
	VOML3	IOMH4 = +0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOM4S = −0.05mA, VL1=1.2V	V_{L2} −0.2	—	—		
	VOLM3	IOML4 = +0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOML4S = −0.05mA, VL1=1.2V	V_{L1} −0.2	—	—		
	VOL3	IOL4 = +0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20–P22, P24) (P30–P35) (P40–P47) (P50–P57) [1][2] (P60-P63) [1] (P64-P67)	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	−1	—	—		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1 = V_{DD}	0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH1 = V_{DD}	2	300	600		
	IIL2	VIL1 = V_{ss}	-1	—	—		
Input current 3 (P00-P04) (P30-P35) (P40-P47) (P50-P57)	IIH3	VIH3 = V_{DD} ,V_{DD} = 1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3 = V_{DD} ,V_{DD} = 1.25 to 3.6V (when pulled-down)					
	IIL3	VIL3 = V_{SS} , V_{DD} = 1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3 = V_{SS} , V_{DD} = 1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)	−1	—	—		

[1]: pins for ML610Q407
[2]: pins for ML610Q408
[3]: pins for ML610Q409

DC CHARACTERISTICS (5/5))

$(V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, Ta = -20 to $+70°C$, Ta = -40 to $+85°C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0, TEST1_N) (P00–P04) (P30–P35) (P40–P47) (P50–P57)	VIH1	—	$0.7 \times V_{DD}$	—	V_{DD}	V	5
	VIL1	$V_{DD} = 1.8$ to $3.6V$	0	—	$0.3 \times V_{DD}$		
		$V_{DD} = 1.25$ to $3.6V$	0	—	$0.2 \times V_{DD}$		
Input pin capacitance (P00–P04) (P30–P35) (P40–P47) (P50–P57)	CIN	f = 10kHz $V_{rms} = 50mV$ Ta = $25°C$	—	—	5	pF	—