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FEUL610Q428-03

ML610Q428/ML610Q429
User's Manual

Issue Date: Apr. 22, 2015

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q428/ML610Q429.

The following manuals are also available. Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual
Description about the connection between uEASE and ML610Qxxx.

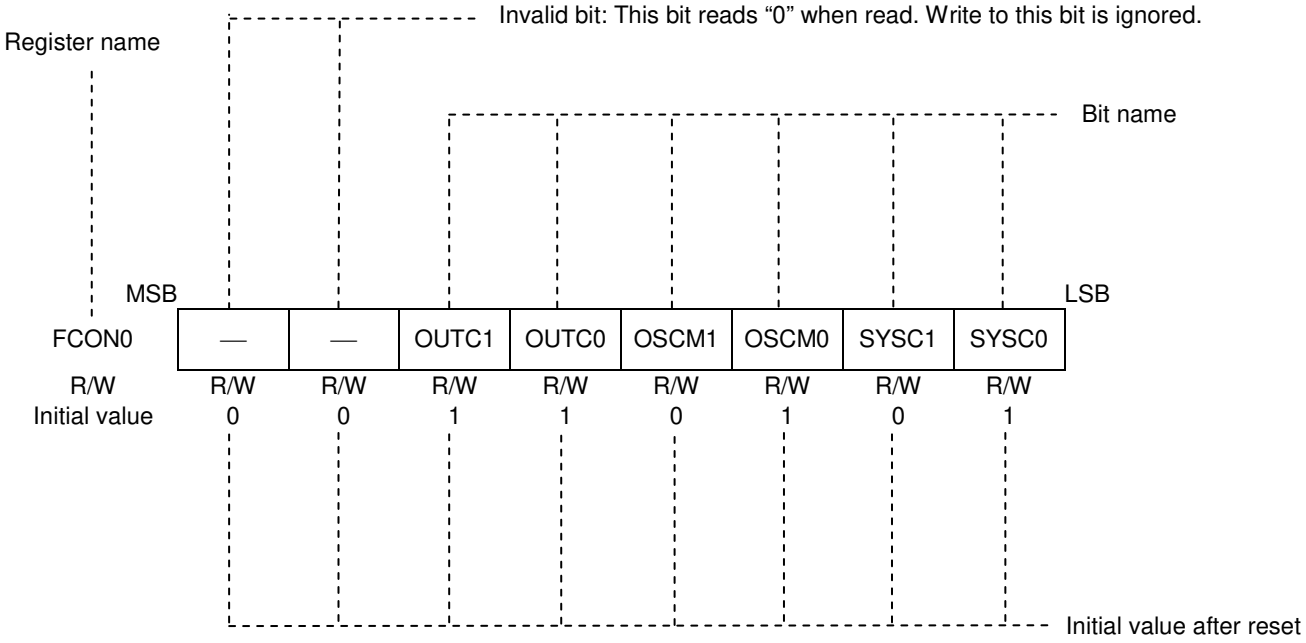
■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1. Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel procesing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.24 4μs (@4.096 MHz system clock)

- Internal memory
  - Internal 48KByte Flash ROM (24K×16 bits) (including unusable 1KByte TEST area)
  - Internal 3KByte Data RAM (3072×8 bits), 1KByte Display Allocation RAM (1024 x 8bit)
  - Internal 192-byte RAM for display

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 27 maskable interrupt sources (Internal sources: 19, External sources: 8)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 2 channels (16-bit configuration available)

- 1 kHz timer
  - 10 Hz/1 Hz interrupt function

- PWM
  - Resolution 16 bits × 3 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 10 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q428: 14 channels (including secondary functions)
    ML610Q429: 20 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610Q428: 1392 dots max. (58 seg × 24 com), 1/1 to 1/24 duty
    ML610Q429: 512 dots max. (64 seg × 8 com) , 1/1 to 1/8 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 32Hz, 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (2M/500kHz)
    Built-in PLL oscillation (8.192 MHz ±TBD%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C
  - Operating voltage: V_{DD} = 1.1V to 3.6V

• Product name – Supported Function

The line-up of the ML610Q428 and the ML610Q429 is below.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q428-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q429-xxxWA	Flash ROM	-20°C to +70°C	Yes

-128-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q428-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q429-xxxTB	Flash ROM	-20°C to +70°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)
Q:Flash ROM version
WA: Chip
TB: TQFP

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML610Q428

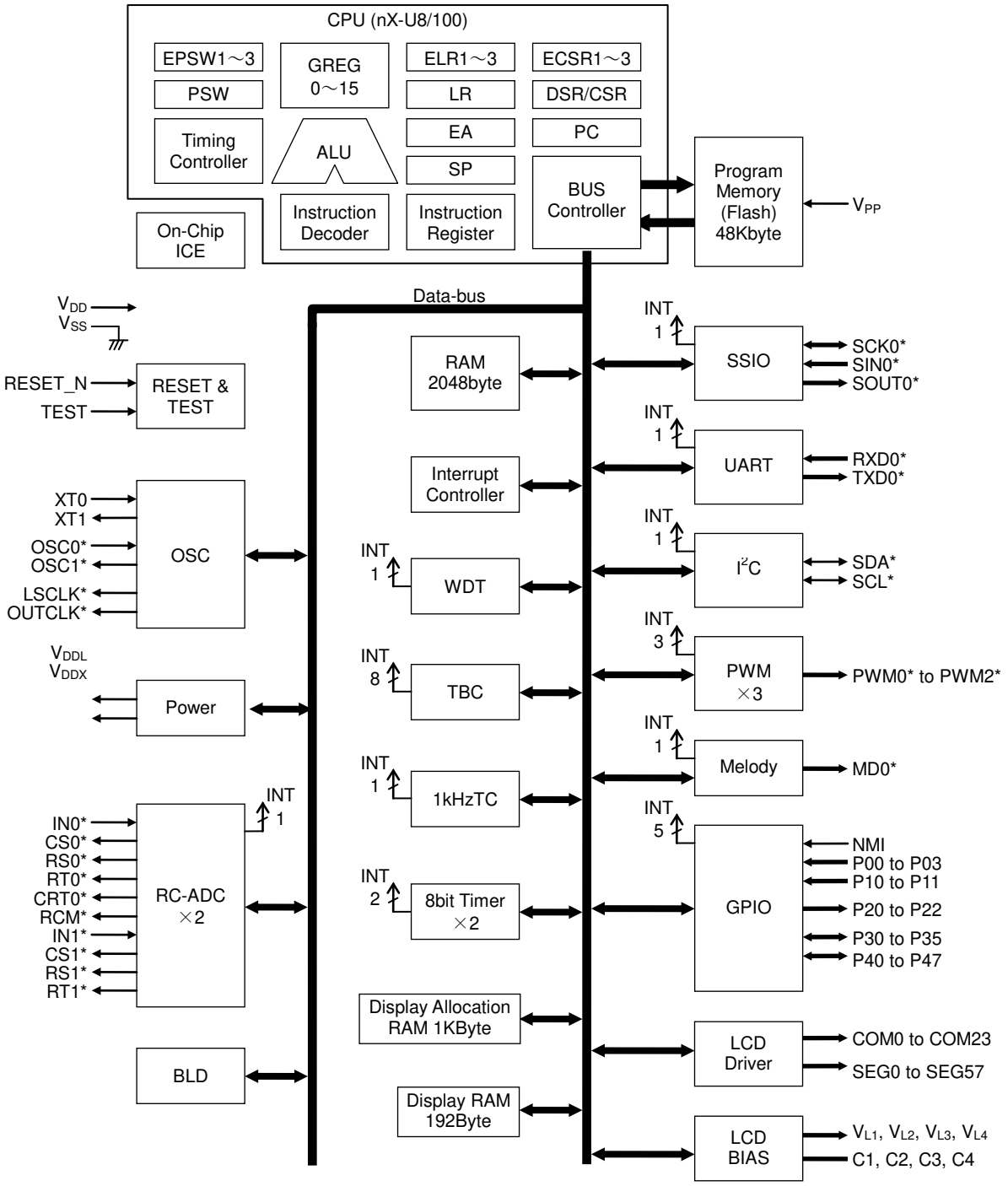


Figure 1-1 Block Diagram of ML610Q428

1.2.2 Block Diagram of ML610Q429

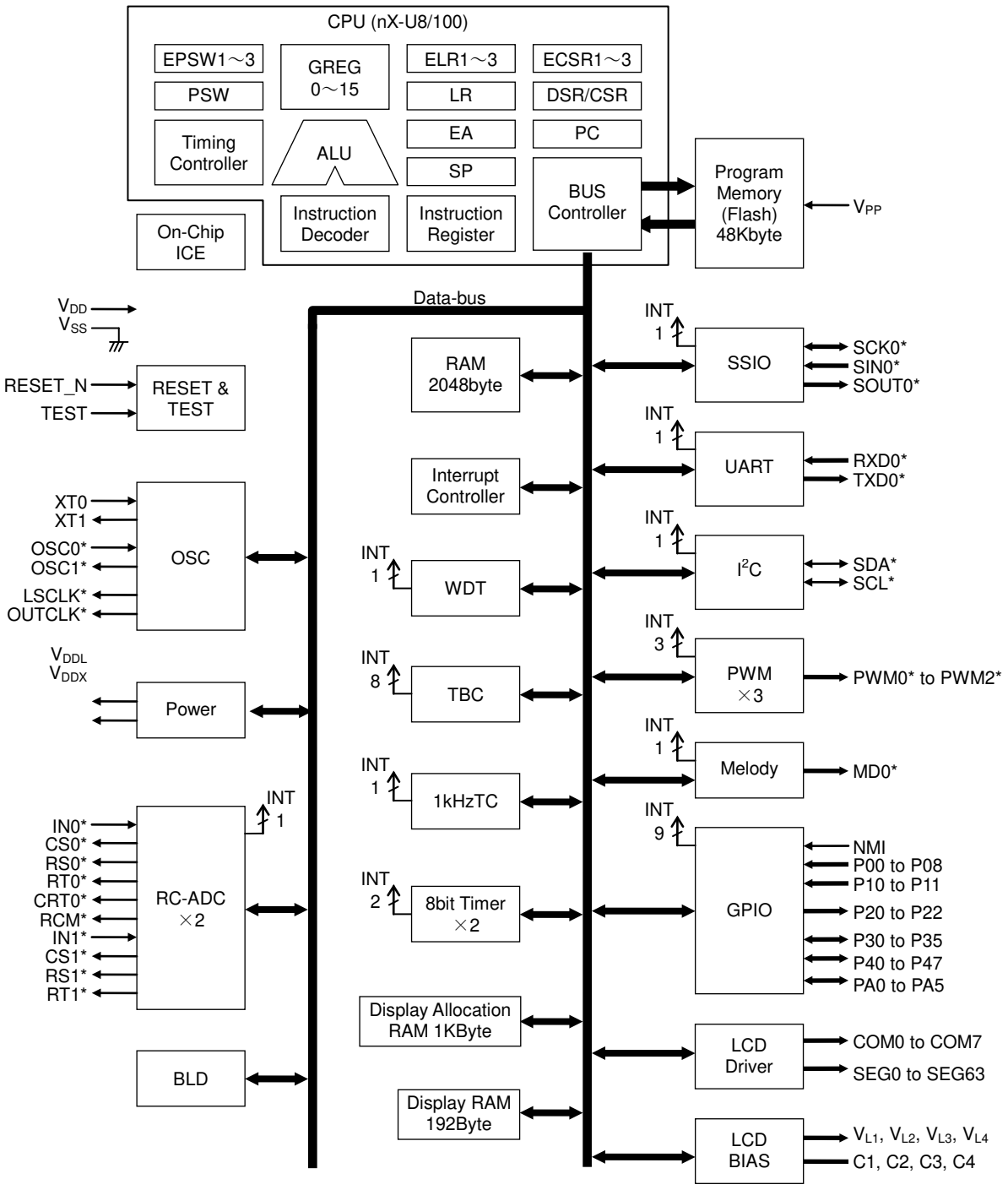
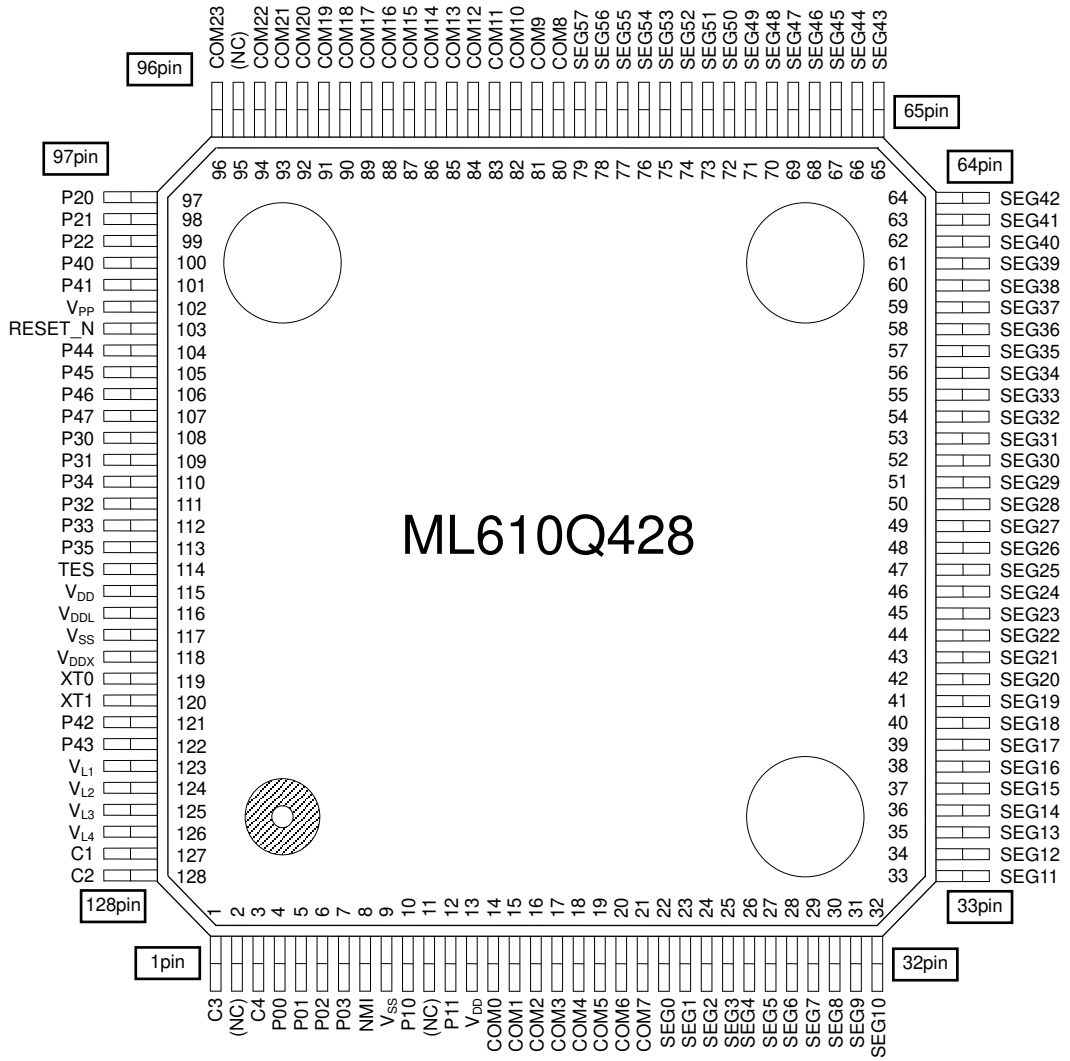


Figure 1-2 Block Diagram of ML610Q429

1.3 Pins

1.3.1 Pin Layout

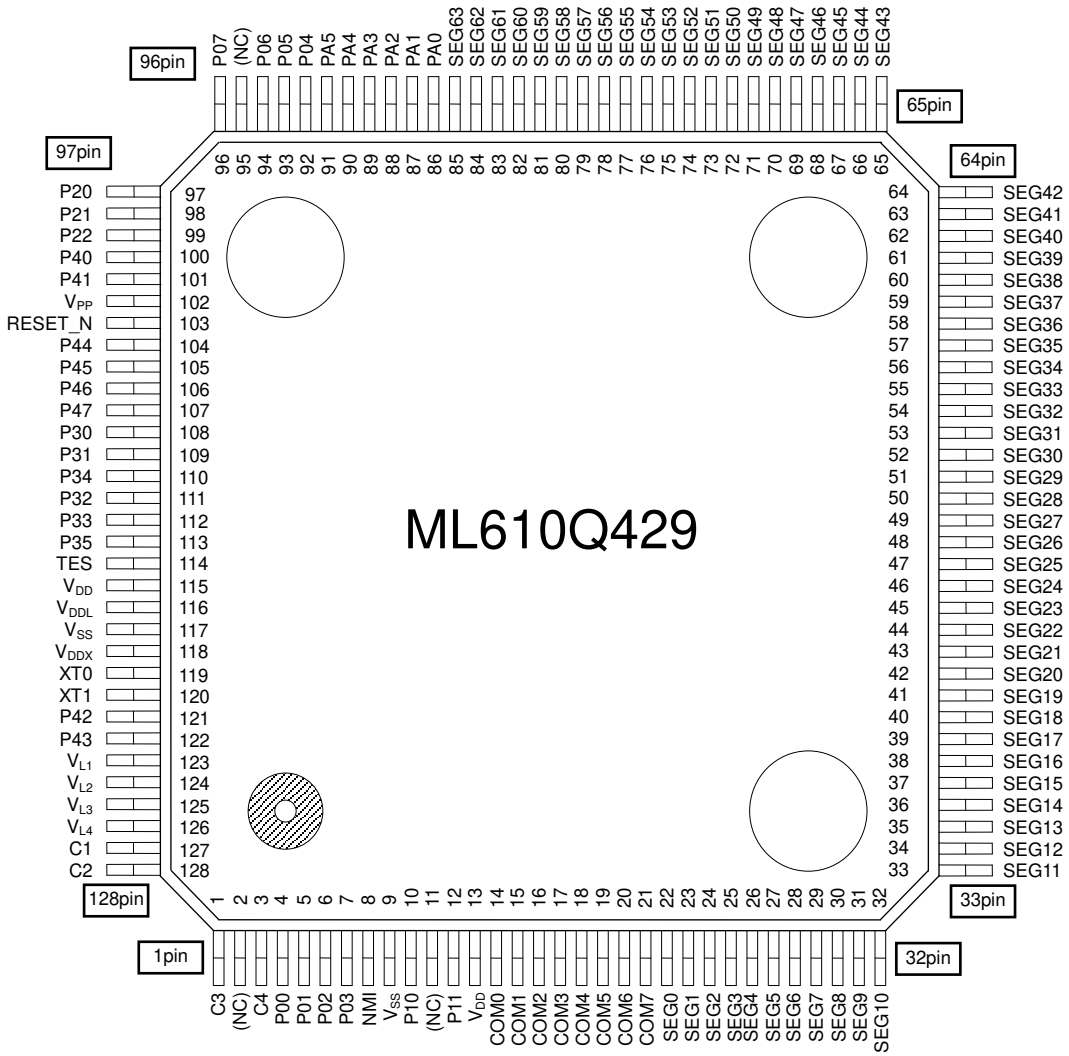
1.3.1.1 Pin Layout of ML610Q428 TQFP Package



(NC): No Connection

Figure 1-3 Pin Layout of ML610Q428 Package

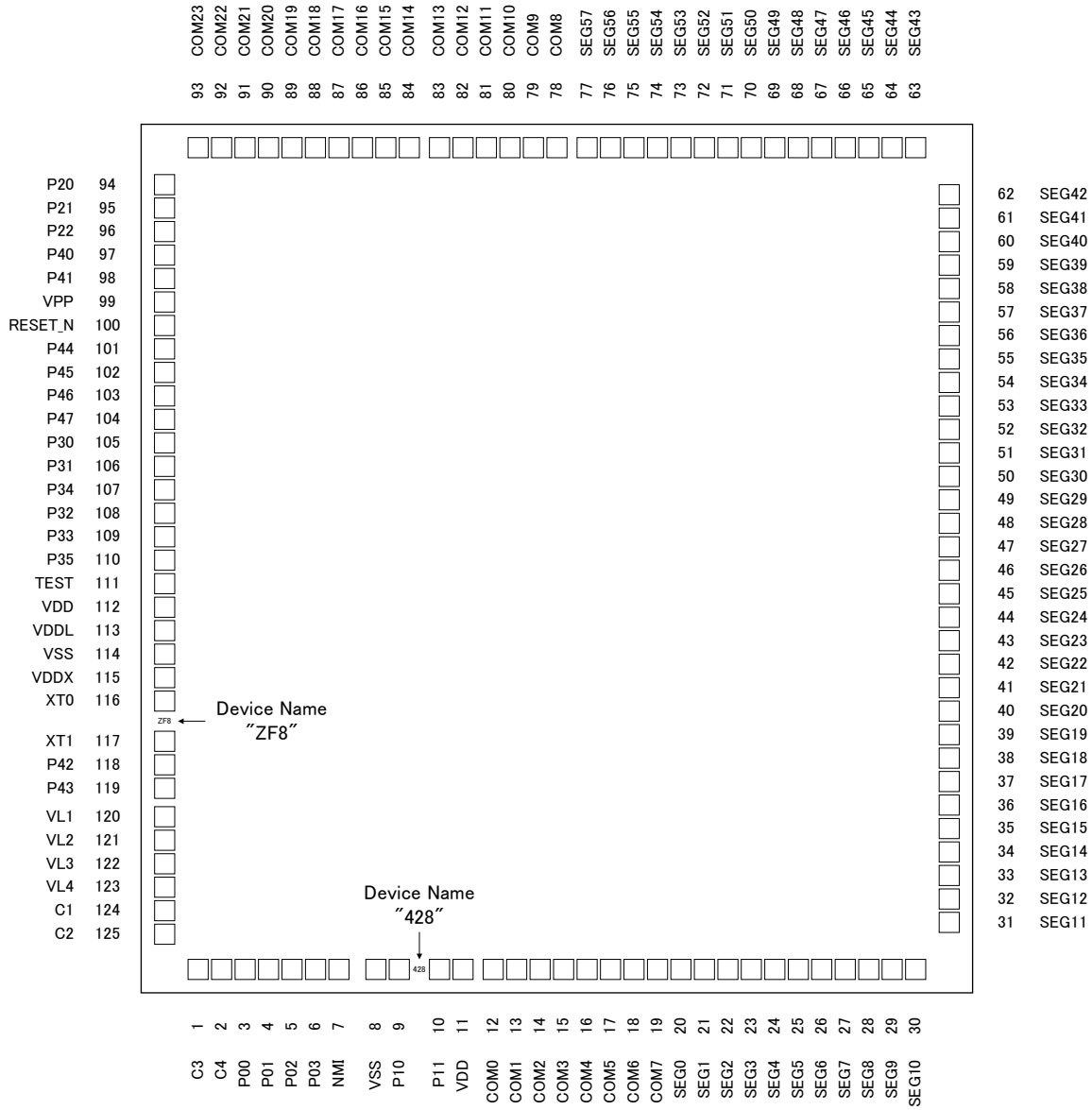
1.3.1.2 Pin Layout of ML610Q429 TQFP Package



(NC): No Connection

Figure 1-4 Pin Layout of ML610Q429 Package

1.3.1.3 Pin Layout of ML610Q428 Chip

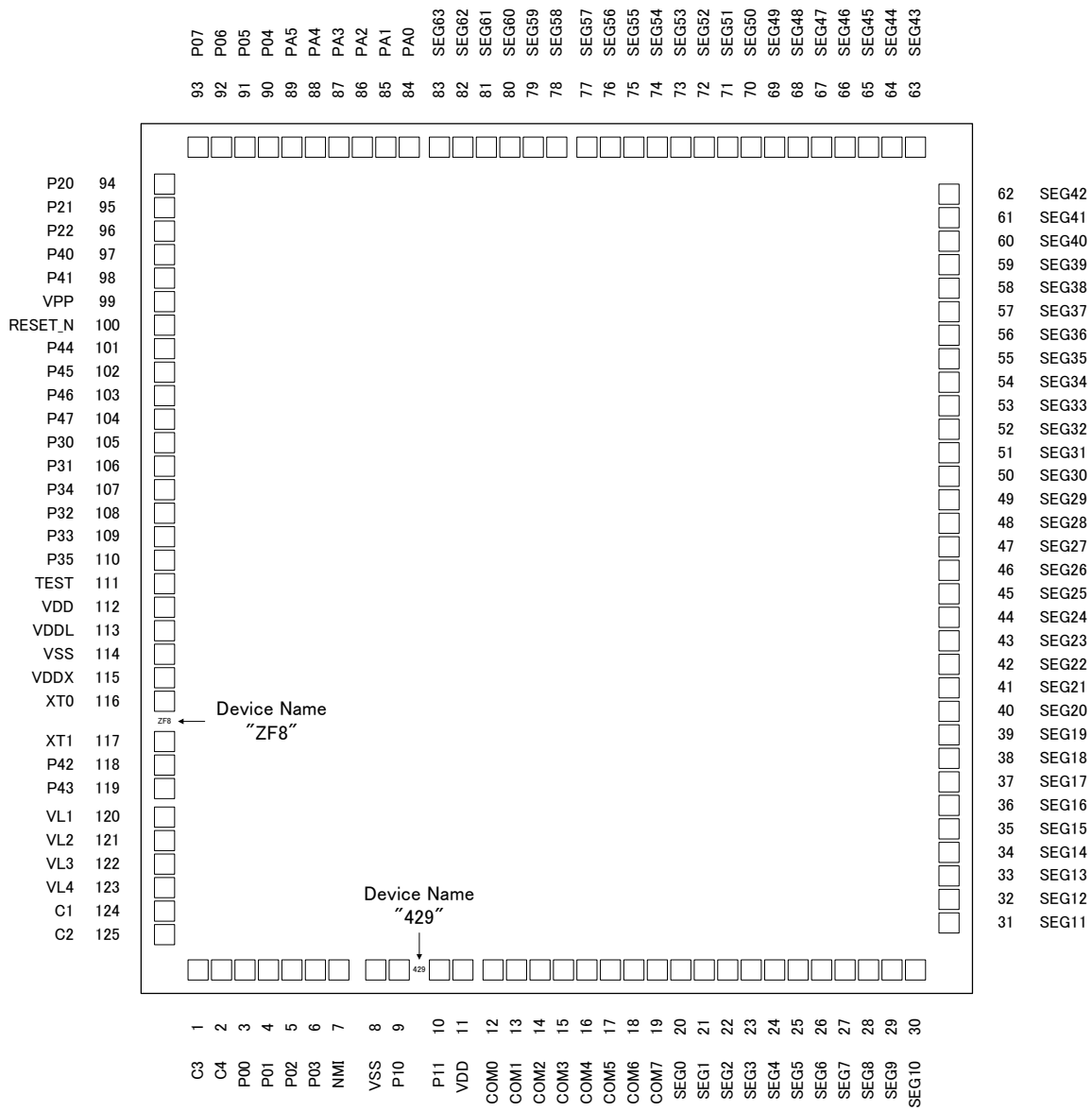


Chip size:	2.99 mm × 3.11 mm
PAD count:	125 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-5 Dimensions of ML610Q428 Chip

Note:
Figure 1-5 is an image figure of the order of PAD, and it differs from an actual image. Refer to the PAD coordinate for detailed arrangement.
A chip angle can be checked by the distinguishing mark of three figures.

1.3.1.4 Pin Layout of ML610Q429 Chip



Chip size:	2.99 mm × 3.11 mm
PAD count:	125 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-6 Dimensions of ML610Q429 Chip

Note:
Figure 1-6 is an image figure of the order of PAD, and it differs from an actual image. Refer to the PAD coordinate for detailed arrangement.
A chip angle can be checked by the distinguishing mark of three figures.

1.3.1.5 Pad Coordinates of ML610Q428 Chip

Table 1-1 Pad Coordinates of ML610Q428

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)
1	C3	-1225	-1449
2	C4	-1145	-1449
3	P00	-1055	-1449
4	P01	-975	-1449
5	P02	-895	-1449
6	P03	-815	-1449
7	NMI	-735	-1449
8	VSS	-605	-1449
9	P10	-525	-1449
10	P11	-365	-1449
11	VDD	-285	-1449
12	COM0	-185	-1449
13	COM1	-105	-1449
14	COM2	-25	-1449
15	COM3	55	-1449
16	COM4	135	-1449
17	COM5	215	-1449
18	COM6	295	-1449
19	COM7	375	-1449
20	SEG0	455	-1449
21	SEG1	535	-1449
22	SEG2	615	-1449
23	SEG3	695	-1449
24	SEG4	775	-1449
25	SEG5	855	-1449
26	SEG6	935	-1449
27	SEG7	1015	-1449
28	SEG8	1095	-1449
29	SEG9	1175	-1449
30	SEG10	1255	-1449
31	SEG11	1389	-1240
32	SEG12	1389	-1160
33	SEG13	1389	-1080
34	SEG14	1389	-1000
35	SEG15	1389	-920
36	SEG16	1389	-840
37	SEG17	1389	-760
38	SEG18	1389	-680
39	SEG19	1389	-600
40	SEG20	1389	-520
41	SEG21	1389	-440
42	SEG22	1389	-360
43	SEG23	1389	-280
44	SEG24	1389	-200
45	SEG25	1389	-120
46	SEG26	1389	-40
47	SEG27	1389	40
48	SEG28	1389	120
49	SEG29	1389	200
50	SEG30	1389	280
51	SEG31	1389	360
52	SEG32	1389	440
53	SEG33	1389	520
54	SEG34	1389	600
55	SEG35	1389	680
56	SEG36	1389	760
57	SEG37	1389	840
58	SEG38	1389	920
59	SEG39	1389	1000
60	SEG40	1389	1080
61	SEG41	1389	1160
62	SEG42	1389	1240
63	SEG43	1255	1449
64	SEG44	1175	1449
65	SEG45	1095	1449
66	SEG46	1015	1449
67	SEG47	935	1449
68	SEG48	855	1449
69	SEG49	775	1449
70	SEG50	695	1449
71	SEG51	615	1449
72	SEG52	535	1449
73	SEG53	455	1449
74	SEG54	375	1449
75	SEG55	295	1449
76	SEG56	215	1449
77	SEG57	135	1449
78	COM8	35	1449
79	COM9	-45	1449
80	COM10	-125	1449
81	COM11	-205	1449
82	COM12	-285	1449
83	COM13	-365	1449
84	COM14	-465	1449
85	COM15	-545	1449
86	COM16	-625	1449
87	COM17	-705	1449
88	COM18	-785	1449
89	COM19	-865	1449
90	COM20	-945	1449
91	COM21	-1025	1449
92	COM22	-1105	1449
93	COM23	-1185	1449
94	P20	-1389	1270
95	P21	-1389	1190
96	P22	-1389	1110
97	P40	-1389	1030
98	P41	-1389	950
99	VPP	-1389	870
100	RESET_N	-1389	790
101	P44	-1389	710
102	P45	-1389	630
103	P46	-1389	550
104	P47	-1389	470
105	P30	-1389	390
106	P31	-1389	310
107	P34	-1389	230
108	P32	-1389	150
109	P33	-1389	70
110	P35	-1389	-10
111	TEST	-1389	-90
112	VDD	-1389	-170
113	VDDL	-1389	-250
114	VSS	-1389	-330
115	VDDX	-1389	-410
116	XT0	-1389	-490
117	XT1	-1389	-650
118	P42	-1389	-730
119	P43	-1389	-810
120	VL1	-1389	-905
121	VL2	-1389	-985
122	VL3	-1389	-1065
123	VL4	-1389	-1145
124	C1	-1389	-1225
125	C2	-1389	-1305