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# ML610Q435/ML610Q436

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8-bit Microcontroller with a Built-in LCD driver

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## GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as real-time clock, synchronous serial port, UART, I<sup>2</sup>C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, 12-bit successive approximation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100. The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications. The on-chip debug function that is installed enables program debugging and programming.

## FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    - 30.5 μs (@32.768 kHz system clock)
    - 0.24 4μs (@4.096 MHz system clock)
- Internal memory
  - Internal 96KByte Flash ROM (48K×16 bits) (including unusable 1KByte TEST area)
  - Internal 2KByte Data RAM (2048×8 bits), 1KByte Display Allocation RAM (1024 x 8bit)
  - Internal 192Byte RAM for display
- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 23 maskable interrupt sources (Internal sources: 19, External sources: 4)
- Time base counter
  - Low-speed time base counter ×1 channel
    - Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel
- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
  - 8 bits × 4 channels (16-bit configuration available)
- 1 kHz timer
  - 10 Hz/1 Hz interrupt function

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
  - Resolution 16 bits × 1 channel
- Real time clock
  - Year, month, day, day of the week, hour, minute, and second registers
  - Automatic leap year correction
  - Regular interrupts (0.5 sec, 1 sec, 1 minute, 1 hour)
  - Alarm interrupt × 2 channels (day of the week, hour, minute; month, day hour, minute)
- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator
- I<sup>2</sup>C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)
- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels
- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 2 channels
- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    - ML610Q435: 22 channels (including secondary functions)
    - ML610Q436: 14 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.  
ML610Q435: 1024 dots max. (64 seg × 16 com)  
ML610Q436: 1536 dots max. (64 seg × 24 com)
  - 1/1 to 1/24 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)
- Reset
  - Reset through the RESET\_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected  
(“A” version(ML610Q435A/Q436A) don’t have the oscillation stop function.)
  - Reset by the watchdog timer (WDT) overflow
- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)
- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)  
Crystal oscillation (32.768 kHz)
  - High-speed clock:  
Built-in RC oscillation (500 kHz)  
Built-in PLL oscillation (8.192 MHz ±TBD%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:  
Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock
- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Shipment
  - Chip  
ML610Q435-xxxWA (Blank product: ML610Q435-NNNWA)  
ML610Q436-xxxWA (Blank product: ML610Q436-NNNWA)  
ML610Q435A-xxxWA (Blank product: ML610Q435A-NNNWA)  
ML610Q436A-xxxWA (Blank product: ML610Q436A-NNNWA)
  - 144-pin plastic LQFP  
ML610Q435-xxxTCZ03A (Blank product: ML610Q435-NNNTCZ03A)  
ML610Q436-xxxTCZ03A (Blank product: ML610Q436-NNNTCZ03A)  
ML610Q435A-xxxTCZ03A (Blank product: ML610Q435A-NNNTCZ03A)  
ML610Q436A-xxxTCZ03A (Blank product: ML610Q436A-NNNTCZ03A)  
xxx: ROM code number
- Guaranteed operating range
  - Operating temperature: -20°C to 70°C
  - Operating voltage:  $V_{DD} = 1.1V$  to 3.6V,  $AV_{DD} = 2.2V$  to 3.6V

**BLOCK DIAGRAM**  
ML610Q435 Block Diagram

Figure 1 show the block diagram of the ML610Q435.  
"\*" indicates the secondary function of each port.

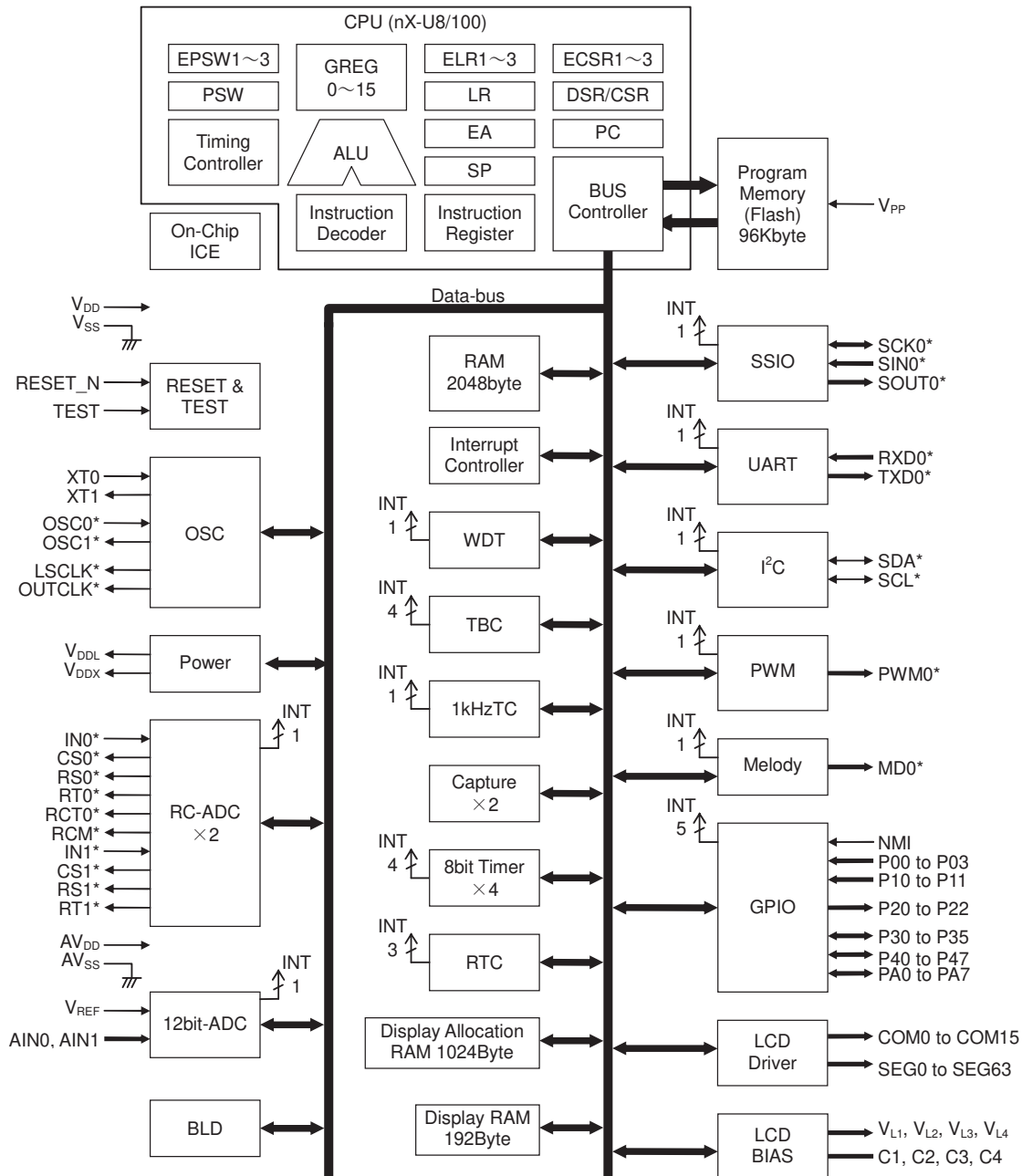
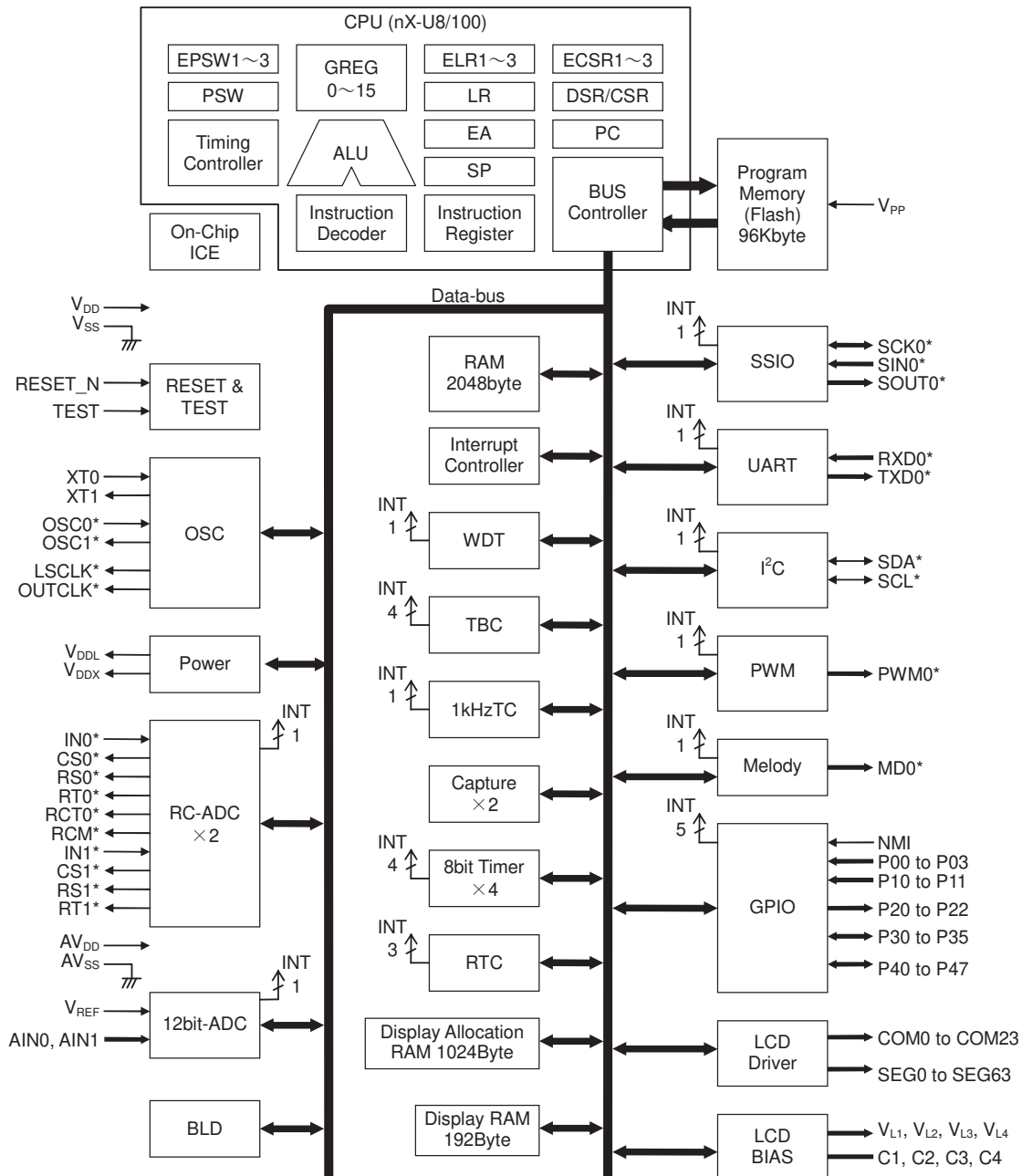


Figure 1 ML610Q435 Block Diagram

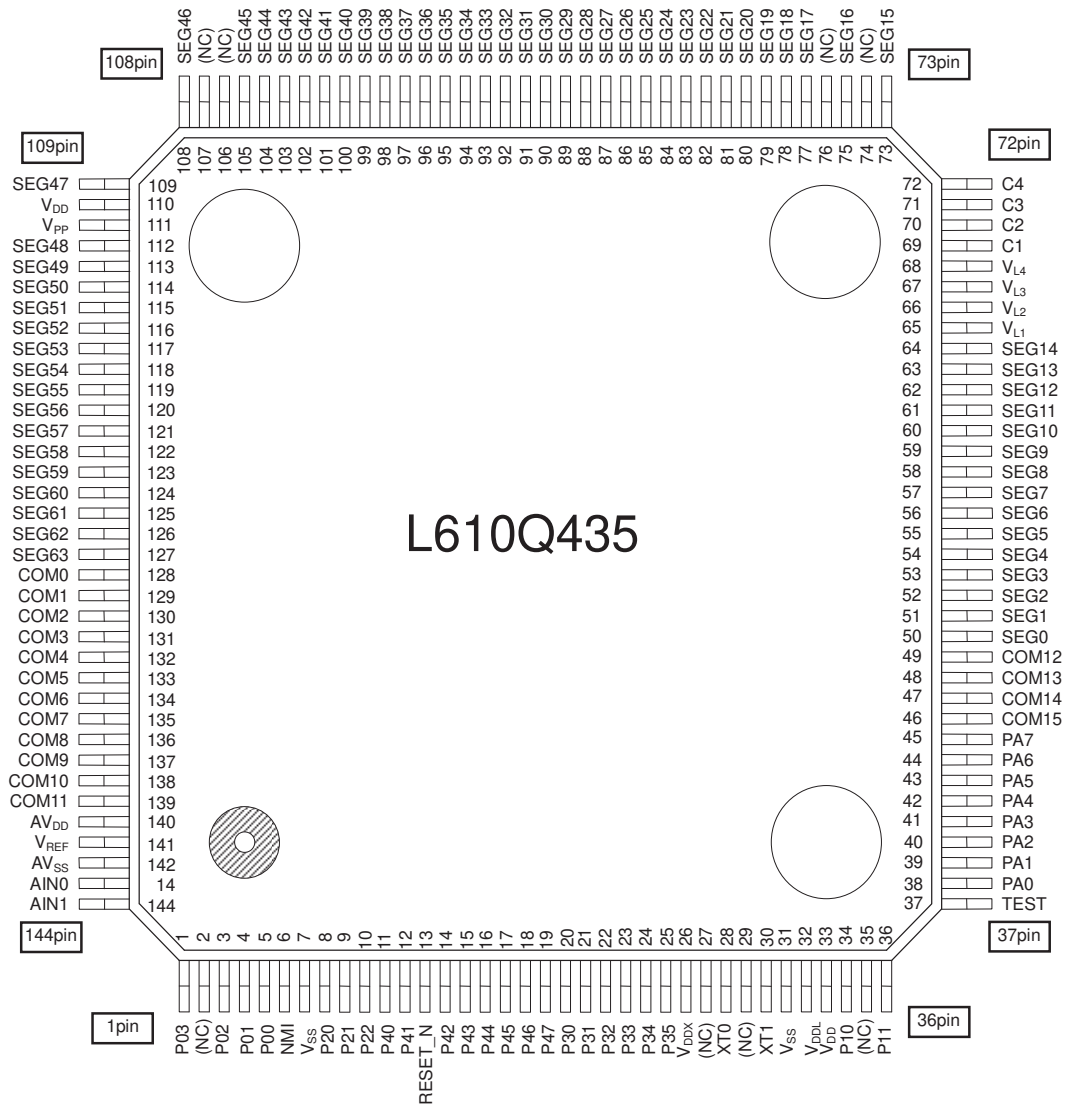
**ML610Q436 Block Diagram**

Figure 2 show the block diagram of the ML610Q436.  
 "\*" indicates the secondary function of each port.



**Figure 2 ML610Q436 Block Diagram**

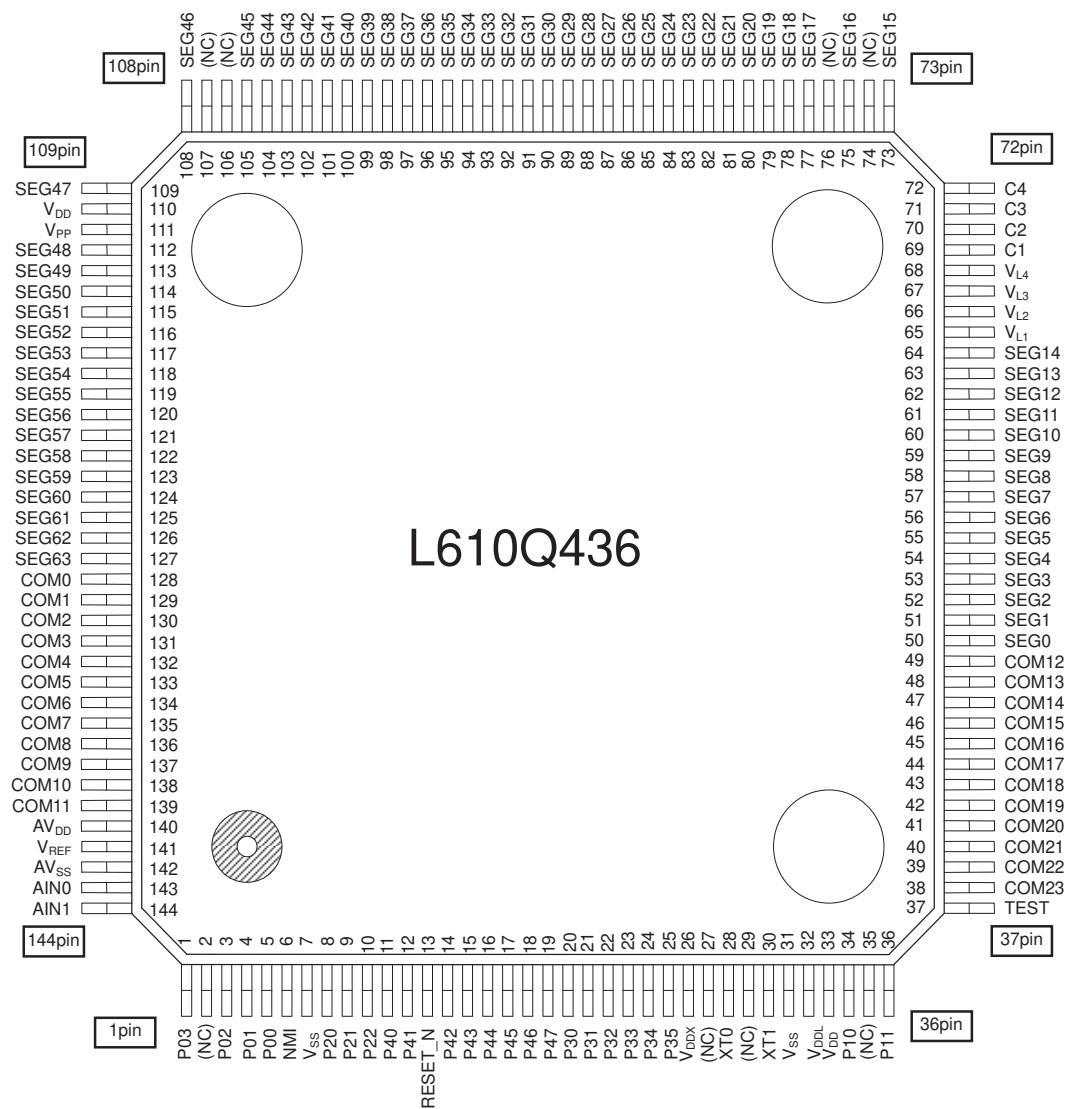
**PIN CONFIGURATION**  
**ML610Q435 LQFP144 Pin Layout**



(NC): No Connection

**Figure 3 ML610Q435 LQFP144 Pin Configuration**

ML610Q436 LQFP144 Pin Layout

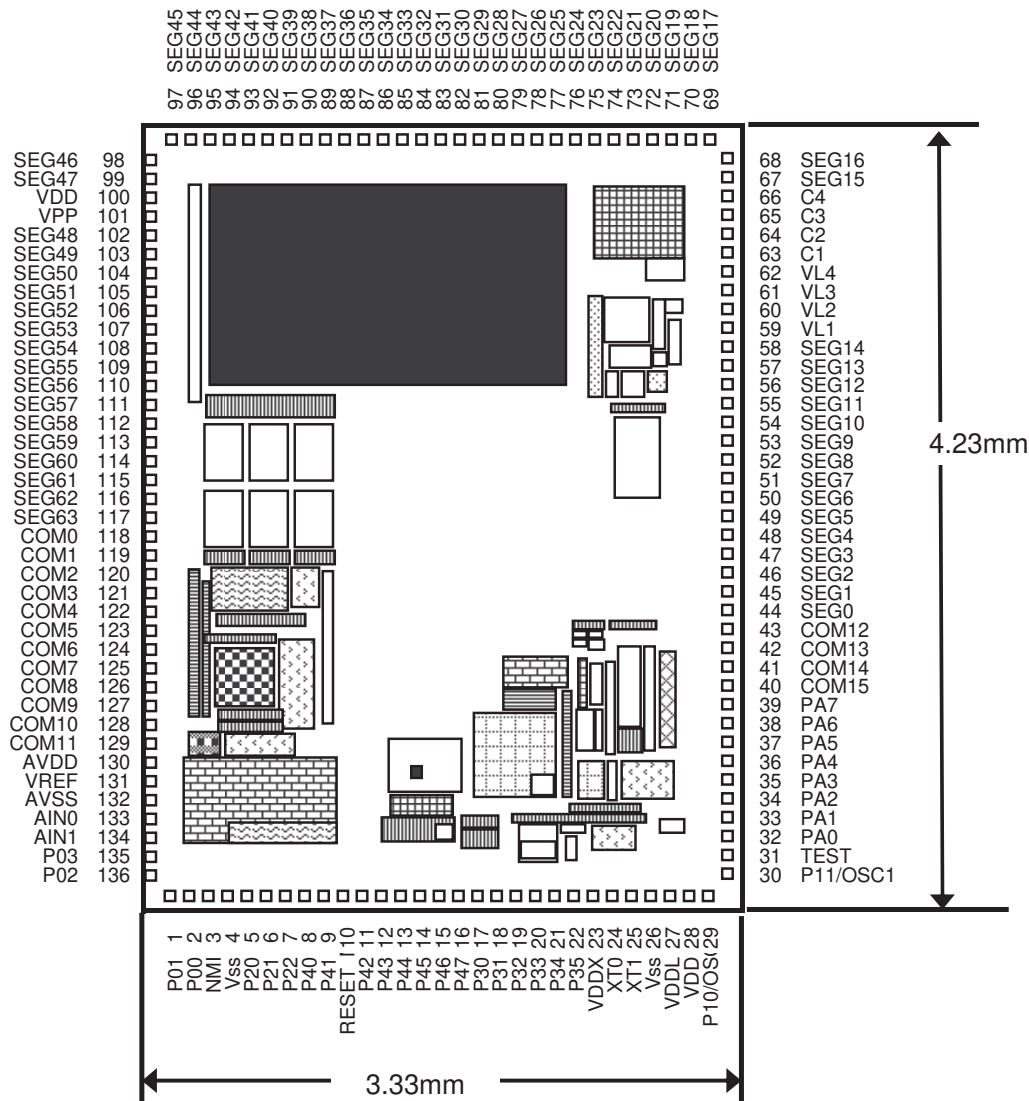


(NC): No Connection

Figure 4 ML610Q436 LQFP144 Pin Configuration



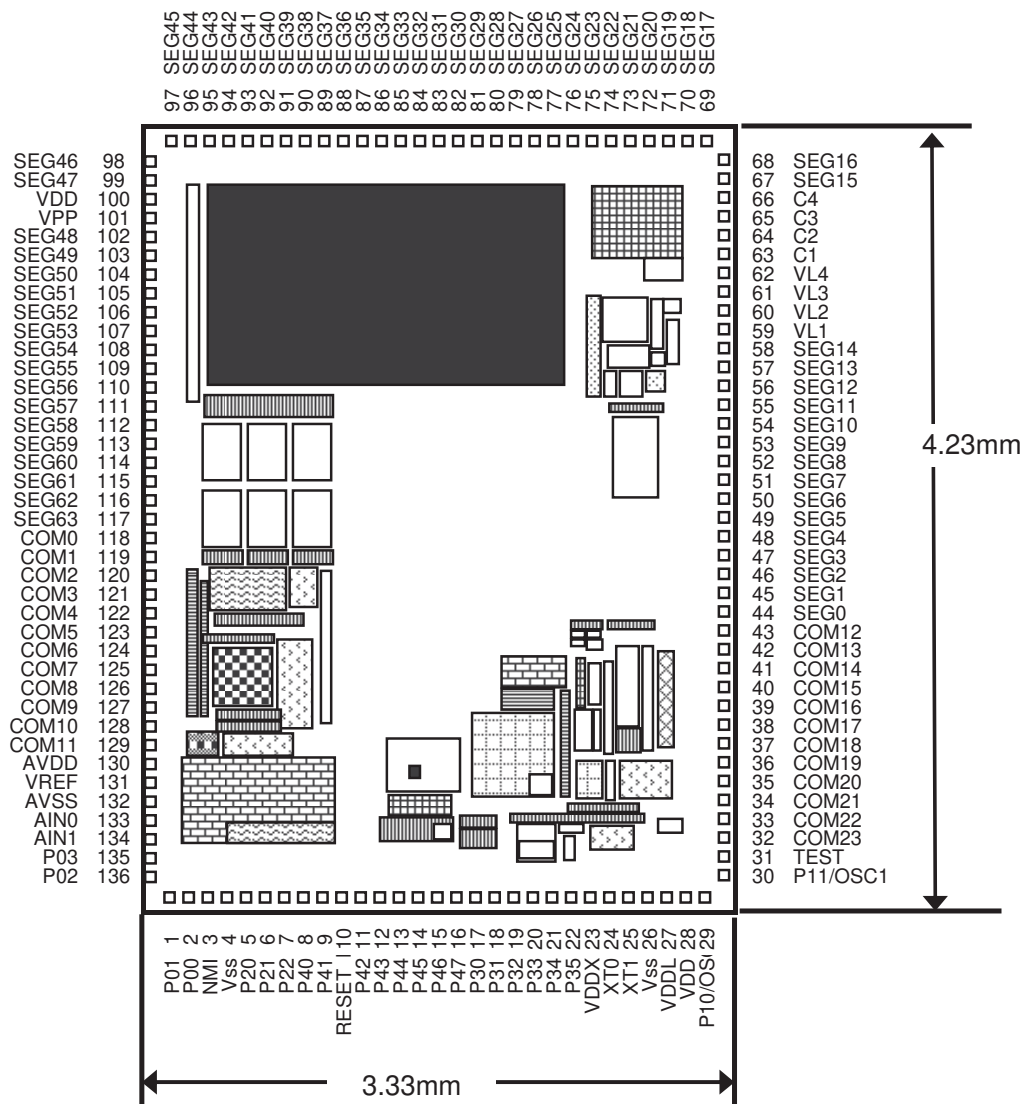
ML610Q435 Chip Pin Layout & Dimension



Chip size:	3.33 mm × 4.23 mm
PAD count:	136 pins
Minimum PAD pitch:	100 μm
PAD aperture:	80 μm × 80 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V <sub>SS</sub> level

Figure 5 ML610Q435 Chip Layout & Dimension

ML610Q436 Chip Pin Layout & Dimension



Chip size: 3.33 mm × 4.23 mm  
 PAD count: 136 pins  
 Minimum PAD pitch: 100 μm  
 PAD aperture: 80 μm × 80 μm  
 Chip thickness: 350 μm  
 Voltage of the rear side of chip: V<sub>SS</sub> level

Figure 6 ML610Q436 Chip Layout & Dimension

## ML610Q435 Pad Coordinates

Table 1 ML610Q435 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	P01	-1400	-1978	51	SEG7	1528	200	101	V <sub>PP</sub>	-1528	1600
2	P00	-1300	-1978	52	SEG8	1528	300	102	SEG48	-1528	1500
3	NMI	-1200	-1978	53	SEG9	1528	400	103	SEG49	-1528	1400
4	V <sub>SS</sub>	-1100	-1978	54	SEG10	1528	500	104	SEG50	-1528	1300
5	P20	-1000	-1978	55	SEG11	1528	600	105	SEG51	-1528	1200
6	P21	-900	-1978	56	SEG12	1528	700	106	SEG52	-1528	1100
7	P22	-800	-1978	57	SEG13	1528	800	107	SEG53	-1528	1000
8	P40	-700	-1978	58	SEG14	1528	900	108	SEG54	-1528	900
9	P41	-600	-1978	59	V <sub>L1</sub>	1528	1000	109	SEG55	-1528	800
10	RESET_N	-500	-1978	60	V <sub>L2</sub>	1528	1100	110	SEG56	-1528	700
11	P42	-400	-1978	61	V <sub>L3</sub>	1528	1200	111	SEG57	-1528	600
12	P43	-300	-1978	62	V <sub>L4</sub>	1528	1300	112	SEG58	-1528	500
13	P44	-200	-1978	63	C1	1528	1400	113	SEG59	-1528	400
14	P45	-100	-1978	64	C2	1528	1500	114	SEG60	-1528	300
15	P46	0	-1978	65	C3	1528	1600	115	SEG61	-1528	200
16	P47	100	-1978	66	C4	1528	1700	116	SEG62	-1528	100
17	P30	200	-1978	67	SEG15	1528	1800	117	SEG63	-1528	0
18	P31	300	-1978	68	SEG16	1528	1900	118	COM0	-1528	-100
19	P32	400	-1978	69	SEG17	1400	1978	119	COM1	-1528	-200
20	P33	500	-1978	70	SEG18	1300	1978	120	COM2	-1528	-300
21	P34	600	-1978	71	SEG19	1200	1978	121	COM3	-1528	-400
22	P35	700	-1978	72	SEG20	1100	1978	122	COM4	-1528	-500
23	V <sub>DDX</sub>	800	-1978	73	SEG21	1000	1978	123	COM5	-1528	-600
24	XT0	900	-1978	74	SEG22	900	1978	124	COM6	-1528	-700
25	XT1	1000	-1978	75	SEG23	800	1978	125	COM7	-1528	-800
26	V <sub>SS</sub>	1100	-1978	76	SEG24	700	1978	126	COM8	-1528	-900
27	V <sub>DDL</sub>	1200	-1978	77	SEG25	600	1978	127	COM9	-1528	-1000
28	V <sub>DD</sub>	1300	-1978	78	SEG26	500	1978	128	COM10	-1528	-1100
29	P10	1400	-1978	79	SEG27	400	1978	129	COM11	-1528	-1200
30	P11	1528	-1900	80	SEG28	300	1978	130	A <sub>VDD</sub>	-1528	-1300
31	TEST	1528	-1800	81	SEG29	200	1978	131	V <sub>REF</sub>	-1528	-1400
32	PA0	1528	-1700	82	SEG30	100	1978	132	A <sub>VSS</sub>	-1528	-1500
33	PA1	1528	-1600	83	SEG31	0	1978	133	AIN0	-1528	-1600
34	PA2	1528	-1500	84	SEG32	-100	1978	134	AIN1	-1528	-1700
35	PA3	1528	-1400	85	SEG33	-200	1978	135	P03	-1528	-1800
36	PA4	1528	-1300	86	SEG34	-300	1978	136	P02	-1528	-1900
37	PA5	1528	-1200	87	SEG35	-400	1978				
38	PA6	1528	-1100	88	SEG36	-500	1978				
39	PA7	1528	-1000	89	SEG37	-600	1978				
40	COM15	1528	-900	90	SEG38	-700	1978				
41	COM14	1528	-800	91	SEG39	-800	1978				
42	COM13	1528	-700	92	SEG40	-900	1978				
43	COM12	1528	-600	93	SEG41	-1000	1978				
44	SEG0	1528	-500	94	SEG42	-1100	1978				
45	SEG1	1528	-400	95	SEG43	-1200	1978				
46	SEG2	1528	-300	96	SEG44	-1300	1978				
47	SEG3	1528	-200	97	SEG45	-1400	1978				
48	SEG4	1528	-100	98	SEG46	-1528	1900				
49	SEG5	1528	0	99	SEG47	-1528	1800				
50	SEG6	1528	100	100	V <sub>DD</sub>	-1528	1700				

## ML610Q436 Pad Coordinates

Table 2 ML610Q436 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	P01	-1400	-1978	51	SEG7	1528	200	101	V <sub>PP</sub>	-1528	1600
2	P00	-1300	-1978	52	SEG8	1528	300	102	SEG48	-1528	1500
3	NMI	-1200	-1978	53	SEG9	1528	400	103	SEG49	-1528	1400
4	V <sub>SS</sub>	-1100	-1978	54	SEG10	1528	500	104	SEG50	-1528	1300
5	P20	-1000	-1978	55	SEG11	1528	600	105	SEG51	-1528	1200
6	P21	-900	-1978	56	SEG12	1528	700	106	SEG52	-1528	1100
7	P22	-800	-1978	57	SEG13	1528	800	107	SEG53	-1528	1000
8	P40	-700	-1978	58	SEG14	1528	900	108	SEG54	-1528	900
9	P41	-600	-1978	59	V <sub>L1</sub>	1528	1000	109	SEG55	-1528	800
10	RESET_N	-500	-1978	60	V <sub>L2</sub>	1528	1100	110	SEG56	-1528	700
11	P42	-400	-1978	61	V <sub>L3</sub>	1528	1200	111	SEG57	-1528	600
12	P43	-300	-1978	62	V <sub>L4</sub>	1528	1300	112	SEG58	-1528	500
13	P44	-200	-1978	63	C1	1528	1400	113	SEG59	-1528	400
14	P45	-100	-1978	64	C2	1528	1500	114	SEG60	-1528	300
15	P46	0	-1978	65	C3	1528	1600	115	SEG61	-1528	200
16	P47	100	-1978	66	C4	1528	1700	116	SEG62	-1528	100
17	P30	200	-1978	67	SEG15	1528	1800	117	SEG63	-1528	0
18	P31	300	-1978	68	SEG16	1528	1900	118	COM0	-1528	-100
19	P32	400	-1978	69	SEG17	1400	1978	119	COM1	-1528	-200
20	P33	500	-1978	70	SEG18	1300	1978	120	COM2	-1528	-300
21	P34	600	-1978	71	SEG19	1200	1978	121	COM3	-1528	-400
22	P35	700	-1978	72	SEG20	1100	1978	122	COM4	-1528	-500
23	V <sub>DDX</sub>	800	-1978	73	SEG21	1000	1978	123	COM5	-1528	-600
24	XT0	900	-1978	74	SEG22	900	1978	124	COM6	-1528	-700
25	XT1	1000	-1978	75	SEG23	800	1978	125	COM7	-1528	-800
26	V <sub>SS</sub>	1100	-1978	76	SEG24	700	1978	126	COM8	-1528	-900
27	V <sub>DDL</sub>	1200	-1978	77	SEG25	600	1978	127	COM9	-1528	-1000
28	V <sub>DD</sub>	1300	-1978	78	SEG26	500	1978	128	COM10	-1528	-1100
29	P10	1400	-1978	79	SEG27	400	1978	129	COM11	-1528	-1200
30	P11	1528	-1900	80	SEG28	300	1978	130	A <sub>VDD</sub>	-1528	-1300
31	TEST	1528	-1800	81	SEG29	200	1978	131	V <sub>REF</sub>	-1528	-1400
32	COM23	1528	-1700	82	SEG30	100	1978	132	A <sub>VSS</sub>	-1528	-1500
33	COM22	1528	-1600	83	SEG31	0	1978	133	AIN0	-1528	-1600
34	COM21	1528	-1500	84	SEG32	-100	1978	134	AIN1	-1528	-1700
35	COM20	1528	-1400	85	SEG33	-200	1978	135	P03	-1528	-1800
36	COM19	1528	-1300	86	SEG34	-300	1978	136	P02	-1528	-1900
37	COM18	1528	-1200	87	SEG35	-400	1978				
38	COM17	1528	-1100	88	SEG36	-500	1978				
39	COM16	1528	-1000	89	SEG37	-600	1978				
40	COM15	1528	-900	90	SEG38	-700	1978				
41	COM14	1528	-800	91	SEG39	-800	1978				
42	COM13	1528	-700	92	SEG40	-900	1978				
43	COM12	1528	-600	93	SEG41	-1000	1978				
44	SEG0	1528	-500	94	SEG42	-1100	1978				
45	SEG1	1528	-400	95	SEG43	-1200	1978				
46	SEG2	1528	-300	96	SEG44	-1300	1978				
47	SEG3	1528	-200	97	SEG45	-1400	1978				
48	SEG4	1528	-100	98	SEG46	-1528	1900				
49	SEG5	1528	0	99	SEG47	-1528	1800				
50	SEG6	1528	100	100	V <sub>DD</sub>	-1528	1700				

## PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
4,26	4,26	V <sub>SS</sub>	—	Negative power supply pin	—	—	—	—	—	—
28, 100	28, 100	V <sub>DD</sub>	—	Positive power supply pin	—	—	—	—	—	—
27	27	V <sub>DDL</sub>	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
23	23	V <sub>DDX</sub>	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
101	101	V <sub>PP</sub>	—	Power supply pin for Flash ROM	—	—	—	—	—	—
132	132	AV <sub>SS</sub>	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
130	130	AV <sub>DD</sub>	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
59	59	V <sub>L1</sub>	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
60	60	V <sub>L2</sub>	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
61	61	V <sub>L3</sub>	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
62	62	V <sub>L4</sub>	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
63	63	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
64	64	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
65	65	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
66	66	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
31	31	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
10	10	RESET <sub>N</sub>	I	Reset input pin	—	—	—	—	—	—
24	24	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
25	25	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
131	131	V <sub>REF</sub>	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
133	133	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
134	134	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
3	3	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
2	2	P00/EXI0/CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
1	1	P01/EXI1/CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
136	136	P02/EXI2/RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
135	135	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
29	29	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
30	30	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
5	5	P20/LE D0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
6	6	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
7	7	P22/LE D2	O	Output port	MD0	O	Melody output	—	—	—
17	17	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
18	18	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
19	19	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
20	20	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
21	21	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
22	22	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
8	8	P40	I/O	Input/output port	SDA	I/O	I <sup>2</sup> C data input/output	SIN0	I	SSIO data input
9	9	P41	I/O	Input/output port	SCL	I/O	I <sup>2</sup> C clock input/output	SCK0	I/O	SSIO synchronous clock
11	11	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
12	12	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
13	13	P44/T02 P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
14	14	P45/T13 P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
15	15	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
16	16	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
—	32	PA0	I/O	Input/output port	—	—	—	—	—	—
—	33	PA1	I/O	Input/output port	—	—	—	—	—	—
—	34	PA2	I/O	Input/output port	—	—	—	—	—	—
—	35	PA3	I/O	Input/output port	—	—	—	—	—	—
—	36	PA4	I/O	Input/output port	—	—	—	—	—	—
—	37	PA5	I/O	Input/output port	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
—	38	PA6	I/O	Input/output port	—	—	—	—	—	—
—	39	PA7	I/O	Input/output port	—	—	—	—	—	—
118	118	COM0	O	LCD common pin	—	—	—	—	—	—
119	119	COM1	O	LCD common pin	—	—	—	—	—	—
120	120	COM2	O	LCD common pin	—	—	—	—	—	—
121	121	COM3	O	LCD common pin	—	—	—	—	—	—
122	122	COM4	O	LCD common pin	—	—	—	—	—	—
123	123	COM5	O	LCD common pin	—	—	—	—	—	—
124	124	COM6	O	LCD common pin	—	—	—	—	—	—
125	125	COM7	O	LCD common pin	—	—	—	—	—	—
126	126	COM8	O	LCD common pin	—	—	—	—	—	—
127	127	COM9	O	LCD common pin	—	—	—	—	—	—
128	128	COM10	O	LCD common pin	—	—	—	—	—	—
129	129	COM11	O	LCD common pin	—	—	—	—	—	—
43	43	COM12	O	LCD common pin	—	—	—	—	—	—
42	42	COM13	O	LCD common pin	—	—	—	—	—	—
41	41	COM14	O	LCD common pin	—	—	—	—	—	—
40	40	COM15	O	LCD common pin	—	—	—	—	—	—
39	—	COM16	O	LCD common pin	—	—	—	—	—	—
38	—	COM17	O	LCD common pin	—	—	—	—	—	—
37	—	COM18	O	LCD common pin	—	—	—	—	—	—
36	—	COM19	O	LCD common pin	—	—	—	—	—	—
35	—	COM20	O	LCD common pin	—	—	—	—	—	—
34	—	COM21	O	LCD common pin	—	—	—	—	—	—
33	—	COM22	O	LCD common pin	—	—	—	—	—	—
32	—	COM23	O	LCD common pin	—	—	—	—	—	—
44	44	SEG0	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG1	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG2	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG3	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG4	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG5	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG6	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG7	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG8	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG9	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG10	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG11	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG12	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG13	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG14	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG15	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG16	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG17	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG18	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG19	O	LCD segment pin	—	—	—	—	—	—
72	72	SEG20	O	LCD segment pin	—	—	—	—	—	—
73	73	SEG21	O	LCD segment pin	—	—	—	—	—	—
74	74	SEG22	O	LCD segment pin	—	—	—	—	—	—
75	75	SEG23	O	LCD segment pin	—	—	—	—	—	—
76	76	SEG24	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG25	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG26	O	LCD segment pin	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
79	79	SEG27	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG28	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG29	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG30	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG31	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG32	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG33	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG34	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG35	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG36	O	LCD segment pin	—	—	—	—	—	—
89	89	SEG37	O	LCD segment pin	—	—	—	—	—	—
90	90	SEG38	O	LCD segment pin	—	—	—	—	—	—
91	91	SEG39	O	LCD segment pin	—	—	—	—	—	—
92	92	SEG40	O	LCD segment pin	—	—	—	—	—	—
93	93	SEG41	O	LCD segment pin	—	—	—	—	—	—
94	94	SEG42	O	LCD segment pin	—	—	—	—	—	—
95	95	SEG43	O	LCD segment pin	—	—	—	—	—	—
96	96	SEG44	O	LCD segment pin	—	—	—	—	—	—
97	97	SEG45	O	LCD segment pin	—	—	—	—	—	—
98	98	SEG46	O	LCD segment pin	—	—	—	—	—	—
99	99	SEG47	O	LCD segment pin	—	—	—	—	—	—
102	102	SEG48	O	LCD segment pin	—	—	—	—	—	—
103	103	SEG49	O	LCD segment pin	—	—	—	—	—	—
104	104	SEG50	O	LCD segment pin	—	—	—	—	—	—
105	105	SEG51	O	LCD segment pin	—	—	—	—	—	—
106	106	SEG52	O	LCD segment pin	—	—	—	—	—	—
107	107	SEG53	O	LCD segment pin	—	—	—	—	—	—
108	108	SEG54	O	LCD segment pin	—	—	—	—	—	—
109	109	SEG55	O	LCD segment pin	—	—	—	—	—	—
110	110	SEG56	O	LCD segment pin	—	—	—	—	—	—
111	111	SEG57	O	LCD segment pin	—	—	—	—	—	—
112	112	SEG58	O	LCD segment pin	—	—	—	—	—	—
113	113	SEG59	O	LCD segment pin	—	—	—	—	—	—
114	114	SEG60	O	LCD segment pin	—	—	—	—	—	—
115	115	SEG61	O	LCD segment pin	—	—	—	—	—	—
116	116	SEG62	O	LCD segment pin	—	—	—	—	—	—
117	117	SEG63	O	LCD segment pin	—	—	—	—	—	—



**PIN DESCRIPTION**

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>System</b>				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V <sub>SS</sub> as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V <sub>SS</sub> . This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
<b>General-purpose input port</b>				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
<b>General-purpose output port</b>				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
<b>General-purpose input/output port</b>				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q435, but are not provided in the ML610Q436.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>UART</b>				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
<b>I<sup>2</sup>C bus interface</b>				
SDA	I/O	I <sup>2</sup> C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I <sup>2</sup> C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I <sup>2</sup> C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I <sup>2</sup> C, externally connect a pull-up resistor.	Secondary	Positive
<b>Synchronous serial (SSIO)</b>				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
<b>PWM</b>				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
<b>External interrupt</b>				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/negative
<b>Capture</b>				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/negative
<b>Timer</b>				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
<b>Melody</b>				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/negative
<b>LED drive</b>				
LED0-2	O	NMOS open drain output pins to drive LED. These pins are used as the primary function of the P20-P22 pins.	Primary	Positive/negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>RC oscillation type A/D converter</b>				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
<b>Successive approximation type A/D converter</b>				
AV <sub>SS</sub>	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV <sub>DD</sub>	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V <sub>REF</sub>	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
<b>LCD drive signal</b>				
COM0-15	O	Common output pins.	—	—
COM16-23	O	Common output pins. These pins are for the ML610Q436, but are not provided in the ML610Q435.	—	—
SEG0-63	O	Segment output pin.	—	—
<b>LCD driver power supply</b>				
V <sub>L1</sub>	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V <sub>SS</sub> and V <sub>L1</sub> , V <sub>L2</sub> , V <sub>L3</sub> , and V <sub>L4</sub> , respectively.	—	—
V <sub>L2</sub>	—		—	—
V <sub>L3</sub>	—		—	—
V <sub>L4</sub>	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
<b>For testing</b>				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
<b>Power supply</b>				
V <sub>SS</sub>	—	Negative power supply pin.	—	—
V <sub>DD</sub>	—	Positive power supply pin.	—	—
V <sub>DDL</sub>	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V <sub>SS</sub> .	—	—
V <sub>DDX</sub>	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V <sub>SS</sub> .	—	—
V <sub>PP</sub>	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected.	—	—

## TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

**Table 3 Termination of Unused Pins**

Pin	Recommended pin termination
V <sub>PP</sub>	Open
AV <sub>DD</sub>	V <sub>SS</sub>
AV <sub>SS</sub>	V <sub>SS</sub>
V <sub>REF</sub>	V <sub>SS</sub>
AIN0, AIN1	Open
V <sub>L1</sub> , V <sub>L2</sub> , V <sub>L3</sub> , V <sub>L4</sub>	Open
C1, C2, C3, C4	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V <sub>DD</sub> or V <sub>SS</sub>
P10 to P11	V <sub>DD</sub>
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 23	Open
SEG0 to 63	Open

**Note:**

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

**ELECTRICAL CHARACTERISTICS****ABSOLUTE MAXIMUM RATINGS**(V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V <sub>DD</sub>	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 2	AV <sub>DD</sub>	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 3	V <sub>PP</sub>	Ta = 25°C	-0.3 to +9.5	V
Power supply voltage 4	V <sub>DDL</sub>	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 5	V <sub>DDX</sub>	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 6	V <sub>L1</sub>	Ta = 25°C	-0.3 to +1.75	V
Power supply voltage 7	V <sub>L2</sub>	Ta = 25°C	-0.3 to +3.5	V
Power supply voltage 8	V <sub>L3</sub>	Ta = 25°C	-0.3 to +5.25	V
Power supply voltage 9	V <sub>L4</sub>	Ta = 25°C	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output current 1	I <sub>OUT1</sub>	Port3-A, Ta = 25°C	-12 to +11	mA
Output current 2	I <sub>OUT2</sub>	Port2, Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	122	mW
Storage temperature	T <sub>STG</sub>	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**(V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T <sub>OP</sub>	—	-20 to +70	°C
Operating voltage	V <sub>DD</sub>	—	1.1 to 3.6	V
	AV <sub>DD</sub>	—	2.2 to 3.6	
Operating frequency (CPU)	f <sub>OP</sub>	V <sub>DD</sub> = 1.1 to 3.6V	30k to 36k	Hz
		V <sub>DD</sub> = 1.3 to 3.6V	30k to 650k	
		V <sub>DD</sub> = 1.8 to 3.6V	30k to 4.2M	
Low-speed crystal oscillation frequency	f <sub>XTL</sub>	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C <sub>DL</sub>	—	0 to 12	pF
	C <sub>GL</sub>	—	0 to 12	
High-speed crystal/ceramic oscillation frequency	f <sub>XTH</sub>	—	4.0M / 4.096M	Hz
High-speed crystal oscillation external capacitor	C <sub>DH</sub>	—	24	pF
	C <sub>GH</sub>	—	24	
Capacitor externally connected to V <sub>DDL</sub> pin	C <sub>L0</sub>	—	1.0±30%	μF
	C <sub>L1</sub>	—	0.1±30%	
Capacitor externally connected to V <sub>DDX</sub> pin	C <sub>X</sub>	—	0.1±30%	μF
Capacitors externally connected to V <sub>L1, 2, 3, 4</sub> pins	C <sub>a, b, c, d</sub>	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C <sub>12, C34</sub>	—	1.0±30%	μF

## OPERATING CONDITIONS OF FLASH ROM

(V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T <sub>OP</sub>	At write/erase	0 to +40	°C
Operating voltage	V <sub>DD</sub>	At write/erase <sup>*1</sup>	2.75 to 3.6	V
	V <sub>DDL</sub>	At write/erase <sup>*1</sup>	2.5 to 2.75	
	V <sub>PP</sub>	At write/erase <sup>*1</sup>	7.7 to 8.3	
Write cycles	C <sub>EP</sub>	—	80	cycles
Data retention	Y <sub>DR</sub>	—	10	years

<sup>\*1</sup>: In addition the power supply to VDD pin and VPP pin, within the range 2.5V to 2.75V has to be supplied to VDDL pin when programming and erasing Flash ROM

## DC CHARACTERISTICS (1/5)

(V<sub>DD</sub> = 1.1 to 3.6V, AV<sub>DD</sub> = 2.2 to 3.6V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, Ta = -20 to +70°C, unless otherwise specified) (1/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
500kHz RC oscillation frequency	f <sub>RC</sub>	V <sub>DD</sub> = 1.3 to 3.6V	Ta = 25°C	Typ. -10%	500	Typ. +10%	kHz
			Ta = -20 to +70°C	Typ. -25%	500	Typ. +25%	
PLL oscillation frequency <sup>*4</sup>	f <sub>PLL</sub>	LSCLK = 32.768kHz V <sub>DD</sub> = 1.8 to 3.6V	-2.5%	8.192	+2.5%	MHz	1
Low-speed crystal oscillation start time <sup>*2</sup>	T <sub>XTL</sub>	—	—	0.3	2	s	
500kHz RC oscillation start time	T <sub>RC</sub>	—	—	50	500	μs	
High-speed crystal oscillation start time <sup>*3</sup>	T <sub>XTH</sub>	V <sub>DD</sub> = 1.8 to 3.6V	—	2	20	ms	
PLL oscillation start time	T <sub>PLL</sub>	V <sub>DD</sub> = 1.8 to 3.6V	—	1	10		
Low-speed oscillation stop detect time <sup>*1</sup>	T <sub>STOP</sub>	—	0.2	3	20	μs	
Reset pulse width	P <sub>RST</sub>	—	200	—	—		
Reset noise elimination pulse width	P <sub>NRST</sub>	—	—	—	0.3	ms	
Power-on reset activation power rise time	T <sub>POR</sub>	—	—	—	10		

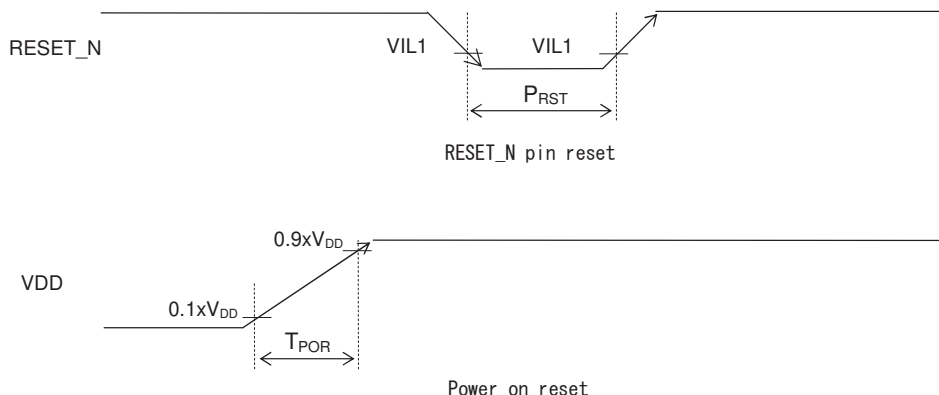
<sup>\*1</sup>: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode. "A" version (ML610Q435A/Q436A) don't have this spec.

<sup>\*2</sup>: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C<sub>GL</sub>/C<sub>DL</sub>=0pF.

<sup>\*3</sup>: Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).

<sup>\*4</sup>: 1024 clock average.

## RESET



**DC CHARACTERISTICS (2/5)**(V<sub>DD</sub> = 1.1 to 3.6V, AV<sub>DD</sub> = 2.2 to 3.6V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, Ta = -20 to +70°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
V <sub>L1</sub> voltage	V <sub>L1</sub>	V <sub>DD</sub> = 3.0V, T <sub>j</sub> = 25°C	CN4-0 = 00H	0.89	0.94	0.99	V	1
			CN4-0 = 01H	0.91	0.96	1.01		
			CN4-0 = 02H	0.93	0.98	1.03		
			CN4-0 = 03H	0.95	1.00	1.05		
			CN4-0 = 04H	0.97	1.02	1.07		
			CN4-0 = 05H	0.99	1.04	1.09		
			CN4-0 = 06H	1.01	1.06	1.11		
			CN4-0 = 07H	1.03	1.08	1.13		
			CN4-0 = 08H	1.05	1.10	1.15		
			CN4-0 = 09H	1.07	1.12	1.17		
			CN4-0 = 0AH	1.09	1.14	1.19		
			CN4-0 = 0BH	1.11	1.16	1.21		
			CN4-0 = 0CH	1.13	1.18	1.23		
			CN4-0 = 0DH	1.15	1.20	1.25		
			CN4-0 = 0EH	1.17	1.22	1.27		
			CN4-0 = 0FH	1.19	1.24	1.29		
			CN4-0 = 10H	1.21	1.26	1.31		
			CN4-0 = 11H	1.23	1.28	1.33		
			CN4-0 = 12H	1.25	1.30	1.35		
			CN4-0 = 13H	1.27	1.32	1.37		
			CN4-0 = 14H <sup>*1</sup>	1.29	1.34	1.39		
			CN4-0 = 15H <sup>*1</sup>	1.31	1.36	1.41		
			CN4-0 = 16H <sup>*1</sup>	1.33	1.38	1.43		
			CN4-0 = 17H <sup>*1</sup>	1.35	1.40	1.45		
CN4-0 = 18H <sup>*1</sup>	1.37	1.42	1.47					
CN4-0 = 19H <sup>*1</sup>	1.39	1.44	1.49					
CN4-0 = 1AH <sup>*1</sup>	1.41	1.46	1.51					
CN4-0 = 1BH <sup>*1</sup>	1.43	1.48	1.53					
CN4-0 = 1CH <sup>*1</sup>	1.45	1.50	1.55					
CN4-0 = 1DH <sup>*1</sup>	1.47	1.52	1.57					
CN4-0 = 1EH <sup>*1</sup>	1.49	1.54	1.59					
CN4-0 = 1FH <sup>*1</sup>	1.51	1.56	1.61					
V <sub>L1</sub> temperature deviation	ΔV <sub>L1</sub>	V <sub>DD</sub> = 3.0V	—	-1.5	—	mV/°C		
V <sub>L1</sub> voltage dependency	ΔV <sub>L1</sub>	V <sub>DD</sub> = 1.3 to 3.6V	—	5	20	mV/V		
V <sub>L2</sub> voltage	V <sub>L2</sub>	V <sub>DD</sub> = 3.0V, T <sub>j</sub> = 25°C 300kΩ load (V <sub>L4</sub> -V <sub>SS</sub> )	Typ. -10%	V <sub>L1</sub> ×2	Typ. +4%	V		
V <sub>L3</sub> voltage	V <sub>L3</sub>	V <sub>DD</sub> = 3.0V, T <sub>j</sub> = 25°C 300kΩ load (V <sub>L4</sub> -V <sub>SS</sub> )	Typ. -10%	V <sub>L1</sub> ×2	Typ. +4%			
V <sub>L4</sub> voltage	V <sub>L4</sub>		Typ. -10%	V <sub>L1</sub> ×3	Typ. +5%			
LCD bias voltage generation time	T <sub>BIAS</sub>	—	—	—	600			ms

\*1: When using 1/4 bias, the V<sub>L1</sub> voltage is set to typ. 1.32 V (same voltage as in CN4-0 = 13H).

**DC CHARACTERISTICS (3/5)**(V<sub>DD</sub> = 1.1 to 3.6V, AV<sub>DD</sub> = 2.2 to 3.6V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, Ta = -20 to +70°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit		
				Min.	Typ.	Max.				
BLD threshold voltage	V <sub>BLD</sub>	V <sub>DD</sub> = 1.35 to 3.6V		Typ. -2%		Typ. +2%	V	1		
									LD2-0 = 0H	1.35
									LD2-0 = 1H	1.4
									LD2-0 = 2H	1.45
									LD2-0 = 3H	1.5
									LD2-0 = 4H	1.6
									LD2-0 = 5H	1.7
									LD2-0 = 6H	1.8
									LD2-0 = 7H	1.9
									LD2-0 = 8H	2.0
									LD2-0 = 9H	2.1
									LD2-0 = 0AH	2.2
									LD2-0 = 0BH	2.3
									LD2-0 = 0CH	2.4
LD2-0 = 0DH	2.5									
LD2-0 = 0EH	2.7									
LD2-0 = 0FH	2.9									
BLD threshold voltage temperature deviation	ΔV <sub>BLD</sub>	V <sub>DD</sub> = 1.35 to 3.6V		—	0.1	—	%/°C			
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.50	μA			
			Ta = -20 to +70°C	—	—	2.50				
Supply current 2	IDD2	CPU: In HALT state (LTBC, RTC: Operating <sup>*3*5</sup> ). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.3	μA			
			Ta = -20 to +70°C	—	—	3.5				
Supply current 3	IDD3	CPU: In 32.768kHz operating state. <sup>*1*3</sup> High-speed oscillation: Stopped. LCD/BIAS circuits: Operating. <sup>*2</sup>	Ta = 25°C	—	5	7	μA			
			Ta = -20 to +70°C	—	—	12				
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating. <sup>*2</sup>	Ta = 25°C	—	70	85	μA			
			Ta = -20 to +70°C	—	—	100				
Supply current 5	IDD5	CPU: In 4.096MHz operating state. <sup>*2*3</sup> PLL: In oscillating state. LCD/BIAS circuits: Operating. <sup>*2</sup> V <sub>DD</sub> = 1.8 to 3.6V	Ta = 25°C	—	0.8	1.0	mA			
			Ta = -20 to +70°C	—	—	1.2				
Supply current 6	IDD6	CPU: In 4.096MHz operating state. <sup>*2</sup> PLL: In oscillating state. <sup>*3*4</sup> A/D: In operating state. LCD/BIAS circuits: Operating. <sup>*2</sup> V <sub>DD</sub> = AV <sub>DD</sub> = 3.0V	Ta = 25°C	—	1.5	1.6	mA			
			Ta = -20 to +70°C	—	—	2.5				

\*1: When the CPU operating rate is 100% (No HALT state).

\*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

\*3: Use 32.768kHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C<sub>GL</sub>/C<sub>DL</sub>=0pF.

\*4: Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).

\*5: Significant bits of BLKCON0~BLKCON4 registers are all "1".



**DC CHARACTERISTICS (4/5)**(V<sub>DD</sub> = 1.1 to 3.6V, AV<sub>DD</sub> = 2.2 to 3.6V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, Ta = -20 to +70°C, unless otherwise specified) (4/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22/2 <sup>nd</sup> function is selected) (P30–P35) (P40–P47) (PA0–PA7) <sup>*1</sup>	VOH1	IOH1 = -0.5mA, V <sub>DD</sub> = 1.8 to 3.6V	V <sub>DD</sub> -0.5	—	—	V	2
		IOH1 = -0.1mA, V <sub>DD</sub> = 1.3 to 3.6V	V <sub>DD</sub> -0.3	—	—		
		IOH1 = -0.03mA, V <sub>DD</sub> = 1.1 to 3.6V	V <sub>DD</sub> -0.3	—	—		
	VOL1	IOL1 = +0.5mA, V <sub>DD</sub> = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V <sub>DD</sub> = 1.3 to 3.6V	—	—	0.5		
		IOL1 = +0.03mA, V <sub>DD</sub> = 1.1 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P22/2 <sup>nd</sup> function is Not selected)	VOH2	IOH1 = -0.5mA, V <sub>DD</sub> = 1.8 to 3.6V	V <sub>DD</sub> -0.5	—	—		
		IOH1 = -0.1mA, V <sub>DD</sub> = 1.3 to 3.6V	V <sub>DD</sub> -0.3	—	—		
		IOH1 = -0.03mA, V <sub>DD</sub> = 1.1 to 3.6V	V <sub>DD</sub> -0.3	—	—		
	VOL2	IOL2 = +5mA, V <sub>DD</sub> = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V <sub>DD</sub> = 2.0 to 3.6V (when I <sup>2</sup> C mode is selected)	—	—	0.4		
Output voltage 4 (COM0–15) (COM16–23) <sup>*2</sup> (SEG0–63)	VOH4	IOH4 = -0.2mA, VL1=1.2V	V <sub>L4</sub> -0.2	—	—		
	VOMH4	IOMH4 = +0.2mA, VL1=1.2V	—	—	V <sub>L3</sub> +0.2		
	VOMH4S	IOMH4S = -0.2mA, VL1=1.2V	V <sub>L3</sub> -0.2	—	—		
	VOM4	IOM4 = +0.2mA, VL1=1.2V	—	—	V <sub>L2</sub> +0.2		
	VOM4S	IOM4S = -0.2mA, VL1=1.2V	V <sub>L2</sub> -0.2	—	—		
	VOML4	IOML4 = +0.2mA, VL1=1.2V	—	—	V <sub>L1</sub> +0.2		
	VOML4S	IOML4S = -0.2mA, VL1=1.2V	V <sub>L1</sub> -0.2	—	—		
	VOL4	IOL4 = +0.2mA, VL1=1.2V	—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7) <sup>*1</sup>	IOOH	VOH = V <sub>DD</sub> (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V <sub>SS</sub> (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V <sub>DD</sub>	0	—	1	μA	4
	IIL1	VIL1 = V <sub>SS</sub>	V <sub>DD</sub> = 1.8 to 3.6V	-600	-300	-20	
			V <sub>DD</sub> = 1.3 to 3.6V	-600	-300	-10	
V <sub>DD</sub> = 1.1 to 3.6V			-600	-300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V <sub>DD</sub>	V <sub>DD</sub> = 1.8 to 3.6V	20	300	600	
			V <sub>DD</sub> = 1.3 to 3.6V	10	300	600	
			V <sub>DD</sub> = 1.1 to 3.6V	2	300	600	
	IIL1	VIL1 = V <sub>SS</sub>	-1	—	—		
Input current 2 (NMI) (P00–P03)	IIH2	VIH2 = V <sub>DD</sub> (when pulled-down)	V <sub>DD</sub> = 1.8 to 3.6V	2	30	200	
			V <sub>DD</sub> = 1.3 to 3.6V	0.2	30	200	
			V <sub>DD</sub> = 1.1 to 3.6V	0.01	30	200	

(P10–P11) (P30–P35) (P40–P47) (PA0–PA7)**1	IIL2	VIL2 = V <sub>SS</sub> (when pulled-up)	V <sub>DD</sub> = 1.8 to 3.6V	-200	-30	-2		
			V <sub>DD</sub> = 1.3 to 3.6V	-200	-30	-0.2		
			V <sub>DD</sub> = 1.1 to 3.6V	-200	-30	-0.01		
	IIH2Z	VIH2 = V <sub>DD</sub> (in high-impedance state)	—	—	1			
	IIL2Z	VIL2 = V <sub>SS</sub> (in high-impedance state)	-1	—	—			

\*1: ML610Q435 only

\*2: ML610Q436 only

**DC CHARACTERISTICS (5/5)**(V<sub>DD</sub> = 1.1 to 3.6V, AV<sub>DD</sub> = 2.2 to 3.6V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, Ta = -20 to +70°C, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)**1	VIH1	V <sub>DD</sub> = 1.3 to 3.6V	0.7 ×V <sub>DD</sub>	—	V <sub>DD</sub>	V	5
		V <sub>DD</sub> = 1.1 to 3.6V	0.7 ×V <sub>DD</sub>	—	V <sub>DD</sub>		
	VIL1	V <sub>DD</sub> = 1.3 to 3.6V	0	—	0.3 ×V <sub>DD</sub>		
		V <sub>DD</sub> = 1.1 to 3.6V	0	—	0.2 ×V <sub>DD</sub>		
Hysteresis width (RESET_N) (TEST_N) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)**1	ΔVT	V <sub>DD</sub> = 2.0 to 3.6V	0.05 ×V <sub>DD</sub>	0.18 ×V <sub>DD</sub>	0.4 ×V <sub>DD</sub>	V	5
		V <sub>DD</sub> = 1.1 to 3.6V	0.02 ×V <sub>DD</sub>	0.18 ×V <sub>DD</sub>	0.4 ×V <sub>DD</sub>		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V <sub>DD</sub>	—	V <sub>DD</sub>	pF	—
	VIL2	—	0	—	0.3 ×V <sub>DD</sub>		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)**1	CIN	f = 10kHz V <sub>rms</sub> = 50mV Ta = 25°C	—	—	5	pF	—

\*1: ML610Q435 only

**HYSTERESIS WIDTH**