



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



ML610Q438/ML610Q439

User's Manual

Notes

- 1) The information contained herein is subject to change without notice.
- 2) Although LAPIS Semiconductor is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. LAPIS Semiconductor shall have no responsibility for any damages arising out of the use of our Products beyond the rating specified by LAPIS Semiconductor.
- 3) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.
- 4) The technical information specified herein is intended only to show the typical functions of the Products and examples of application circuits for the Products. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Semiconductor or any third party with respect to the information contained in this document; therefore LAPIS Semiconductor shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.
- 5) The Products are intended for use in general electronic equipment (i.e. AV/OA devices, communication, consumer systems, gaming/entertainment sets) as well as the applications indicated in this document.
- 6) The Products specified in this document are not designed to be radiation tolerant.
- 7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a LAPIS Semiconductor representative: transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.
- 8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.
- 9) LAPIS Semiconductor shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.
- 10) LAPIS Semiconductor has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Semiconductor does not warrant that such information is error-free and LAPIS Semiconductor shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.
- 11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. LAPIS Semiconductor shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.
- 12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.
- 13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Semiconductor.

Copyright 2010 – 2015 LAPIS Semiconductor Co., Ltd.

LAPIS Semiconductor Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku,
Yokohama 222-8575, Japan
<http://www.lapis-semi.com/en/>

Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q438/ML610Q439.

The following manuals are also available. Read them as necessary.

- nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.
- MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.
- CCU8 User's Manual
Description on the method of operating the compiler.
- CCU8 Programming Guide
Description on the method of programming.
- CCU8 Language Reference
Description on the language specifications.
- DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.
- IDEU8 User's Manual
Description on the integrated development environment IDEU8.
- uEASE User's Manual
Description on the on-chip debug tool uEASE.
- uEASE connection Manual
Description about the connection between uEASE and ML610Qxxx.
- FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
◆ Numeric value	xxh, xxH xxb	Indicates a hexadecimal number. x: Any value in the range of 0 to F Indicates a binary number; "b" may be omitted. x: A value 0 or 1
◆ Unit	word, W byte, B nibble, N mega-, M kilo-, K kilo-, k milli-, m micro-, μ nano-, n second, s (lower case)	1 word = 16 bits 1 byte = 8 bits 1 nibble = 4 bits 10^6 $2^{10} = 1024$ $10^3 = 1000$ 10^{-3} 10^{-6} 10^{-9} second
◆ Terminology	"H" level, "1" level "L" level, "0" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics. Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.
◆ Register description		R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

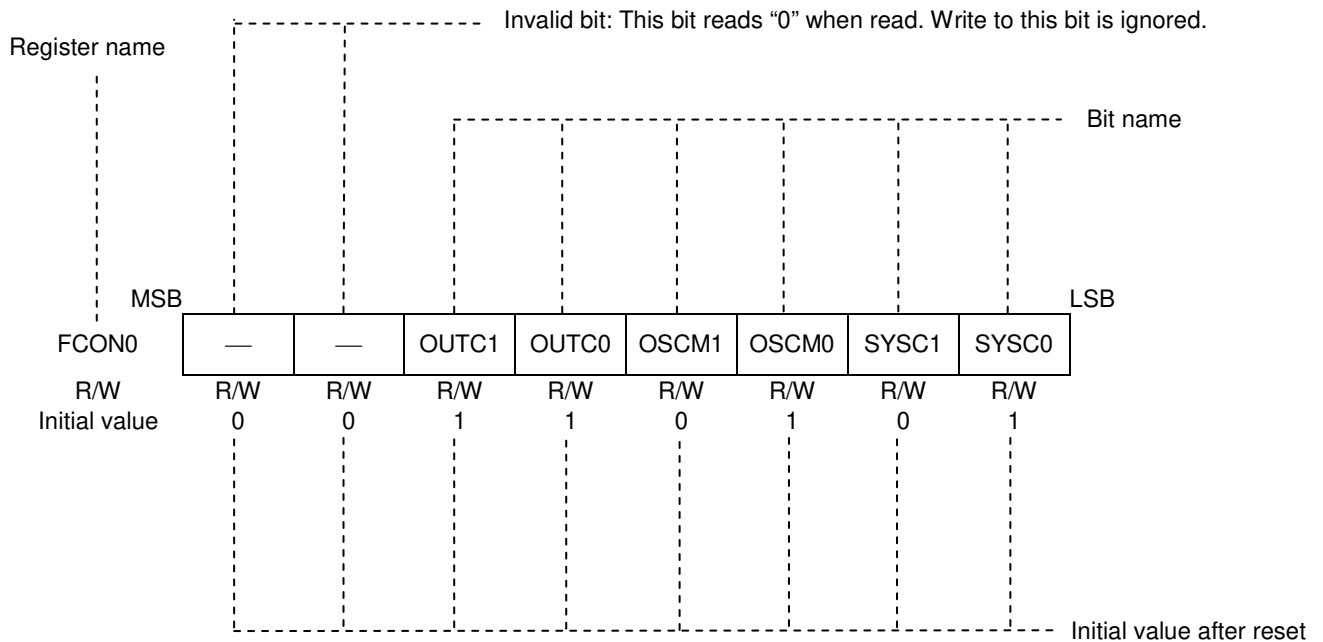


Table of Contents

Chapter 1

1. Overview.....	1-1
1.1 Features.....	1-1
1.2 Configuration of Functional Blocks.....	1-5
1.2.1 Block Diagram of ML610Q438.....	1-5
1.2.2 Block Diagram of ML610Q439.....	1-6
1.3 Pins.....	1-7
1.3.1 Pin Layout.....	1-7
1.3.1.1 Pin Layout of ML610Q438 LQFP Package.....	1-7
1.3.1.2 Pin Layout of ML610Q439P LQFP Package.....	1-8
1.3.1.3 Pin Layout of ML610Q438 Chip.....	1-9
1.3.1.4 Pin Layout of ML610Q439 Chip.....	1-10
1.3.1.5 Pad Coordinates of ML610Q438 Chip.....	1-11
1.3.1.6 Pad Coordinates of ML610Q439 Chip.....	1-12
1.3.2 List of Pins.....	1-13
1.3.3 Description of Pins.....	1-17
1.3.4 Termination of Unused Pins.....	1-21
1.3.5 The main difference points of ML610Q438 and ML610Q439.....	1-21

Chapter 2

2. CPU and Memory Space.....	2-1
2.1 Overview.....	2-1
2.2 Program Memory Space.....	2-1
2.3 Data Memory Space.....	2-2
2.4 Instruction Length.....	2-2
2.5 Data Type.....	2-2
2.6 Description of Registers.....	2-3
2.6.1 List of Registers.....	2-3
2.6.2 Data Segment Register (DSR).....	2-4

Chapter 3

3. Reset Function.....	3-1
3.1 Overview.....	3-1
3.1.1 Features.....	3-1
3.1.2 Configuration.....	3-1
3.1.3 List of Pin.....	3-1
3.2 Description of Registers.....	3-2
3.2.1 List of Registers.....	3-2
3.2.2 Reset Status Register (RSTAT).....	3-2
3.3 Description of Operation.....	3-3
3.3.1 Operation of System Reset Mode.....	3-3

Chapter 4

4. MCU Control Function.....	4-1
4.1 Overview.....	4-1
4.1.1 Features.....	4-1
4.1.2 Configuration.....	4-1
4.2 Description of Registers.....	4-2
4.2.1 List of Registers.....	4-2
4.2.2 Stop Code Acceptor (STPACP).....	4-3
4.2.3 Standby Control Register (SBYCON).....	4-4
4.2.4 Block Control Register 0 (BLKCON0).....	4-5
4.2.5 Block Control Register 1 (BLKCON1).....	4-6

4.2.6	Block Control Register 2 (BLKCON2).....	4-7
4.2.7	Block Control Register 3 (BLKCON3).....	4-8
4.2.8	Block Control Register 4 (BLKCON4).....	4-9
4.3	Description of Operation.....	4-11
4.3.1	Program Run Mode.....	4-11
4.3.2	HALT Mode	4-11
4.3.3	STOP Mode	4-12
4.3.3.1	STOP Mode When CPU Operates with Low-Speed Clock	4-12
4.3.3.2	STOP Mode When CPU Operates with High-Speed Clock	4-13
4.3.3.3	Note on Return Operation from STOP/HALT Mode	4-14
4.3.4	Block Control Function.....	4-15

Chapter 5

5.	Interrupts (INTs).....	5-1
5.1	Overview.....	5-1
5.1.1	Features.....	5-1
5.2	Description of Registers.....	5-2
5.2.1	List of Registers	5-2
5.2.2	Interrupt Enable Register 1 (IE1).....	5-3
5.2.3	Interrupt Enable Register 2 (IE2).....	5-5
5.2.4	Interrupt Enable Register 3 (IE3).....	5-6
5.2.5	Interrupt Enable Register 4 (IE4).....	5-7
5.2.6	Interrupt Enable Register 5 (IE5).....	5-8
5.2.7	Interrupt Enable Register 6 (IE6).....	5-9
5.2.8	Interrupt Enable Register 7 (IE7).....	5-11
5.2.9	Interrupt Request Register 0 (IRQ0).....	5-12
5.2.10	Interrupt Request Register 1 (IRQ1).....	5-13
5.2.11	Interrupt Request Register 2 (IRQ2).....	5-15
5.2.12	Interrupt Request Register 3 (IRQ3).....	5-16
5.2.13	Interrupt Request Register 4 (IRQ4).....	5-17
5.2.14	Interrupt Request Register 5 (IRQ5).....	5-18
5.2.15	Interrupt Request Register 6 (IRQ6).....	5-19
5.2.16	Interrupt Request Register 7 (IRQ7).....	5-21
5.3	Description of Operation.....	5-23
5.3.1	Maskable Interrupt Processing.....	5-24
5.3.2	Non-Maskable Interrupt Processing.....	5-24
5.3.3	Software Interrupt Processing.....	5-24
5.3.4	Notes on Interrupt Routine.....	5-25
5.3.5	Interrupt Disable State	5-28

Chapter 6

6.	Clock Generation Circuit.....	6-1
6.1	Overview.....	6-1
6.1.1	Features.....	6-1
6.1.2	Configuration.....	6-1
6.1.3	List of Pins	6-2
6.2	Description of Registers.....	6-2
6.2.1	List of Registers	6-2
6.2.2	Frequency Control Register 0 (FCON0).....	6-3
6.2.3	Frequency Control Register 1 (FCON1).....	6-5
6.3	Description of Operation.....	6-6
6.3.1	Low-Speed Clock.....	6-6
6.3.1.1	Low-Speed Clock Generation Circuit.....	6-6
6.3.1.2	Operation of Low-Speed Clock Generation Circuit	6-7
6.3.2	High-Speed Clock.....	6-8
6.3.2.1	500 kHz RC Oscillation.....	6-8

6.3.2.2	Crystal/Ceramic Oscillation Mode	6-9
6.3.2.3	Built-in PLL Oscillation Mode	6-10
6.3.2.4	External Clock Input Mode	6-10
6.3.2.5	2 MHz RC Oscillation	6-11
6.3.2.6	Operation of High-Speed Clock Generation Circuit.....	6-12
6.3.3	Switching of System Clock.....	6-14
6.4	Specifying port registers	6-16
6.4.1	Functioning P21 (OUTCLK) as the high speed clock output	6-16
6.4.2	Functioning P22 (LSCLK) as the low speed clock output.....	6-16

Chapter 7

7.	Time Base Counter	7-1
7.1	Overview.....	7-1
7.1.1	Features.....	7-1
7.1.2	Configuration	7-1
7.2	Description of Registers.....	7-3
7.2.1	List of Registers	7-3
7.2.2	Low-Speed Time Base Counter (LTBR)	7-4
7.2.3	High-Speed Time Base Counter Divide Register (HTBDR)	7-5
7.2.4	Low-Speed Time Base Counter Frequency Adjustment Registers L and H (LTBADJL, LTBADJH).....	7-6
7.3	Description of Operation.....	7-7
7.3.1	Low-Speed Time Base Counter	7-7
7.3.2	High-Speed Time Base Counter	7-8
7.3.3	Low-Speed Time Base Counter Frequency Adjustment Function.....	7-9

Chapter 8

8.	Capture.....	8-1
8.1	Overview.....	8-1
8.1.1	Features.....	8-1
8.1.2	Configuration	8-1
8.1.3	List of Pins	8-1
8.2	Description of Registers.....	8-2
8.2.1	List of Registers	8-2
8.2.2	Capture Control Register (CAPCON).....	8-3
8.2.3	Capture Status Register (CAPSTAT).....	8-4
8.2.4	Capture Data Register 0 (CAPR0)	8-5
8.2.5	Capture Data Register 1 (CAPR1)	8-6
8.3	Description of Operation.....	8-7

Chapter 9

9.	1 kHz Timer (1kHzTM).....	9-1
9.1	Overview.....	9-1
9.1.1	Features.....	9-1
9.1.2	Configuration	9-1
9.2	Description of Registers.....	9-2
9.2.1	List of Registers	9-2
9.2.2	1 kHz Timer Count Registers (T1KCRL, T1KCRH).....	9-3
9.2.3	1 kHz Timer Control Register (T1KCON)	9-4
9.3	Description of Operation.....	9-5

Chapter 10

10.	Timers	10-1
10.1	Overview.....	10-1
10.1.1	Features.....	10-1
10.1.2	Configuration	10-1

10.2	Description of Registers.....	10-2
10.2.1	List of Registers.....	10-2
10.2.2	Timer 0 Data Register (TM0D).....	10-3
10.2.3	Timer 1 Data Register (TM1D).....	10-4
10.2.4	Timer 2 Data Register (TM2D).....	10-5
10.2.5	Timer 3 Data Register (TM3D).....	10-6
10.2.6	Timer 0 Counter Register (TM0C).....	10-7
10.2.7	Timer 1 Counter Register (TM1C).....	10-8
10.2.8	Timer 2 Counter Register (TM2C).....	10-9
10.2.9	Timer 3 Counter Register (TM3C).....	10-10
10.2.10	Timer 0 Control Register 0 (TM0CON0).....	10-11
10.2.11	Timer 1 Control Register 0 (TM1CON0).....	10-13
10.2.12	Timer 2 Control Register 0 (TM2CON0).....	10-14
10.2.13	Timer 3 Control Register 0 (TM3CON0).....	10-16
10.2.14	Timer 0 Control Register 1 (TM0CON1).....	10-17
10.2.15	Timer 1 Control Register 1 (TM1CON1).....	10-18
10.2.16	Timer 2 Control Register 1 (TM2CON1).....	10-19
10.2.17	Timer 3 Control Register 1 (TM3CON1).....	10-19
10.3	Description of Operation.....	10-20

Chapter 11

11.	PWM.....	11-1
11.1	Overview.....	11-1
11.1.1	Features.....	11-1
11.1.2	Configuration.....	11-1
11.1.3	List of Pins.....	11-2
11.2	Description of Registers.....	11-2
11.2.1	List of Registers.....	11-2
11.2.2	PWM0 Period Registers (PW0PL, PW0PH).....	11-3
11.2.3	PWM1 Period Registers (PW1PL, PW1PH).....	11-4
11.2.4	PWM2 Period Registers (PW2PL, PW2PH).....	11-5
11.2.5	PWM0 Duty Registers (PW0DL, PW0DH).....	11-6
11.2.6	PWM1 Duty Registers (PW1DL, PW1DH).....	11-7
11.2.7	PWM2 Duty Registers (PW2DL, PW2DH).....	11-8
11.2.8	PWM0 Counter Registers (PW0CH, PW0CL).....	11-9
11.2.9	PWM1 Counter Registers (PW1CH, PW1CL).....	11-10
11.2.10	PWM2 Counter Registers (PW2CH, PW2CL).....	11-11
11.2.11	PWM0 Control Register 0 (PW0CON0).....	11-12
11.2.12	PWM1 Control Register 0 (PW1CON0).....	11-13
11.2.13	PWM2 Control Register 0 (PW2CON0).....	11-14
11.2.14	PWM0 Control Register 1 (PW0CON1).....	11-15
11.2.15	PWM1 Control Register 1 (PW1CON1).....	11-16
11.2.16	PWM2 Control Register 1 (PW2CON1).....	11-17
11.3	Description of Operation.....	11-18
11.4	Specifying port registers.....	11-20
11.4.1	Functioning P43 (PWM0) as the PWM0 output.....	11-20
11.4.2	Functioning P34 (PWM0) as the PWM0 output.....	11-21
11.4.3	Functioning P47 (PWM1) as the PWM1 output.....	11-22
11.4.4	Functioning P35 (PWM1) as the PWM1 output.....	11-23
11.4.5	Functioning P20 (PWM2) as the PWM2 output.....	11-24
11.4.6	Functioning P30 (PWM2) as the PWM2 output.....	11-25

Chapter 12

12.	Watchdog Timer.....	12-1
12.1	Overview.....	12-1
12.1.1	Features.....	12-1
12.1.2	Configuration.....	12-1

12.2 Description of Registers.....	12-2
12.2.1 List of Registers.....	12-2
12.2.2 Watchdog Timer Control Register (WDTCON).....	12-3
12.2.3 Watchdog Timer Mode Register (WDTMOD).....	12-4
12.3 Description of Operation.....	12-5

Chapter 13

13. Synchronous Serial Port.....	13-1
13.1 Overview.....	13-1
13.1.1 Features.....	13-1
13.1.2 Configuration.....	13-1
13.1.3 List of Pins.....	13-2
13.2 Description of Registers.....	13-3
13.2.1 List of Registers.....	13-3
13.2.2 Serial Port Transmit/Receive Buffers (SIO0BUFL, SIO0BUFH).....	13-4
13.2.3 Serial Port Control Register (SIO0CON).....	13-5
13.2.4 Serial Port Mode Register 0 (SIO0MOD0).....	13-6
13.2.5 Serial Port Mode Register 1 (SIO0MOD1).....	13-7
13.3 Description of Operation.....	13-8
13.3.1 Transmit Operation.....	13-8
13.3.2 Receive Operation.....	13-9
13.3.3 Transmit/Receive Operation.....	13-10
13.4 Specifying port registers.....	13-11
13.4.1 Functioning P42 (SOUT0), P41 (SCK0) and P40 (SIN0) as the SSIO/ "Master mode".....	13-11
13.4.2 Functioning P42 (SOUT0), P41 (SCK0) and P40 (SIN0) as the SSIO/ "Slave mode".....	13-12
13.4.3 Functioning P46 (SOUT0), P45 (SCK0) and P44 (SIN0) as the SSIO/ "Master mode".....	13-13
13.4.4 Functioning P46 (SOUT0), P45 (SCK0) and P44 (SIN0) as the SSIO/ "Slave mode".....	13-14
13.5 About timer0/1 int clock for the transfer clock of the synchronous serial port.....	13-15

Chapter 14

14. UART.....	14-1
14.1 Overview.....	14-1
14.1.1 Features.....	14-1
14.1.2 Configuration.....	14-1
14.1.3 List of Pins.....	14-1
14.2 Description of Registers.....	14-2
14.2.1 List of Registers.....	14-2
14.2.2 UART0 Transmit/Receive Buffer (UA0BUF).....	14-3
14.2.3 UART0 Control Register (UA0CON).....	14-4
14.2.4 UART0 Mode Register 0 (UA0MOD0).....	14-5
14.2.5 UART0 Mode Register 1 (UA0MOD1).....	14-6
14.2.6 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH).....	14-8
14.2.7 UART0 Status Register (UA0STAT).....	14-9
14.3 Description of Operation.....	14-11
14.3.1 Transfer Data Format.....	14-11
14.3.2 Baud Rate.....	14-12
14.3.3 Transmit Data Direction.....	14-13
14.3.4 Transmit Operation.....	14-14
14.3.5 Receive Operation.....	14-16
14.4 Specifying port registers.....	14-18
14.4.1 Functioning P43(TXD0) and P42(RXD0) as the UART.....	14-18
14.4.2 Functioning P43(TXD0) and P02(RXD0) as the UART.....	14-19

Chapter 15

15. I ² C Bus Interface.....	15-1
15.1 Overview.....	15-1
15.1.1 Features.....	15-1

15.1.2	Configuration	15-1
15.1.3	List of Pins	15-1
15.2	Description of Registers.....	15-2
15.2.1	List of Registers	15-2
15.2.2	I ² C Bus 0 Receive Register (I2C0RD).....	15-3
15.2.3	I ² C Bus 0 Slave Address Register (I2C0SA)	15-4
15.2.4	I ² C Bus 0 Transmit Data Register (I2C0TD).....	15-5
15.2.5	I ² C Bus 0 Control Register (I2C0CON).....	15-6
15.2.6	I ² C Bus 0 Mode Register (I2C0MOD).....	15-7
15.2.7	I ² C Bus 0 Status Register (I2C0STAT)	15-8
15.3	Description of Operation.....	15-9
15.3.1	Communication Operating Mode.....	15-9
15.3.1.1	Start Condition.....	15-9
15.3.1.2	Repeated Condition	15-9
15.3.1.3	Slave Address Transmit Mode.....	15-9
15.3.1.4	Data Transmit Mode	15-9
15.3.1.5	Data Receive Mode	15-9
15.3.1.6	Control Register Setting Wait State.....	15-9
15.3.1.7	Stop Condition.....	15-9
15.3.2	Communication Operation Timing	15-10
15.3.3	Operation Waveforms	15-12
15.4	Specifying port registers	15-13
15.4.1	Functioning P41(SCL) and P40(SDA) as the I2C	15-13

Chapter 16

16.	NMI Pin	16-1
16.1	Overview.....	16-1
16.1.1	Features.....	16-1
16.1.2	Configuration	16-1
16.1.3	List of Pins	16-1
16.2	Description of Registers.....	16-2
16.2.1	List of Registers	16-2
16.2.2	NMI Data Register (NMID).....	16-3
16.2.3	NMI Control Register (NMICON).....	16-4
16.3	Description of Operation.....	16-5
16.3.1	Interrupt Request.....	16-5

Chapter 17

17.	Port 0.....	17-1
17.1	Overview.....	17-1
17.1.1	Features.....	17-1
17.1.2	Configuration	17-1
17.1.3	List of Pins	17-2
17.2	Description of Registers.....	17-3
17.2.1	List of Registers	17-3
17.2.2	Port 0 Data Register (P0D)	17-4
17.2.3	Port 0 Control Registers 0, 1 (P0CON0, P0CON1)	17-5
17.2.4	External Interrupt Control Registers 0, 1 (EXICON0, EXICON1).....	17-6
17.2.5	External Interrupt Control Register 2 (EXICON2)	17-7
17.3	Description of Operation.....	17-9
17.3.1	External Interrupt	17-9
17.3.2	Interrupt Request.....	17-9

Chapter 18

18.	Port 1.....	18-1
18.1	Overview.....	18-1
18.1.1	Features.....	18-1

18.1.2	Configuration	18-1
18.1.3	List of Pins	18-1
18.2	Description of Registers.....	18-2
18.2.1	List of Registers	18-2
18.2.2	Port 1 Data Register (P1D)	18-3
18.2.3	Port 1 Control Registers 0, 1 (P1CON0, P1CON1)	18-4
18.3	Description of Operation.....	18-5
18.3.1	Input Port Function	18-5
18.3.2	Secondary Function	18-5

Chapter 19

19.	Port 2.....	19-1
19.1	Overview.....	19-1
19.1.1	Features	19-1
19.1.2	Configuration	19-1
19.1.3	List of Pins	19-1
19.2	Description of Registers.....	19-2
19.2.1	List of Registers	19-2
19.2.2	Port 2 Data Register (P2D)	19-3
19.2.3	Port 2 control registers 0, 1 (P2CON0, P2CON1)	19-4
19.2.4	Port 2 Mode Register , Port 2 Mode Register1 (P2MOD0, P2MOD1).....	19-5
19.2.5	Port 2 Mode Register 2 (P2MOD2)	19-6
19.3	Description of Operation.....	19-8
19.3.1	Output Port Function.....	19-8
19.3.2	Secondary and Tertiary Function.....	19-8

Chapter 20

20.	Port 3.....	20-1
20.1	Overview.....	20-1
20.1.1	Features	20-1
20.1.2	Configuration	20-1
20.1.3	List of Pins	20-2
20.2	Description of Registers.....	20-3
20.2.1	List of Registers	20-3
20.2.2	Port 3 data register (P3D).....	20-4
20.2.3	Port 3 Direction Register (P3DIR).....	20-5
20.2.4	Port 3 control registers 0, 1 (P3CON0, P3CON1)	20-6
20.2.5	Port 3 mode registers 0, 1 (P3MOD0, P3MOD1)	20-8
20.3	Description of Operation.....	20-10
20.3.1	Input/Output Port Functions.....	20-10
20.3.2	Secondary and Tertiary Functions	20-10

Chapter 21

21.	Port 4.....	21-1
21.1	Overview.....	21-1
21.1.1	Features	21-1
21.1.2	Configuration	21-1
21.1.3	List of Pins	21-2
21.2	Description of Registers.....	21-3
21.2.1	List of Registers	21-3
21.2.2	Port 4 Data Register (P4D)	21-4
21.2.3	Port 4 Direction Register (P4DIR).....	21-5
21.2.4	Port 4 Control Registers 0, 1 (P4CON0, P4CON1)	21-6
21.2.5	Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)	21-8
21.3	Description of Operation.....	21-11
21.3.1	Input/Output Port Functions.....	21-11
21.3.2	Secondary and Tertiary Functions	21-11

Chapter 22

22. Port A.....	22-1
22.1 Overview.....	22-1
22.1.1 Features.....	22-1
22.1.2 Configuration.....	22-1
22.1.3 List of Pins.....	22-1
22.2 Description of Registers.....	22-2
22.2.1 List of Registers.....	22-2
22.2.2 Port A Data Register (PAD).....	22-3
22.2.3 Port A Direction Register (PADIR).....	22-4
22.2.4 Port A Control Registers 0, 1 (PACON0, PACON1).....	22-5
22.3 Description of Operation.....	22-7
22.3.1 Input/Output Port Functions.....	22-7

Chapter 23

23. Melody Driver.....	23-1
23.1 Overview.....	23-1
23.1.1 Features.....	23-1
23.1.2 Configuration.....	23-1
23.1.3 List of Pins.....	23-1
23.2 Description of Registers.....	23-2
23.2.1 List of Registers.....	23-2
23.2.2 Melody 0 Control Register (MD0CON).....	23-3
23.2.3 Melody 0 Tempo Code Register (MD0TMP).....	23-4
23.2.4 Melody 0 Scale Code Register (MD0TON).....	23-5
23.2.5 Melody 0 Tone Length Code Register (MD0LEN).....	23-6
23.3 Description of Operation.....	23-7
23.3.1 Operation of Melody Output.....	23-7
23.3.2 Tempo Codes.....	23-8
23.3.3 Tone Length Codes.....	23-9
23.3.4 Scale Codes.....	23-10
23.3.5 Example of Using Melody Circuit.....	23-11
23.3.6 Operations of Buzzer Output.....	23-12
23.4 Specifying port registers.....	23-13
23.4.1 Functioning P22 (MD0) as the Melody or Buzzer output.....	23-13

Chapter 24

24. RC Oscillation Type A/D Converter.....	24-1
24.1 Overview.....	24-1
24.1.1 Features.....	24-1
24.1.2 Configuration.....	24-1
24.1.3 List of Pins.....	24-2
24.2 Description of Registers.....	24-3
24.2.1 List of Registers.....	24-3
24.2.2 RC-ADC Counter A Registers (RADCA0–2).....	24-4
24.2.3 RC-ADC Counter B Registers (RADCB0–2).....	24-5
24.2.4 RC-ADC Mode Register (RADMOD).....	24-6
24.2.5 RC-ADC Control Register (RADCON).....	24-7
24.3 Description of Operation.....	24-8
24.3.1 RC Oscillator Circuits.....	24-8
24.3.2 Counter A/Counter B Reference Modes.....	24-11
24.3.3 Example of Use of RC Oscillation Type A/D Converter.....	24-15
24.3.4 Monitoring RC Oscillation.....	24-20
24.4 Specifying port registers.....	24-21
24.4.1 Functioning P35(RCM), P34(RCT0), P33(RT0), P32(RS0), P31(CS0) and P30(IN0) as the RC-ADC(Ch0).....	24-21

24.4.2	Functioning P47(RT1), P46(RS1), P45(CS1) and P44(IN1) as the RC-ADC(Ch1).....	24-22
--------	---	-------

Chapter 25

25.	Successive Approximation Type A/D Converter.....	25-1
25.1	Overview.....	25-1
25.1.1	Features.....	25-1
25.1.2	Configuration.....	25-1
25.1.3	List of Pins.....	25-2
25.2	Description of Registers.....	25-3
25.2.1	List of Registers.....	25-3
25.2.2	SA-ADC Result Register 0L (SADR0L).....	25-4
25.2.3	SA-ADC Result Register 0H (SADR0H).....	25-4
25.2.4	SA-ADC Result Register 1L (SADR1L).....	25-5
25.2.5	SA-ADC Result Register 1H (SADR1H).....	25-5
25.2.6	SA-ADC Control Register 0 (SADCON0).....	25-6
25.2.7	SA-ADC Control Register 1 (SADCON1).....	25-7
25.2.8	SA-ADC Mode Register 0 (SADMOD0).....	25-8
25.2.9	Amplifier Offset Register (AMPOFFS).....	25-9
25.2.10	Amplifier Gain Register (AMPGAIN).....	25-10
25.2.11	Amplifier Control Register 0 (AMPCON0).....	25-11
25.3	Description of Operation.....	25-13
25.3.1	Analog Input Settings.....	25-13
25.3.2	Settings of A/D Conversion Channels.....	25-15
25.3.3	Operation of the Successive Approximation A/D Converter in Direct Input.....	25-16
25.3.4	Operation of the Successive Approximation A/D Converter in Amplification Input.....	25-17
25.3.5	Operation of the Successive Approximation A/D Converter in Differential Amplification Input.....	25-18

Chapter 26

26.	LCD Drivers.....	26-1
26.1	Overview.....	26-1
26.1.1	Features.....	26-3
26.1.2	Configuration of the LCD Drivers.....	26-4
26.1.3	Configuration of the Bias Generation Circuit.....	26-5
26.1.4	List of Pins.....	26-6
26.2	Description of Registers.....	26-9
26.2.1	List of Registers.....	26-9
26.2.2	Bias Circuit Control Register 0 (BIASCON).....	26-10
26.2.3	Display Control Register (DSPCNT).....	26-11
26.2.4	Display Mode Register 0 (DSPMOD0).....	26-12
26.2.5	Display Mode Register 1 (DSPMOD1).....	26-14
26.2.6	Display Control Register (DSPCON).....	26-15
26.2.7	Display Allocation Register A (DS0C0A to DS63C7A).....	26-16
26.2.8	Display Allocation Register B (DS0C0B to DS63C7B).....	26-18
26.2.9	Display Registers (DSPR00 to DSPRFE).....	26-20
26.2.10	Segout Data Registers 0 (SEGOUT0).....	26-35
26.2.11	Segout Data Registers 1 (SEGOUT1).....	26-36
26.2.12	Segout Data Registers 2 (SEGOUT2).....	26-37
26.2.13	Segout Data Registers 3 (SEGOUT3).....	26-38
26.3	Description of Operation.....	26-39
26.3.1	Operation of LCD Drivers and Bias Generation Circuit.....	26-39
26.3.2	Segment Mapping When the Programmable Display Allocation Function is Not Used.....	26-40
26.3.3	Segment Mapping When the Programmable Display Allocation Function is Used.....	26-41
26.3.4	Common Output Waveforms.....	26-43
26.3.5	Segment Output Waveform.....	26-45

Chapter 27

27.	Battery Level Detector.....	27-1
-----	-----------------------------	------

27.1 Overview.....	27-1
27.1.1 Features.....	27-1
27.1.2 Configuration.....	27-1
27.2 Description of Registers.....	27-2
27.2.1 List of Registers.....	27-2
27.2.2 Battery Level Detector Control Register 0 (BLDCON0).....	27-3
27.2.3 Battery Level Detector Control Register 1 (BLDCON1).....	27-4
27.3 Description of Operation.....	27-5
27.3.1 Threshold Voltage.....	27-5
27.3.2 Operation of Battery Level Detector.....	27-6

Chapter 28

28. Power Supply Circuit.....	28-1
28.1 Overview.....	28-1
28.1.1 Features.....	28-1
28.1.2 Configuration.....	28-1
28.1.3 List of Pins.....	28-1
28.2 Description of Operation.....	28-2

Chapter 29

29. On-Chip Debug Function.....	29-1
29.1 Overview.....	29-1
29.2 Method of Connecting to On-Chip Debug Emulator.....	29-1
29.3 Flash Memory Rewrite Function.....	29-2

Appendixes

Appendix A Registers.....	A-1
Appendix B Package Dimensions.....	B-1
Appendix C Electrical Characteristics.....	C-1
Appendix D Application Circuit Example.....	D-1
Appendix E Check List.....	E-1

Revision History

Revision History.....	R-1
-----------------------	-----

Chapter 1

Overview

1. Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I²C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.

The on-chip debug function that is installed enables program debugging and programming.

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - 30.5 μ s (@32.768 kHz system clock)
 - 0.24 μ s (@4.096 MHz system clock)
- Internal memory
 - Internal 128KByte Flash ROM (64K \times 16 bits) (including unusable 1KByte TEST area)
 - Internal 6KByte Data RAM (6144 \times 8 bits), 1KByte Display Allocation RAM (1024 \times 8bit)
 - Internal 192-byte RAM for display
- Interrupt controller
 - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
 - 27 maskable interrupt sources (Internal sources: 19, External sources: 8)
- Time base counter
 - Low-speed time base counter \times 1 channel
 - Frequency compensation (Compensation range: Approx. -488 ppm to $+488$ ppm. Compensation accuracy: Approx. 0.48 ppm)
 - High-speed time base counter \times 1 channel
- Watchdog timer
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
 - 8 bits \times 4 channels (16-bit configuration available)
- 1 kHz timer
 - 10 Hz/1 Hz interrupt function

- Capture
 - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
 - Resolution 16 bits × 3 channel
- Synchronous serial port
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
 - Timer interrupt is used as a serial clock and selection is possible
- UART
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)
- Melody driver
 - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
 - Tone length: 63 types
 - Tempo: 15 types
 - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
 - 24-bit counter
 - Time division × 2 channels
- Successive approximation type A/D converter
 - 12-bit A/D converter
 - Input × 2 channels
- General-purpose ports
 - Non-maskable interrupt input port × 1 channel
 - Input-only port × 10 channels (including secondary functions)
 - Output-only port × 3 channels (including secondary functions)
 - Input/output port
20 channels (including secondary functions)

- LCD driver
 - Dot matrix can be supported.
 - ML610Q438: 1344 dots max. (56 seg × 24 com)
 - ML610Q439: 1024 dots max. (64 seg × 16 com)
 - 1/1 to 1/24 duty
 - 1/3 or 1/4 bias (built-in bias generation circuit)
 - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
 - Bias voltage multiplying clock selectable (8 types)
 - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
 - Programmable display allocation function (available only when 1/1~1/8 duty is selected)
- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected
 - Reset by the watchdog timer (WDT) overflow
- Power supply voltage detect function
 - Judgment voltages: One of 16 levels
 - Judgment accuracy: ±2% (Typ.)
- Clock
 - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
 - Crystal oscillation (32.768 kHz)
 - High-speed clock:
 - Built-in RC oscillation (2M/500kHz)
 - Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
 - Selection of high-speed clock mode by software:
 - Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Guaranteed operating range
 - Operating temperature: -20°C to +70°C (non-P version) -40°C to +85°C (P version)
 - Operating voltage: $V_{DD} = 1.1V$ to 3.6V, $AV_{DD} = 2.2V$ to 3.6V

- Product name – Supported Function
The line-up of the ML610Q438 and ML610Q439 is below.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q438-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q439-xxxWA	Flash ROM	-20°C to +70°C	Yes

-144-pin plastic LQFP -	ROM type	Operating temperature	Product availability
ML610Q438-xxxTC	Flash ROM	-20°C to +70°C	Yes
ML610Q439P-xxxTC	Flash ROM	-40°C to +85°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)

Q:Flash ROM version

P: Wide range temperature version

WA: Chip

TC: LQFP

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML610Q438

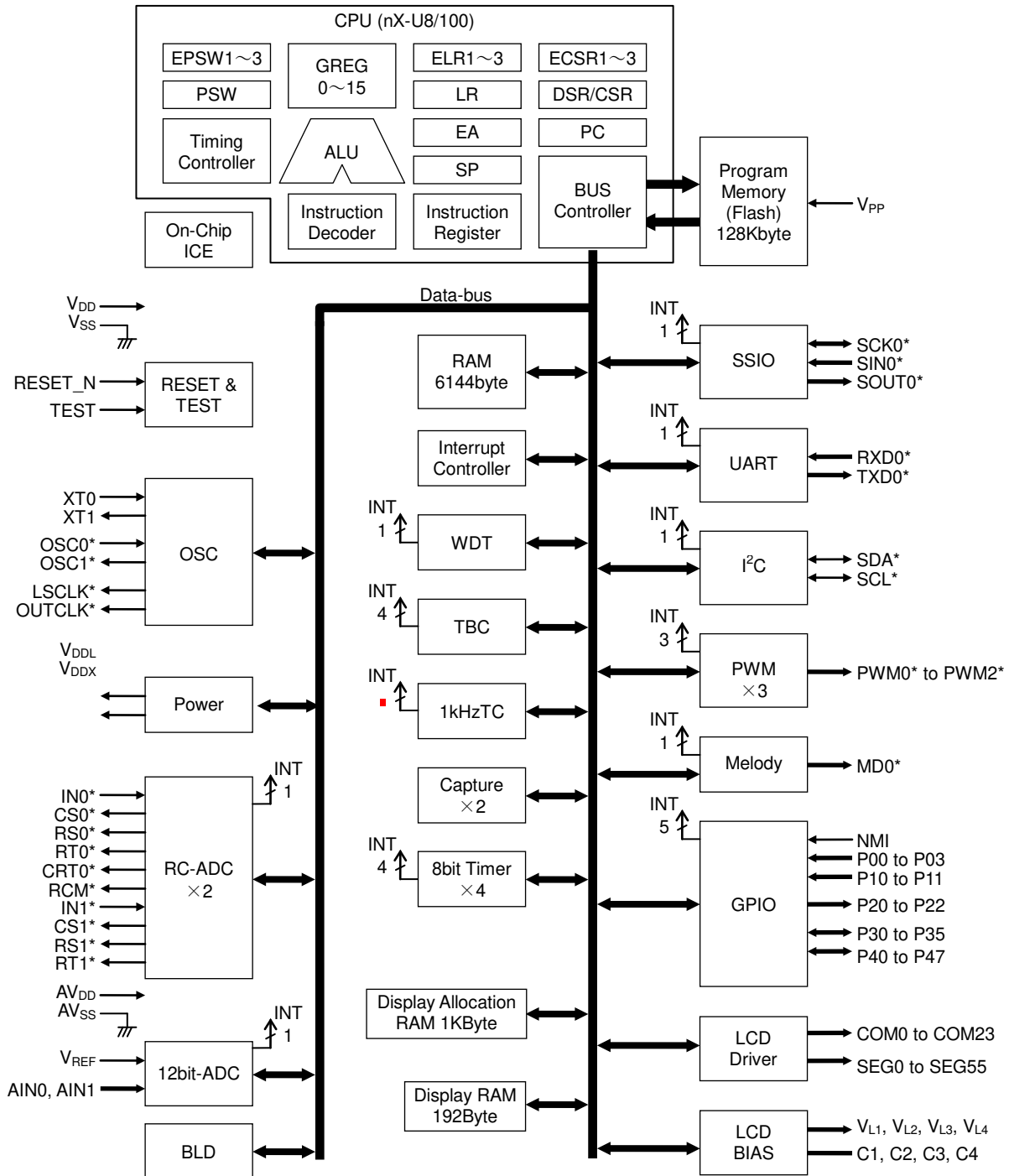


Figure 1-1 Block Diagram of ML610Q438

1.2.2 Block Diagram of ML610Q439

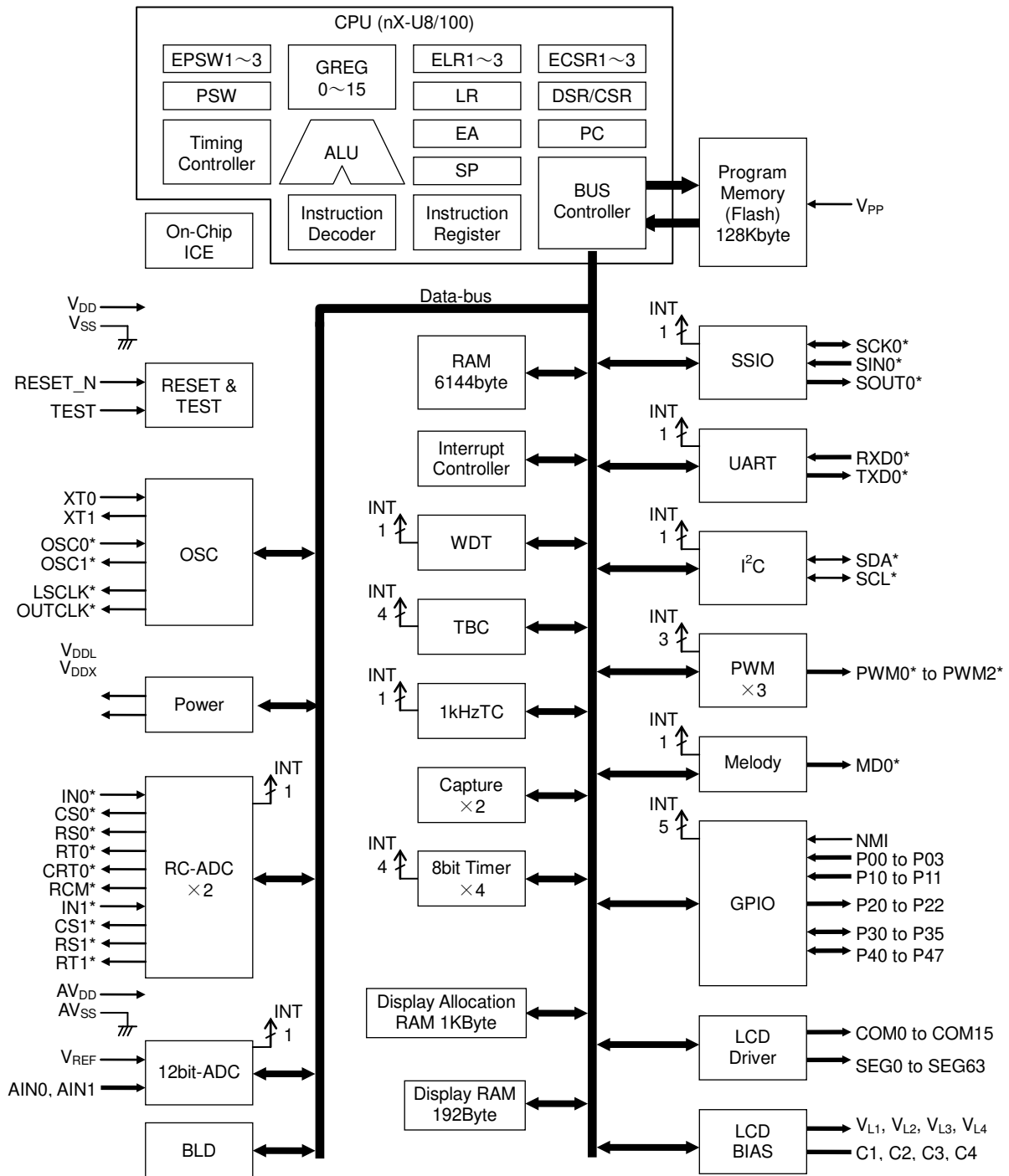
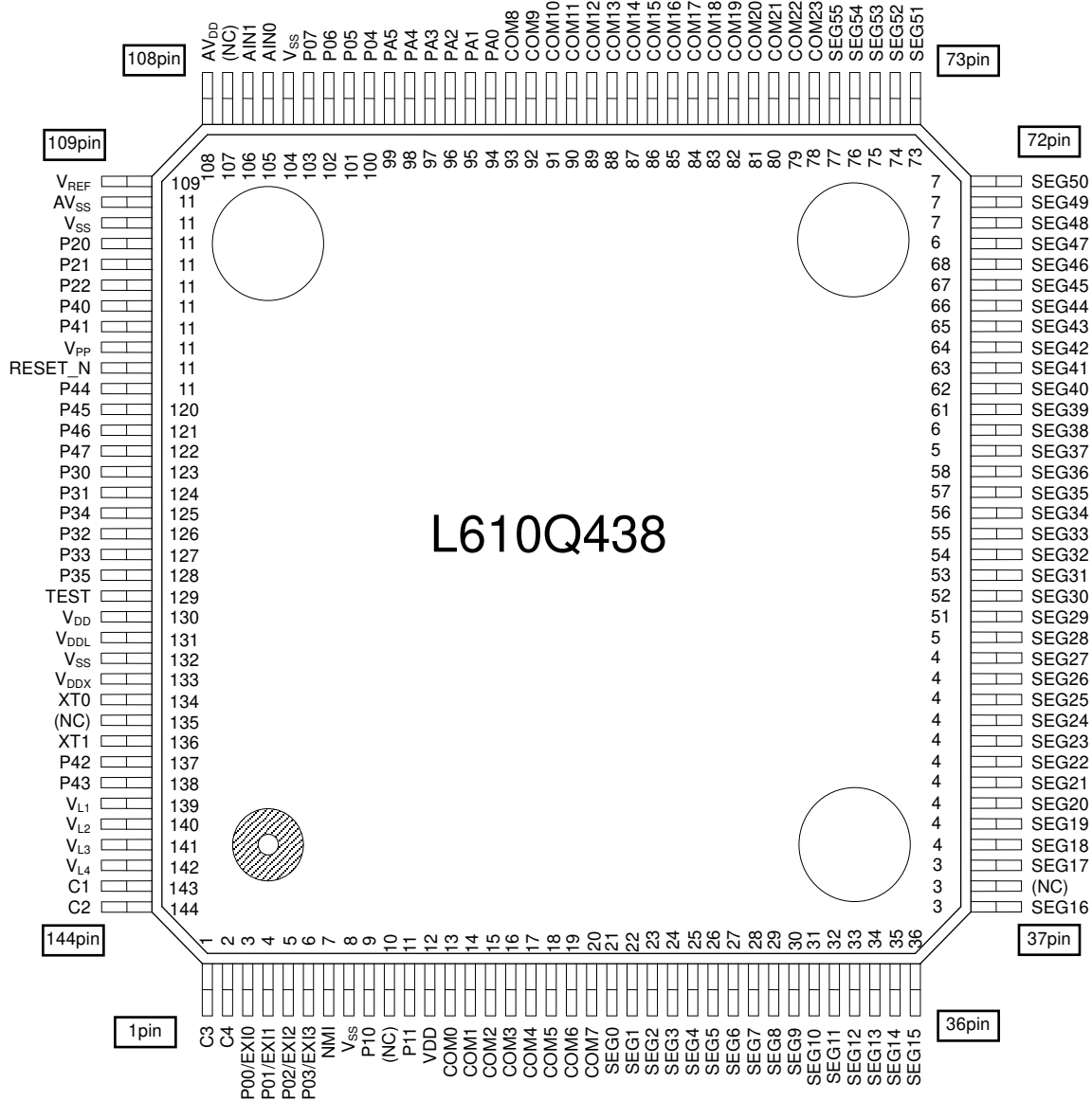


Figure 1-2 Block Diagram of ML610Q439

1.3 Pins

1.3.1 Pin Layout

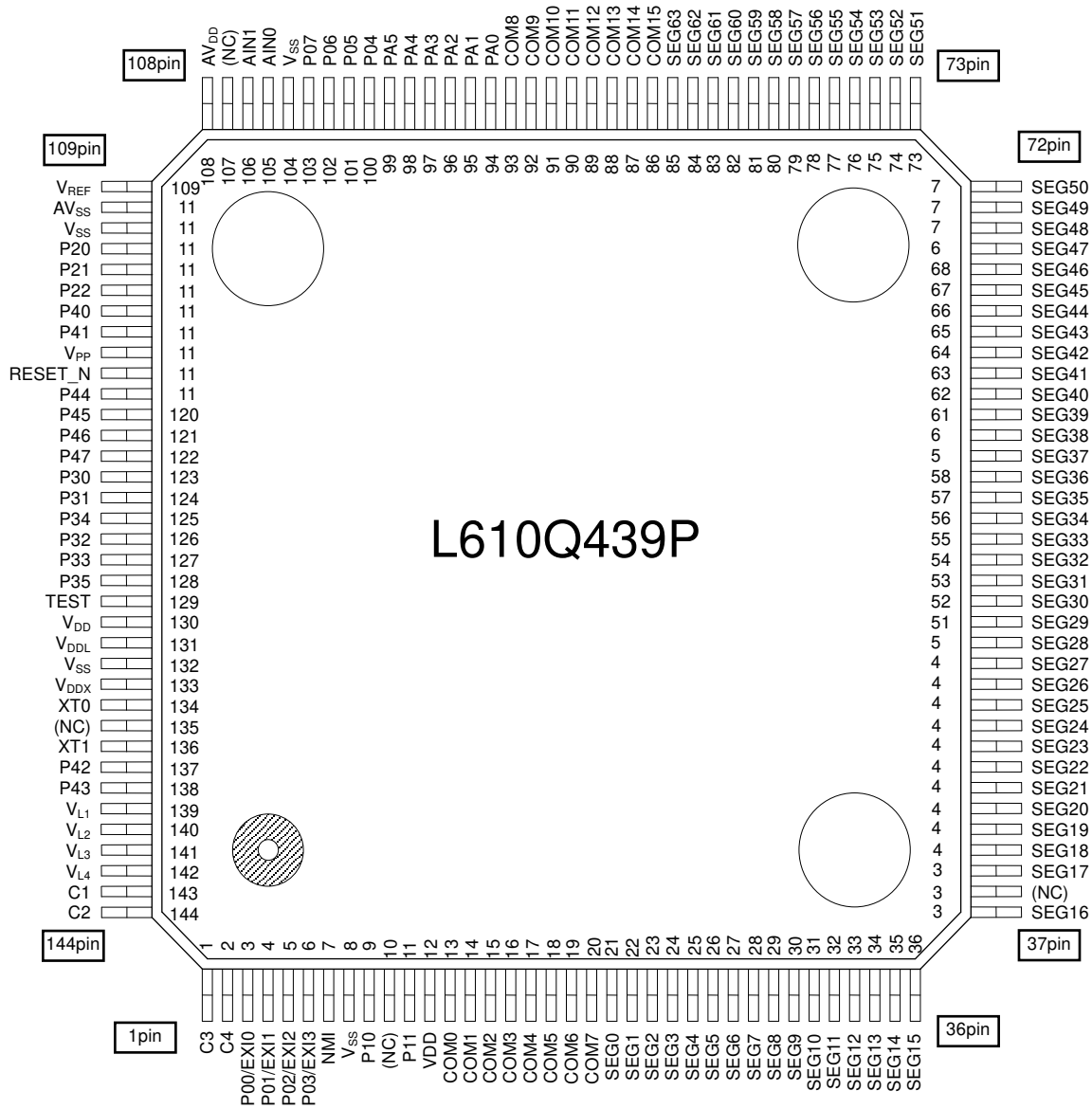
1.3.1.1 Pin Layout of ML610Q438 LQFP Package



(NC): No Connection

Figure 1-3 Pin Layout of ML610Q438 Package

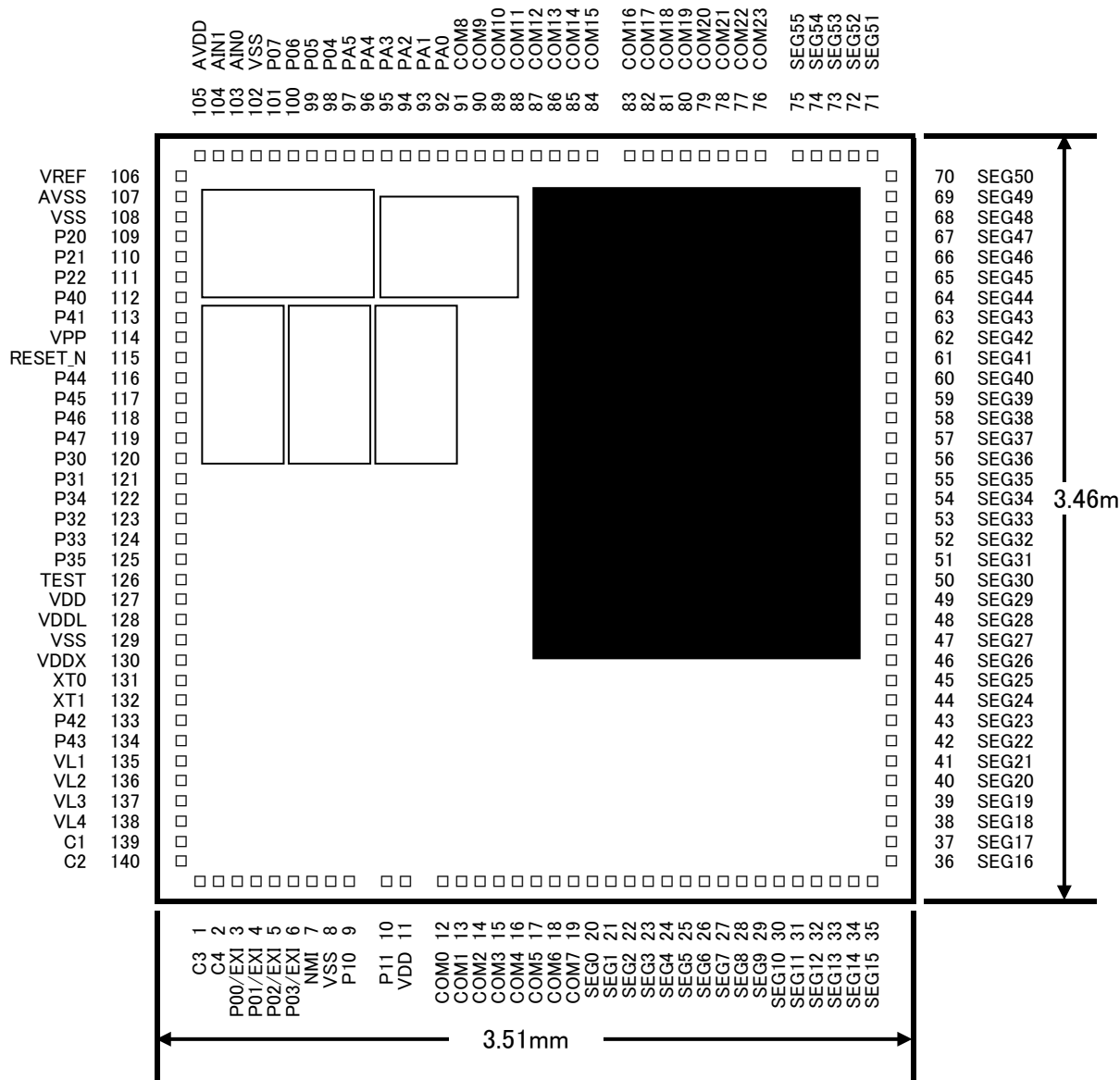
1.3.1.2 Pin Layout of ML610Q439P LQFP Package



(NC): No Connection

Figure 1-4 Pin Layout of ML610Q439P Package

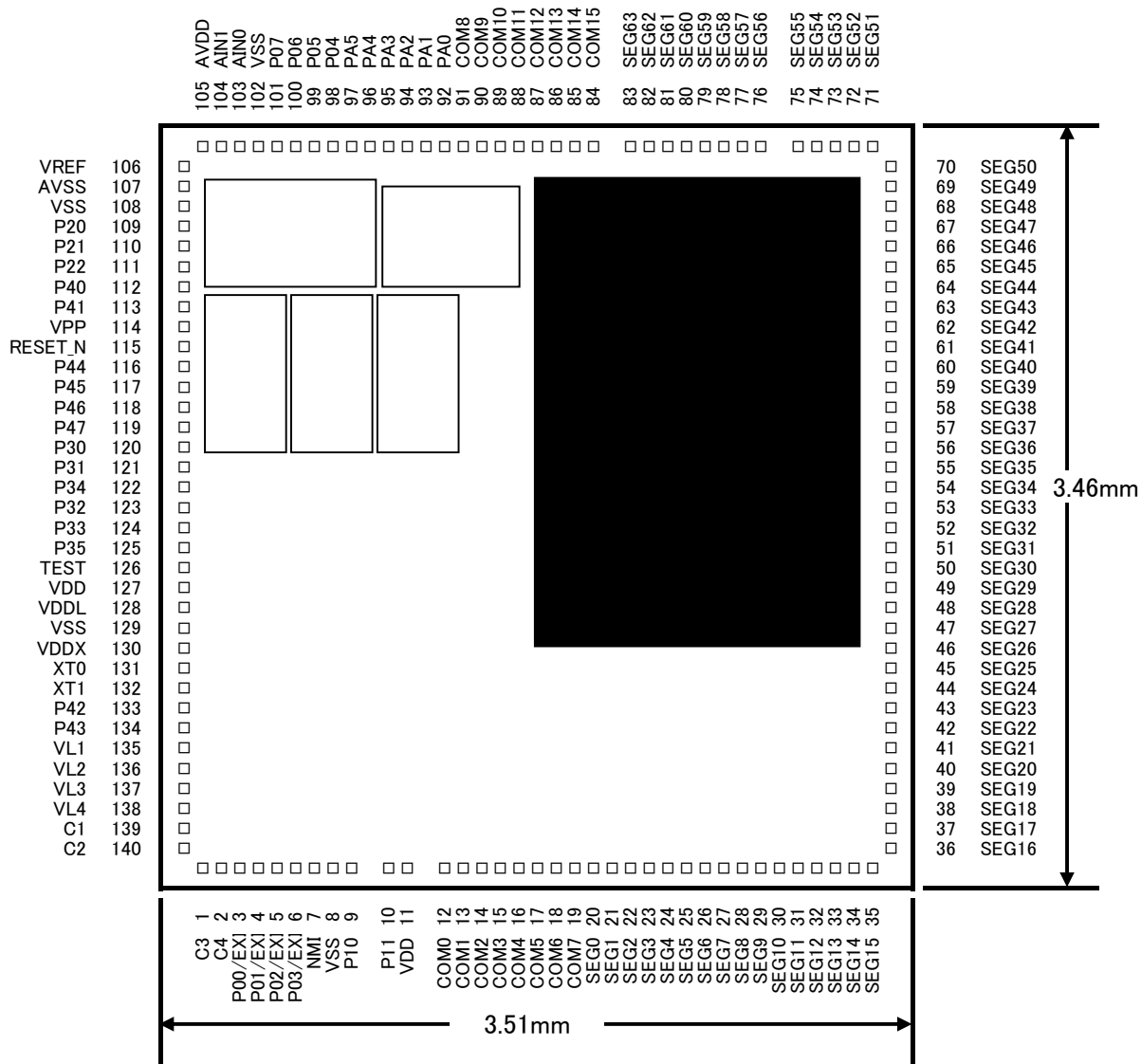
1.3.1.3 Pin Layout of ML610Q438 Chip



Chip size: TBD mm × TBD mm
 PAD count: 138 pins
 Minimum PAD pitch: 80 μm
 PAD aperture: 70 μm × 70 μm
 Chip thickness: 350 μm
 Voltage of the rear side of chip: V_{SS} level

Figure 1-5 Dimensions of ML610Q438 Chip

1.3.1.4 Pin Layout of ML610Q439 Chip



Chip size: TBD mm × TBD mm
 PAD count: 138 pins
 Minimum PAD pitch: 80 μm
 PAD aperture: 70 μm × 70 μm
 Chip thickness: 350 μm
 Voltage of the rear side of chip: V_{SS} level

Figure 1-6 Dimensions of ML610Q439 Chip