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LAPIS SEMICONDUCTOR

FEUL610Q482P-01

ML610Q482P/ML610482P
User's Manual

Issue Date: Jun.20, 2011

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q482.

The following manuals are also available. Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual for ML610Q482
Description about the connection between uEASE and ML610Q482.

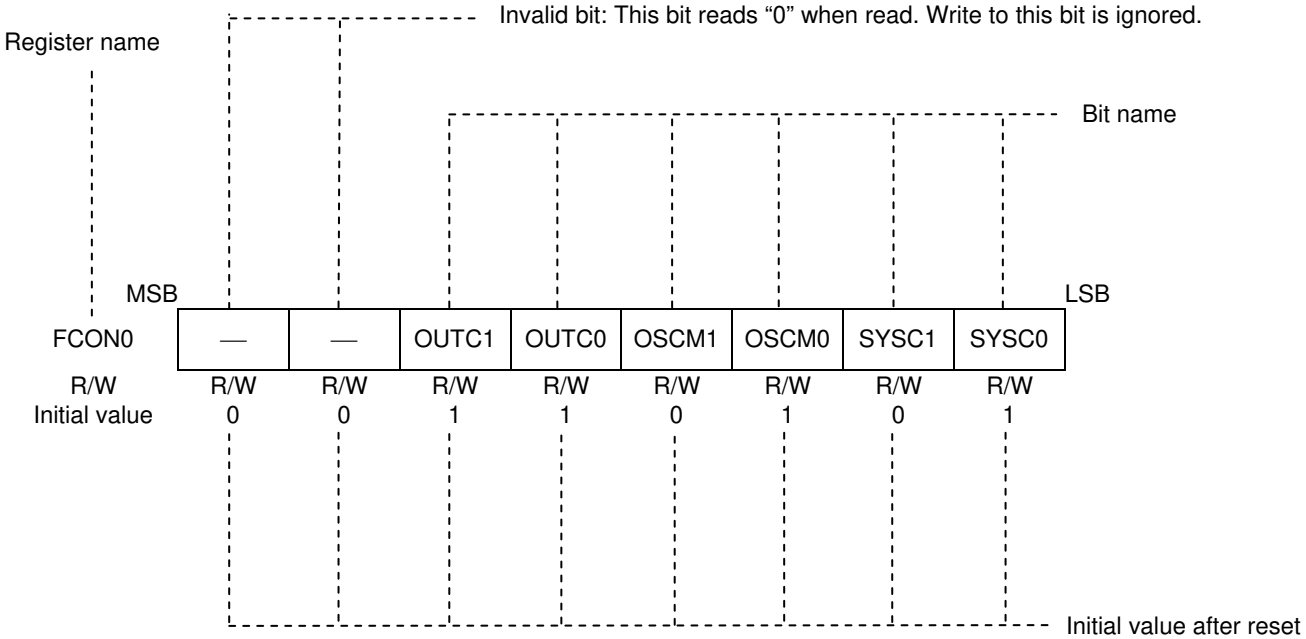
■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1. Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), buzzer driver, battery level detect circuit and RC oscillation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel procesing. The Flash ROM that is installed as program memory achieves to ML610Q482P low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function (ML610Q482P only)
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.24 4μs (@4.096 MHz system clock)

- Internal memory
  - ML610Q482P
    Internal 64KByte Flash ROM (32K×16 bits) (including unusable 1KByte TEST area)
  - ML610482P
    Internal 64KByte Mask ROM (32K×16 bits) (including unusable 1KByte TEST area)
  - Internal 4KByte Data RAM (4096×8 bits)

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 18 maskable interrupt sources (Internal sources: 14, External sources: 4)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)

- Buzzer driver
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Analog comparator
  - Operating voltage: V_{DD} = 1.8V to 3.6V
  - Common mode input voltage: 0.2V to VDD-1.0V
  - Input offset voltage: 50mV(Max)
  - Interrupt allow edge selection and sampling selection

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

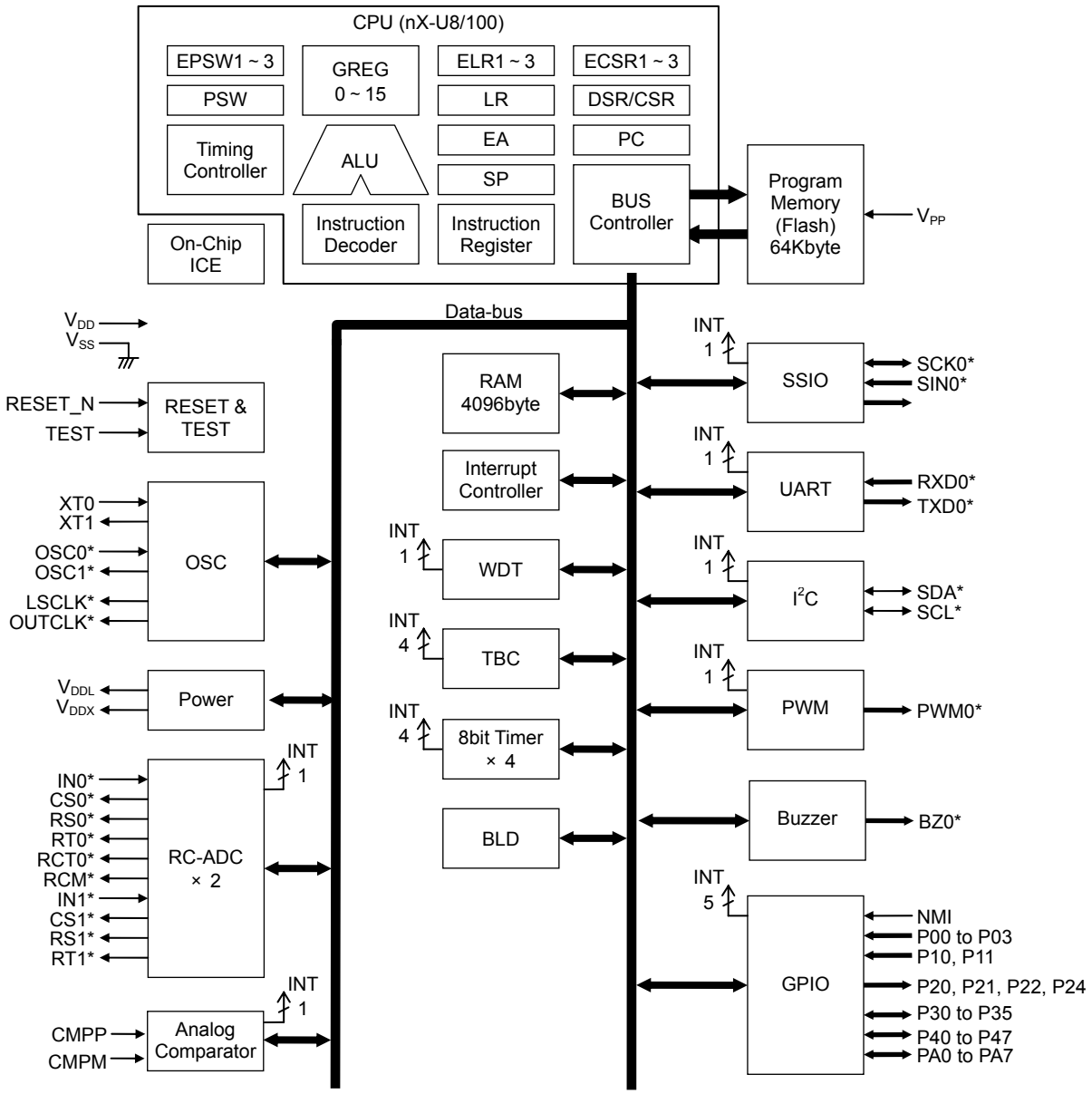
- Shipment
  - Chip (Die)
    Flash ROM version :ML610Q482P-xxxWA (Blank product: ML610Q482P-NNNWA)
    Mask ROM version :ML610482P-xxxWA
    xxx: ROM code number

  - 48-pin plastic TQFP
    Flash ROM version :ML610Q482P-xxxTBZ03A (Blank product: ML610Q482P-NNNTBZ03A)
    Mask ROM version :ML610482P-xxxTBZ03A
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –40°C to 85°C
  - Operating voltage: V_{DD} = 1.1V to 3.6V

1.2 Configuration of Functional Blocks

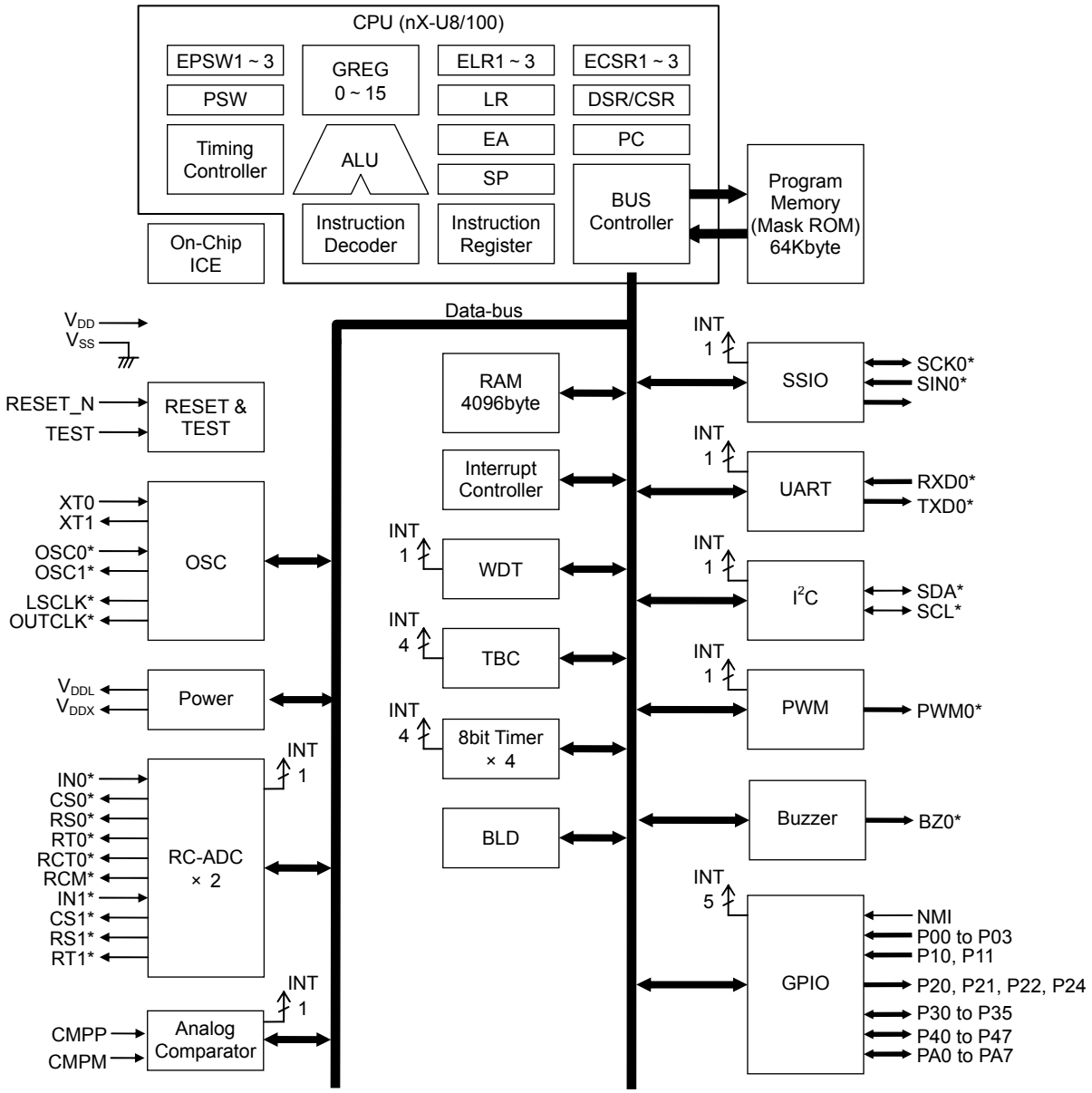
1.2.1 Block Diagram of ML610Q482P



* Secondary function or Tertiary function

Figure 1-1 Block Diagram of ML610Q482P

1.2.2 Block Diagram of ML610482P



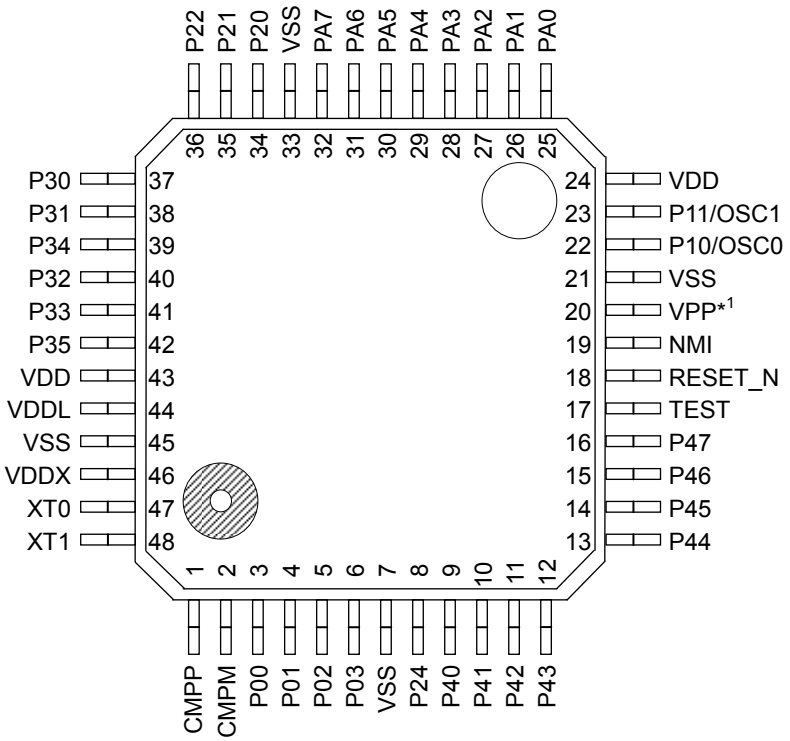
* Secondary function or Tertiary function

Figure 1-2 Block Diagram of ML610482P

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML610Q482P/ML610482P TQFP Package

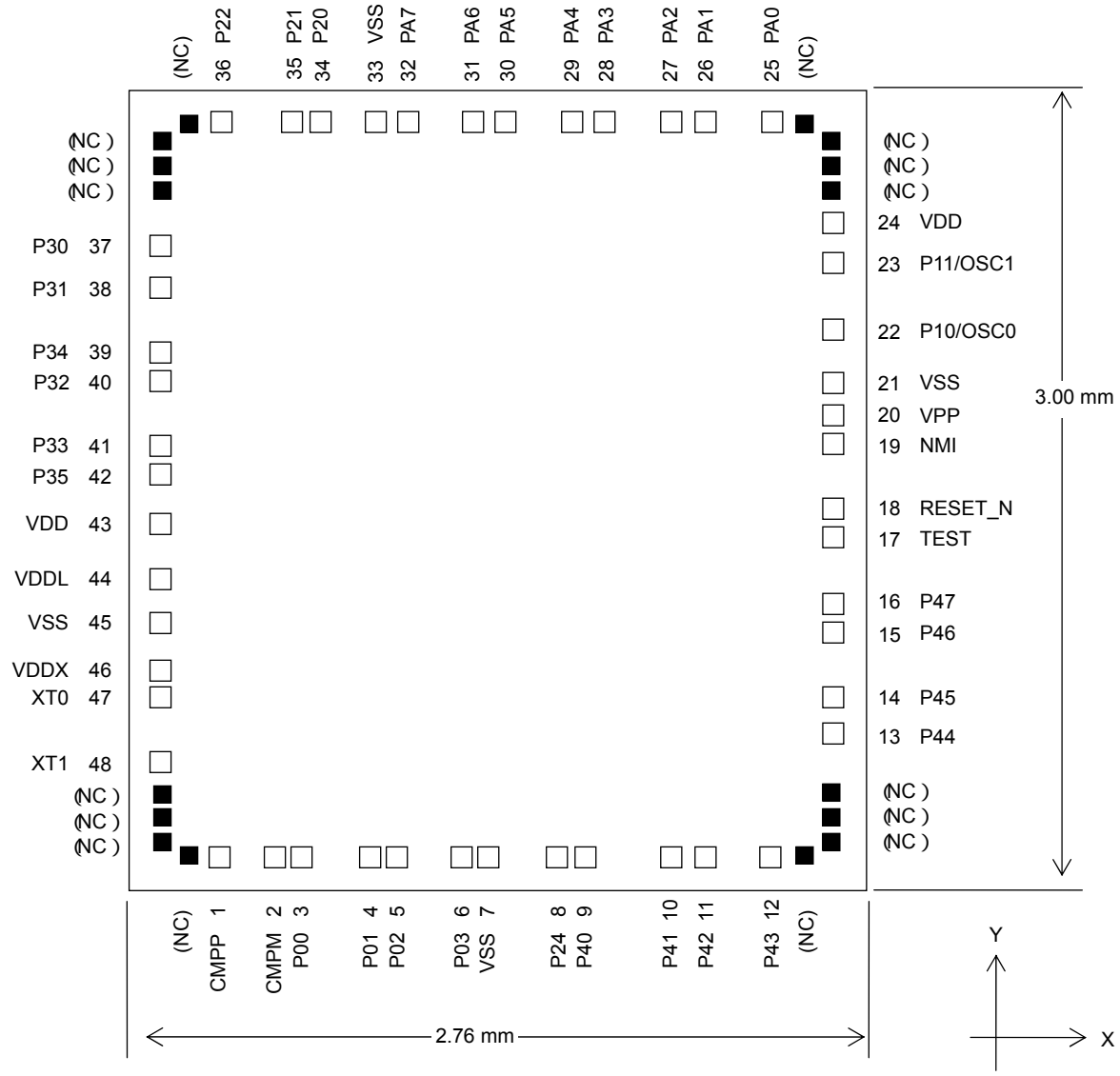


(NC): No Connection

Note:
The assignment of the pads P30 to P35 are not in order.
*1 :A VPP terminal exists only ML610Q482P. Please use (NC) in ML610482P.

Figure 1-3 Pin Layout of ML610Q482P/ML610482P Package

1.3.1.2 Pin Layout of ML610Q482P Chip



(NC): No Connection

Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.76 mm × 3.00mm
PAD count:	48 pins
Minimum PAD pitch:	100 μm
PAD aperture:	80 μm × 80 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-4 Dimensions of ML610Q482P Chip

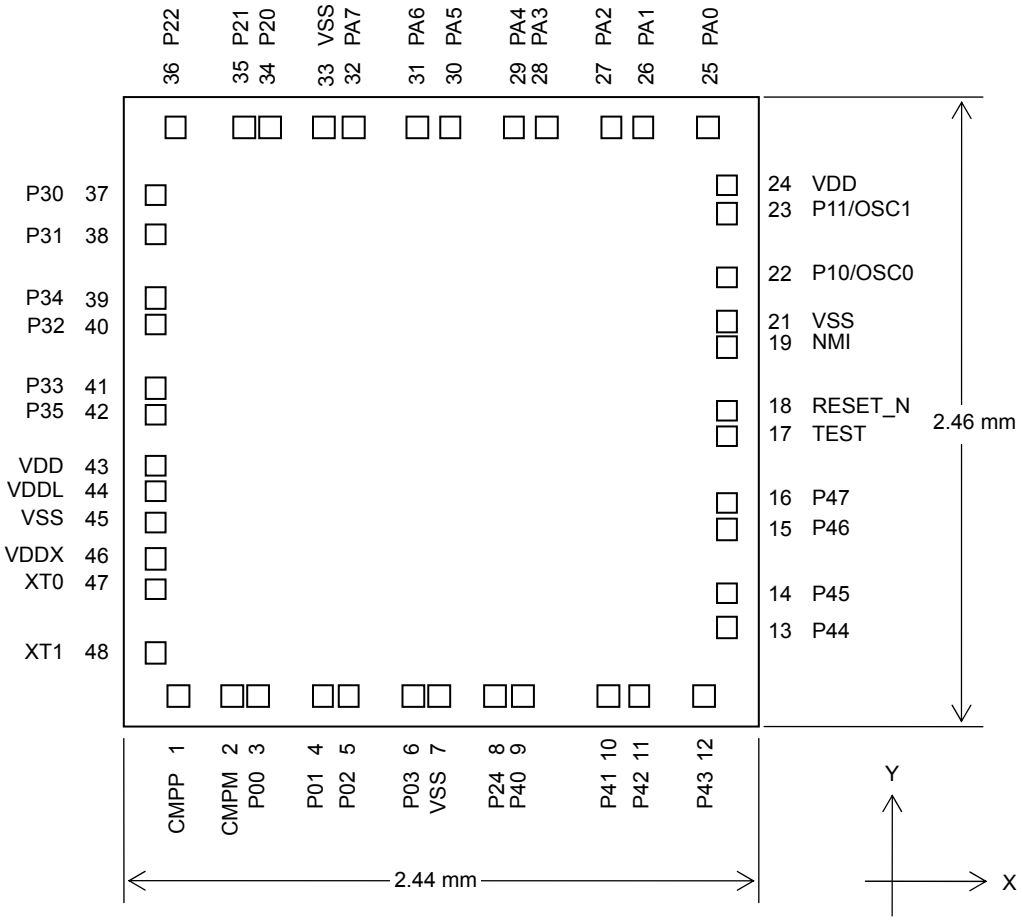
1.3.1.3 Pad Coordinates of ML610Q482P Chip

Table 1-1 Pad Coordinates of ML610Q482P

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	CMPP	-1036.0	-1380.0	25	PA0	1023.0	1380.0
2	CMPM	-830.0	-1380.0	26	PA1	775.0	1380.0
3	P00	-730.0	-1380.0	27	PA2	651.0	1380.0
4	P01	-482.0	-1380.0	28	PA3	403.0	1380.0
5	P02	-382.0	-1380.0	29	PA4	279.0	1380.0
6	P03	-134.0	-1380.0	30	PA5	31.0	1380.0
7	VSS	-34.0	-1380.0	31	PA6	-93.0	1380.0
8	P24	219.0	-1380.0	32	PA7	-341.0	1380.0
9	P40	327.0	-1380.0	33	VSS	-458.0	1380.0
10	P41	655.0	-1380.0	34	P20	-666.0	1380.0
11	P42	775.0	-1380.0	35	P21	-766.0	1380.0
12	P43	1023.0	-1380.0	36	P22	-1032.0	1380.0
13	P44	1260.0	-912.0	37	P30	-1260.0	922.0
14	P45	1260.0	-778.0	38	P31	-1260.0	769.0
15	P46	1260.0	-530.0	39	P34	-1260.0	521.0
16	P47	1260.0	-426.0	40	P32	-1260.0	417.0
17	TEST	1260.0	-167.0	41	P33	-1260.0	169.0
18	RESET_N	1260.0	-67.0	42	P35	-1260.0	67.0
19	NMI	1260.0	181.0	43	VDD	-1260.0	-122.0
20	VPP	1260.0	281.0	44	VDDL	-1260.0	-333.0
21	VSS	1260.0	411.0	45	VSS	-1260.0	-503.0
22	P10	1261.3	610.0	46	VDDX	-1260.0	-673.0
23	P11	1261.3	858.0	47	XT0	-1260.0	-773.0
24	VDD	1260.0	1010.0	48	XT1	-1260.0	-1021.0

1.3.1.4 Pin Layout of ML610482P Chip



Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.44 mm × 2.46mm
PAD count:	48 pins
Minimum PAD pitch:	100 μm
PAD aperture:	80 μm × 80 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 1-5 Dimensions of ML610482P Chip

1.3.1.5 Pad Coordinates of ML610482P Chip

Table 1-2 Pad Coordinates of ML610482P

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	CMPP	-1010	-1110	25	PA0	1025	1110
2	CMPM	-804	-1110	26	PA1	777	1110
3	P00	-704	-1110	27	PA2	653	1110
4	P01	-456	-1110	28	PA3	405	1110
5	P02	-356	-1110	29	PA4	281	1110
6	P03	-108	-1110	30	PA5	33	1110
7	VSS	-8	-1110	31	PA6	-91	1110
8	P24	205	-1110	32	PA7	-339	1110
9	P40	313	-1110	33	VSS	-451	1110
10	P41	641	-1110	34	P20	-659	1110
11	P42	761	-1110	35	P21	-759	1110
12	P43	1009	-1110	36	P22	-1025	1110
13	P44	1100	-842	37	P30	-1100	844
14	P45	1100	-708	38	P31	-1100	691
15	P46	1100	-460	39	P34	-1100	443
16	P47	1100	-356	40	P32	-1100	339
17	TEST	1100	-97	41	P33	-1100	91
18	RESET_N	1100	3	42	P35	-1100	-11
19	NMI	1100	251	43	VDD	-1100	-212
20				44	VDDL	-1100	-312
21	VSS	1100	351	45	VSS	-1100	-434
22	P10	1100	524	46	VDDX	-1100	-574
23	P11	1100	772	47	XT0	-1100	-694
24	VDD	1100	885	48	XT1	-1100	-942

Note: PADNo.20 does not exist.

1.3.2 List of Pins

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
7,21 33,45	Vss	—	Negative power supply pin	—	—	—	—	—	—
24,43	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
44	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
46	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
20	V_{PP} *1	—	Power supply pin for Flash ROM	—	—	—	—	—	—
17	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
18	RESET_N	I	Reset input pin	—	—	—	—	—	—
47	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
48	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
19	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
3	P00/EXI0	I	Input port, External interrupt 0	—	—	—	—	—	—
4	P01/EXI1	I	Input port, External interrupt 1	—	—	—	—	—	—
5	P02/EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
6	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
1	CMPP	—	Comparator input	—	—	—	—	—	—
2	CMPM	—	Comparator input	—	—	—	—	—	—
22	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
23	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
34	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
35	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
36	P22/LED2	O	Output port	BZ0	O	Buzzer output	—	—	—
8	P24/LED4	O	Output port	PWM0	O	PWM0 output	—	—	—
37	P30	I/O	Input/Output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
38	P31	I/O	Input/Output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
40	P32	I/O	Input/Output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
41	P33	I/O	Input/Output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—