Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ML9271

48-Bit Grid/Anode VFD Driver

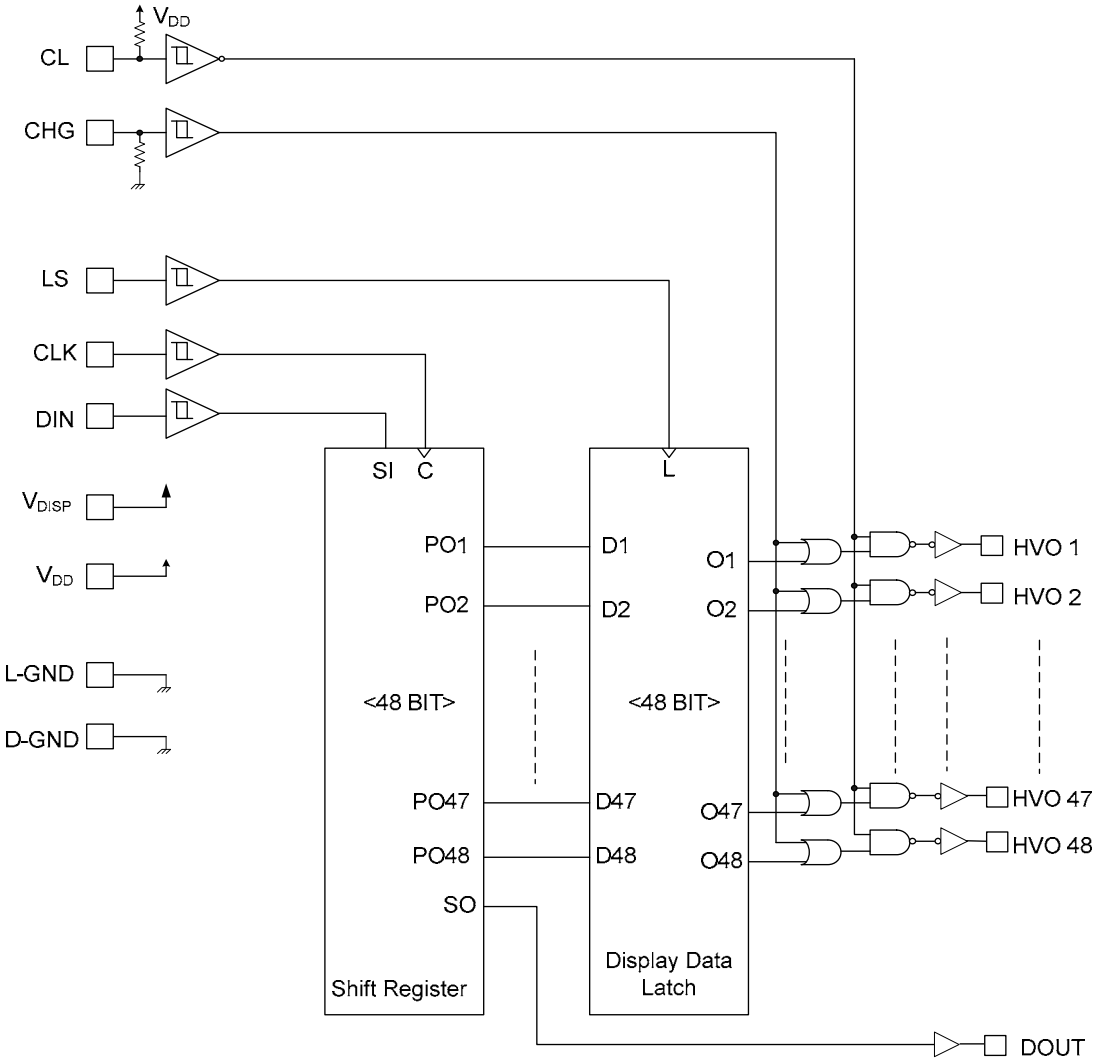
GENERAL DESCRIPTION

The ML9271 is a monolithic IC designed for directly driving the anodes of the vacuum fluorescent display tube. The circuit contains a 48-bit shift register circuit, 48-bit latch circuit, and 48 output circuits on a single chip. Display data is serially stored in the shift register at the rising edge of CLOCK pulse.
Setting the CL pin high allows all the driver outputs to be driven low, which makes it possible to set the display clear.
Setting the CHG pin high with the CL pin set low allows all the driver outputs to be driven high for testing.

FEATURES

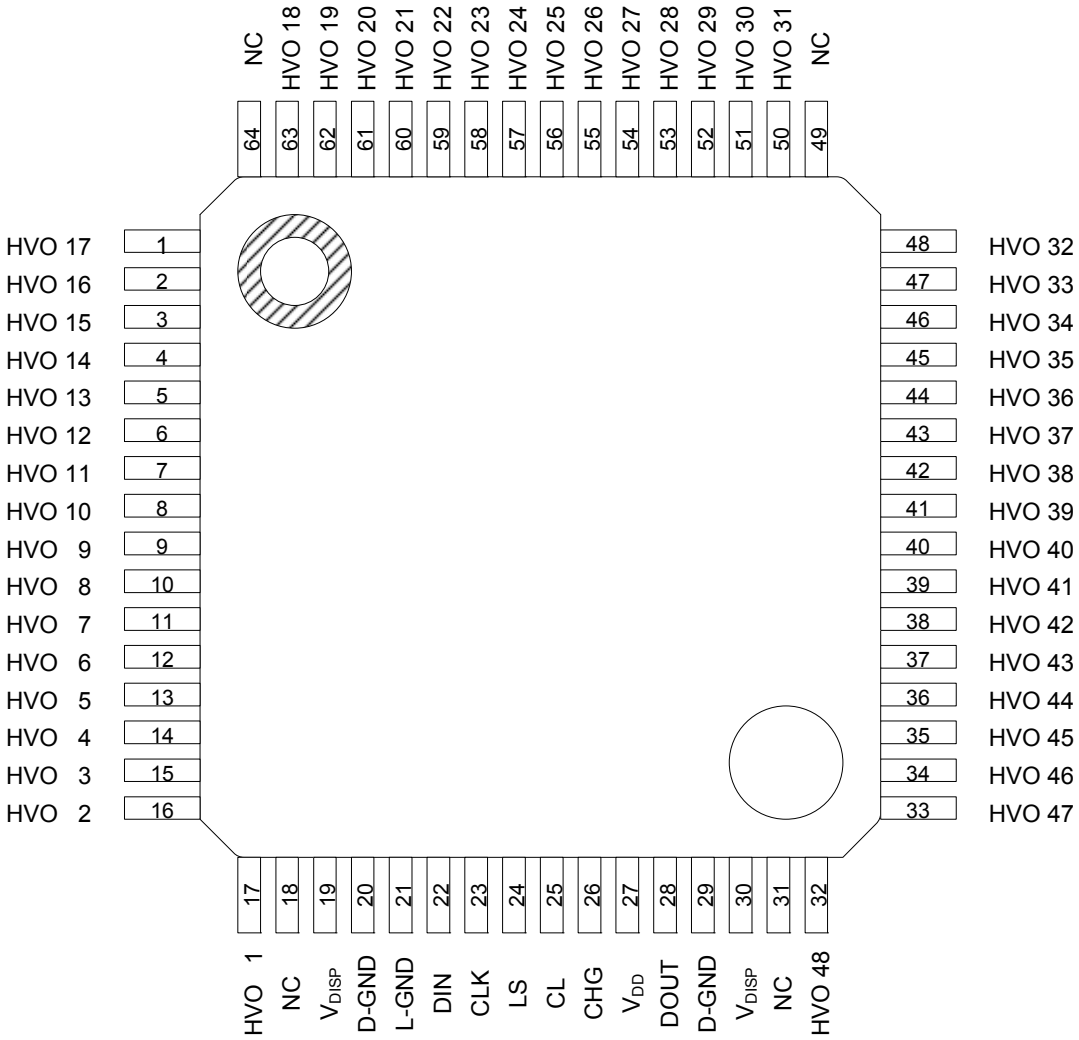
- Logic power supply (V_{DD}) : 3.3V±10% or 5.0 V±10%
- VFD tube drive power supply (V_{DISP}) : 8 to 18 V
- Operating temperature range : −40 to +105°C
- VFD driver outputs can be connected directly to the VFD tube. No pull-down resistor is required.
- VFD driver output current (HVO1 to HVO48) : −6.0 mA
- Clock frequency : 5.0MHz
- Package : 64-pin plastic QFP (QFP64-P-1414-0.80-BK)
  : Al-Pad Chip

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

64-Pin Plastic QFP



NC: No-Connection pin

PIN DESCRIPTION

Pin	Symbol	Type	Function	Description
1 to 17, 32 to 48, 50 to 63	HVO1 to HVO48	O	Driver Outputs	Driver output pins, which correspond to individual bits of the shift register.
19,30	V_{DISP}	—	Driver Power Supply	Power supply pins for driver circuit. Both pin 19 and pin 30 should be connected externally.
27	V_{DD}	—	Logic Power Supply	Power supply pin for logic.
20,29	D-GND	—	Driver GND	GND pins for the driver circuits. Both pin 20 and pin 29 should be connected externally.
21	L-GND	—	Logic GND	GND pin for the logic circuit.
22	DIN	I	Data Input	Input pin without pull-up or pull-down resistor. The input pin to the shift register. Inputs to display data are synchronized with the clock signal. (positive logic)
23	CLK	I	Clock Input	Input pin without pull-up or pull-down resistor. Data of the shift register is shifted from one stage to the next on each rising edge of the clock pulses.
24	LS	I	Latch Strobe Input	Input pin without pull-up or pull-down resistor. When LS is high, the latch is shunted and the shift register outputs become latched. The latch holds the outputs from the shift register just before LS goes from low to high.
25	CL	I	Clear Input	Clear input pin with a pull-up resistor. This pin is normally low. On this condition, driver output changes to high or low according to the latch output level. When CL is high, all driver output pins are fixed to low.
26	CHG	I	Test Input	Test input pin with a pull-down resistor. This pin is normally low. When CL is high, all driver output pins are fixed to low irrespective of CHG. When CL is low and CHG is low, the driver outputs change to high or low according to the latch output level. When CHG is high and CL is low, all driver outputs are high for testing.
28	DOUT	O	Data Output	Serial output pin from the shift register.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage *1	V_{DD}	—	–0.3 to 6.5	V
Driver Supply Voltage *1, *2	V_{DISP}	—	–0.3 to 25	V
Input Voltage *1	V_{IN}	Applicable to all input pins	–0.3 to V_{DD}+0.3	V
Data Output Voltage *1	V_{O1}	Applicable to the data output pins	–0.3 to V_{DD}+0.3	V
Driver Output Voltage *1	V_{O2}	Applicable to the driver output pins	–0.3 to V_{DISP}+0.3	V
Storage Temperature	T_{STG}	—	–55 to 150	°C
Power Dissipation	P_D	Ta < 105°C 64-pin plastic QFP	339	mW
Thermal Resistance *3	R_{j-a}	—	59	°C/W
Output Current	I_{O1}	HVO1 to HVO48	–18.0 to 2.0	mA
	I_{O2}	DOUT	–2.0 to 2.0	

*1 Maximum supply voltage with respect to L-GND and D-GND

*2 Catastrophic breakdown may occur if the applied voltage exceeds the rating value.

*3 Thermal resistance of the package (between junction and atmosphere)

The junction temperature (Tj) given by the following formula should not exceed 150°C.

$$T_j = P \times R_{j-a} + T_a \quad (P \text{ is the maximum power dissipation})$$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	When the logic supply voltage is 3.3 V (typ.)	3.0	3.3	3.6	V
		When the logic supply voltage is 5.0 V (typ.)	4.5	5.0	5.5	V
Driver Supply Voltage	V_{DISP}	Applicable to the driver supply voltage pin	8	—	18	V
CLK Frequency	f_{CLK}	See the Timing Diagram	—	—	5.0	MHZ
Operating Temperature	T_a	64-pin plastic QFP	–40	—	105	°C
	T_j	Al-Pad Chip	–40	—	115	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5.0 V±10% or V_{DD} = 3.3 V±10%, V_{DISP} = 8 to 18 V, Ta = –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	All inputs	V_{DD} = 5.0V±10%		0.7 V_{DD}	—	—	V
			V_{DD} = 3.3V±10%		0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All inputs	V_{DD} = 5.0V±10%		—	—	0.3 V_{DD}	V
			V_{DD} = 3.3V±10%		—	—	0.2 V_{DD}	V
High Level Input Current	I_{IH1}	V_I = V_{DD}	CHG pin	V_{DD} = 5.0V	100	—	600	µA
				V_{DD} = 3.3V	50	—	300	µA
	I_{IH2}		Other input pins		–1	—	1	µA
Low Level Input Current	I_{IL1}	V_I = 0 V	CL pin	V_{DD} = 5.0V	–600	—	–100	µA
				V_{DD} = 3.3V	–300	—	–50	µA
	I_{IL2}		Other input pins		–1	—	1	µA
High Level Driver Output Voltage	V_{OH1}	HVO1 to HVO48	I_{OH1} = –6.0mA V_{DISP}= 9.5v		V_{DISP}–1.0	—	—	V
	V_{OH2}	DOUT	I_{OH2} = –0.1mA		V_{DD}–1.0	—	—	V
Low Level Driver Output Voltage	V_{OL1}	HVO1 to HVO48	I_{OL1} = 0.2mA		—	—	1.0	V
	V_{OL2}	DOUT	I_{OL2} = 0.1mA		—	—	1.0	V
Supply Current (1) (Dynamic Mode)	I_{DD}	V_{DD}	V_{DD} = 5.0V±10% Input Data =”1” “0” “1”…		—	—	2.5	mA
			V_{DD} = 3.3V ±10% Input Data =”1” “0” “1”…		—	—	2.0	mA
	I_{DISP}	V_{DISP}	Input Data =”1” “0” “1”…		—	—	0.5	mA
Supply Current (2) (Static Mode)	I_{DDS}	V_{DD}	No Operation, Typ.: Ta = 25°C Max.: Ta = 85°C		—	1.0	10.0	µA
	I_{DISPS}	V_{DISP}			—	1.0	20.0	µA
Voltage Difference Between GND Pins	V_{GND}	Voltage difference between D-GND and L-GND *1			–0.1	0	0.1	V

*1 The D-GND and L-GND pins are not connected internally. Therefore, set the voltage between D-GND and L-GND at the same voltage level by connecting these pins externally.

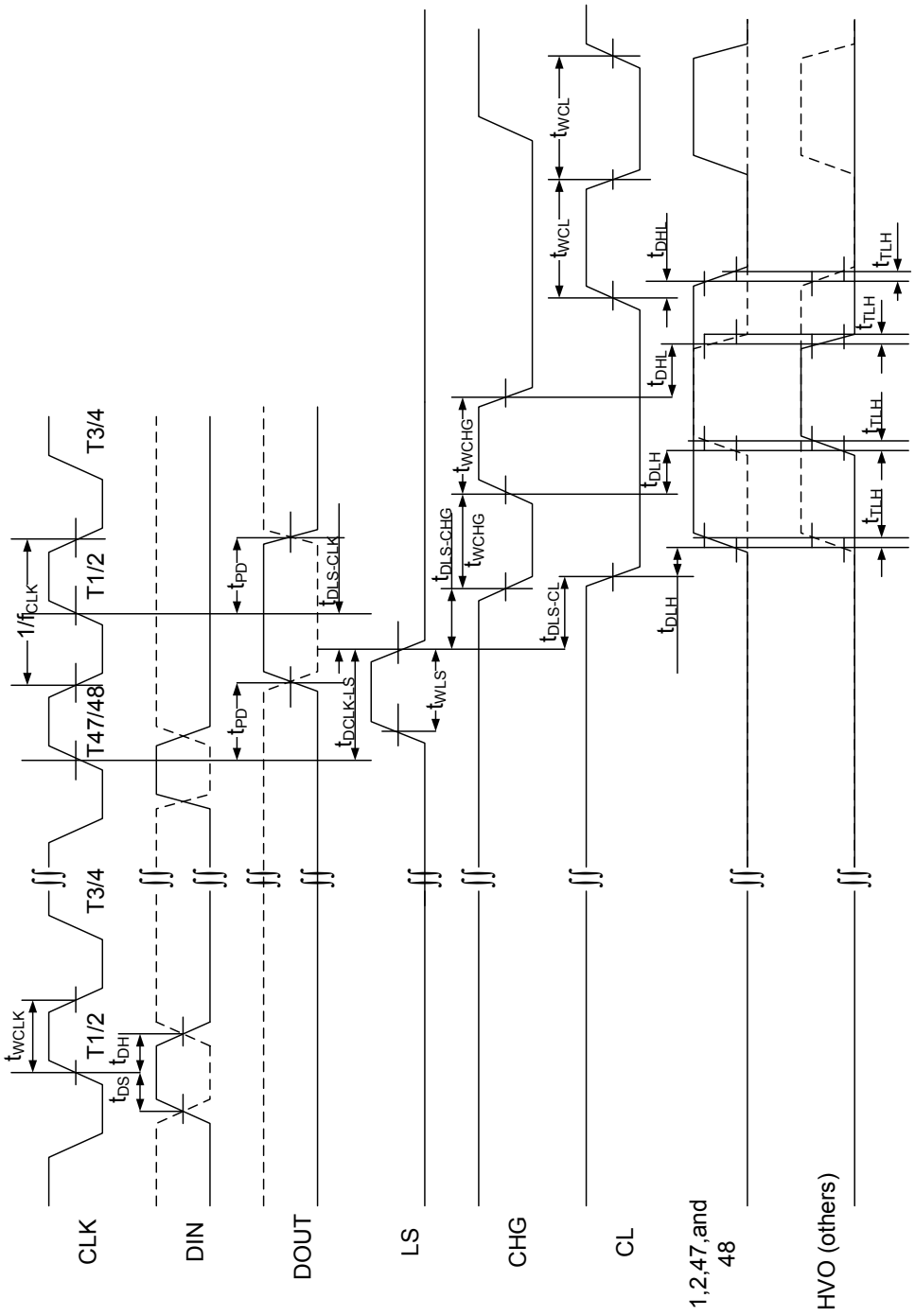
AC Characteristics

(V_{DD} = 5.0 V±10% or V_{DD} = 3.3 V±10%, V_{DISP} = 8 to 18 V, Ta = –40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK Pulse Width	t_{WCLK}	—	100	—	—	ns
Data Setup Time	t_{DS}	—	50	—	—	ns
Data Hold Time	t_{DH}	—	50	—	—	ns
LS Pulse Width	t_{WLS}	—	50	—	—	ns
CHG Pulse Width	t_{WCHG}	—	5	—	—	µs
CL Pulse Width	t_{WCL}	—	5	—	—	µs
CLK-LS Delay Time	$t_{DCLK-LS}$	—	50	—	—	ns
LS-CLK Delay Time	$t_{DLS-CLK}$	—	50	—	—	ns
LS-CHG Delay Time	$t_{DLS-CHG}$	—	0	—	—	ns
LS-CL Delay Time	t_{DLS-CL}	—	0	—	—	ns
CLK-DOUT Delay time	t_{PD}	C_{ll} = 30 pF	—	25	50	ns
All Output Delay Time	t_{DLH}	C_{ld} = 100 pF t_R = 20 to 80% t_F = 80 to 20%	—	1.0	2.0	µs
	t_{DHL}		—	1.0	2.0	µs
All Output Slew Rate	t_{TLH}	C_{ld} = 100 pF t_R = 20 to 80% t_F = 80 to 20%	—	0.5	1.0	µs
	t_{THL}		—	0.5	1.0	µs

TIMING DIAGRAMS

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH} / V_{IL}	0.8 V_{DD} / 0.2 V_{DD}	0.7 V_{DD} / 0.3 V_{DD}
V_{OH} / V_{OL}	0.8 V_{DISP} / 0.2 V_{DISP}	0.8 V_{DISP} / 0.2 V_{DISP}
	0.8 V_{DD} / 0.2 V_{DD}	0.8 V_{DD} / 0.2 V_{DD}



FUNCTIONAL DESCRIPTION

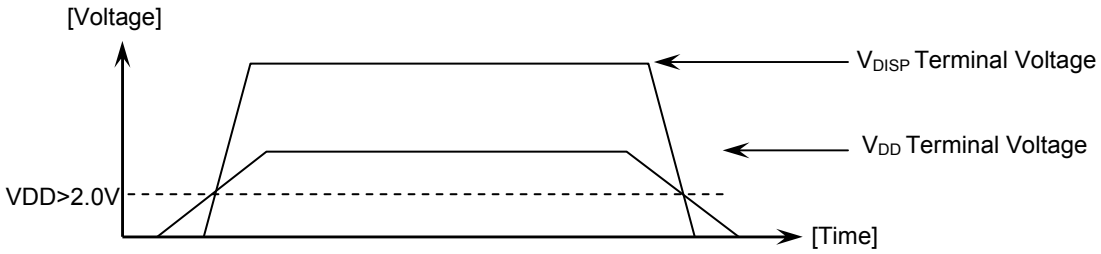
Funtion Table

CLOCK	DIN	PO1 PO2 PO3 PO4 ……PO46 PO47 PO48 DOUT
↗	H	H PO1k PO2k PO3k PO45k PO46k PO47k PO47k
↗	L	L PO1k PO2k PO3k.....PO45k PO46k PO47k PO47k

CL	CHG	LS	POn	HVOn
H	X	X	X	L
L	H	X	X	H
L	L	H	H	H
L	L	H	L	L
L	L	L	X	NC

L: Low Level, H: High Level, X: Don’t Care, NC: No Change

POWER-ON/OFF TIMING

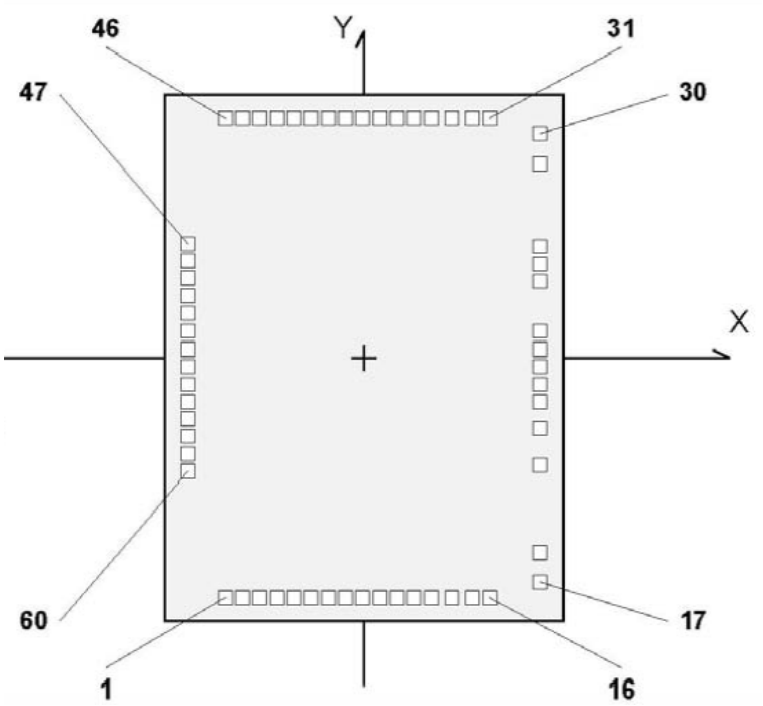


To prevent IC from malfunctioning, V_{DISP} should be applied after V_{DD} is applied.
When the power is turned off, V_{DD} should be applied after V_{DIS}P is applied.

PAD CONFIGURATION

Pad Layout

Chip Size: 2.32×3.00mm
Chip Thickness: 350±30 µm
Pad size Metal 90µm×90µm PV Pad hole 80µm×80µm



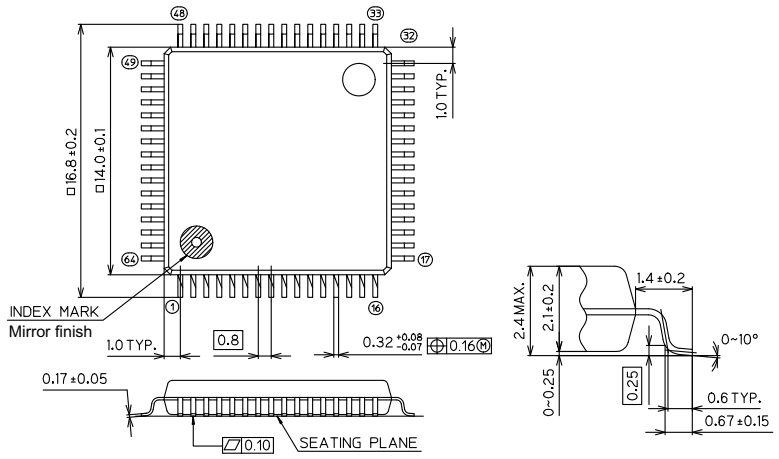
Pad Coordinates

Pad	Symbol	X (μm)	Y (μm)	Pad	Symbol	X (μm)	Y (μm)
1	HVO17	-808	-1365	31	HVO47	732	1365
2	HVO16	-708	-1365	32	HVO46	632	1365
3	HVO15	-608	-1365	33	HVO45	512	1365
4	HVO14	-508	-1365	34	HVO44	392	1365
5	HVO13	-408	-1365	35	HVO43	292	1365
6	HVO12	-308	-1365	36	HVO42	192	1365
7	HVO11	-208	-1365	37	HVO41	92	1365
8	HVO10	-108	-1365	38	HVO40	-8	1365
9	HVO9	-8	-1365	39	HVO39	-108	1365
10	HVO8	92	-1365	40	HVO38	-208	1365
11	HVO7	192	-1365	41	HVO37	-308	1365
12	HVO6	292	-1365	42	HVO36	-408	1365
13	HVO5	392	-1365	43	HVO35	-508	1365
14	HVO4	512	-1365	44	HVO34	-608	1365
15	HVO3	632	-1365	45	HVO33	-708	1365
16	HVO2	732	-1365	46	HVO32	-808	1365
17	HVO1	1025	-1274	47	HVO31	-1025	650
18	VDISP	1025	-1106	48	HVO30	-1025	550
19	D-GND	1025	-612	49	HVO29	-1025	450
20	L-GND	1025	-403	50	HVO28	-1025	350
21	DIN	1025	-250	51	HVO27	-1025	250
22	CLK	1025	-150	52	HVO26	-1025	150
23	LS	1025	-50	53	HVO25	-1025	50
24	CL	1025	50	54	HVO24	-1025	-50
25	CHG	1025	150	55	HVO23	-1025	-150
26	VDD	1025	433	56	HVO22	-1025	-250
27	DOUT	1025	533	57	HVO21	-1025	-350
28	D-GND	1025	633	58	HVO20	-1025	-450
29	VDISP	1025	1106	59	HVO19	-1025	-550
30	HVO48	1025	1274	60	HVO18	-1025	-650

PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9271-01	Dec. 21, 2005	–	–	Preliminary edition 1
FEDL9271-01	Mar. 1, 2007	–	–	Final edition 1

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.