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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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### FEATURES

- **Wideband:** 1.0 to 12 GHz
- **NF:** 1.3 dB @ 2.0 GHz  
1.4 dB @ 6.0 GHz  
1.9 dB @ 12.0 GHz
- **P-1dB:** 16 dBm @ 6.0 GHz
- **OIP3:** 27 dBm @ 6.0 GHz
- **Gain:** 17 dB @ 6.0 GHz
- **Bias Condition:** VDD = 5 V  
IDD = 55 mA
- **50-Ohm On-chip Matching**
- **Unconditionally Stable: 50 MHz to 20 GHz**
- **Gain Control Option Available with 2nd Gate Control Voltage**
- **4x4 mm, 24 Lead Ceramic SMT Package**

### APPLICATIONS

- **Microwave Point-to-Point Radios**
- **Satellite and Telemetry Communications**
- **Test Instrumentation**
- **EW Receiver Systems**
- **Wide-band Communication Systems**
- **Commercial Wireless Systems**

### DESCRIPTION

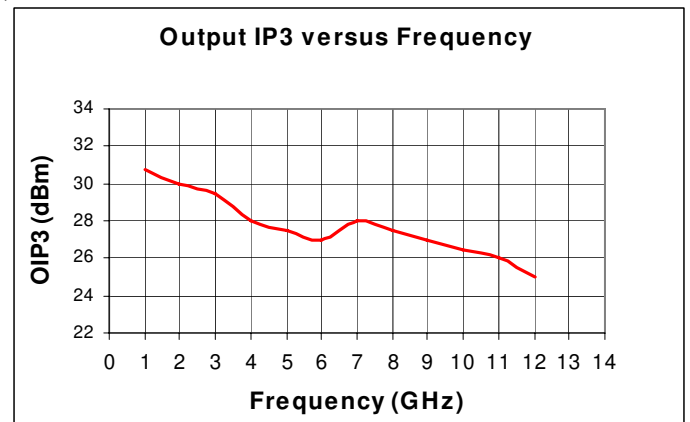
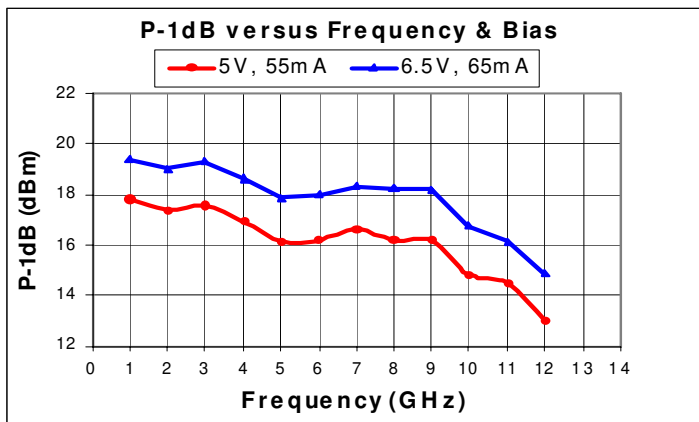
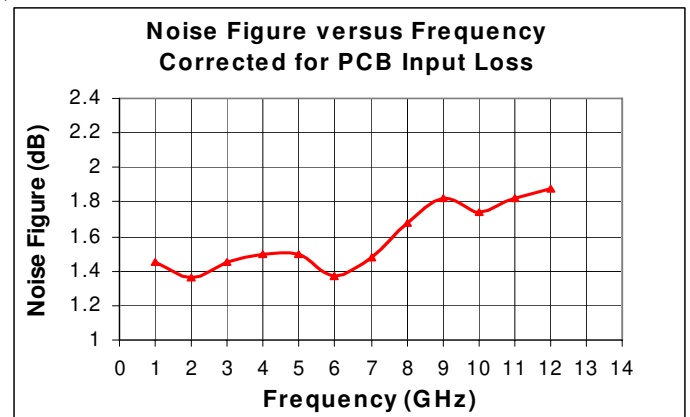
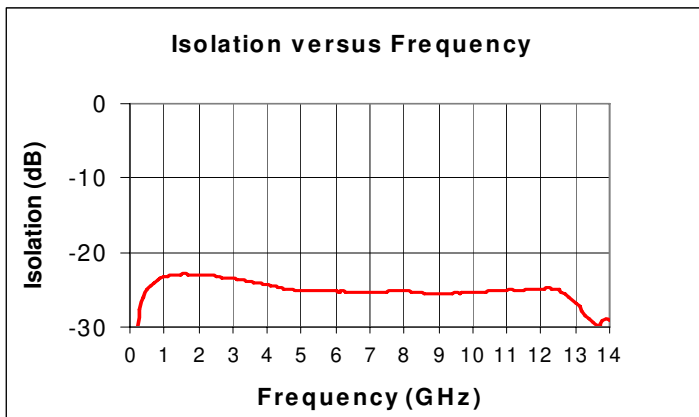
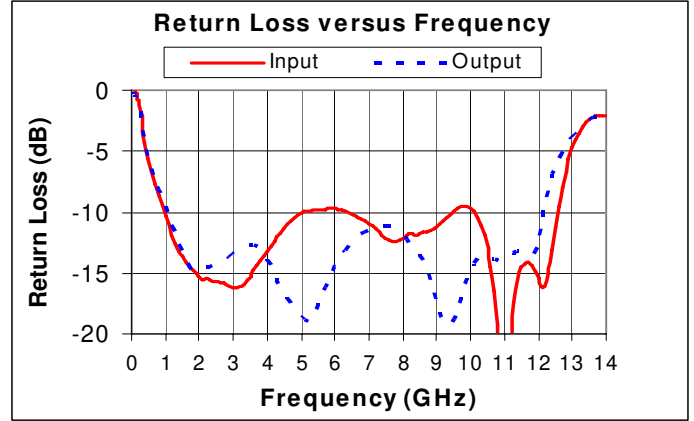
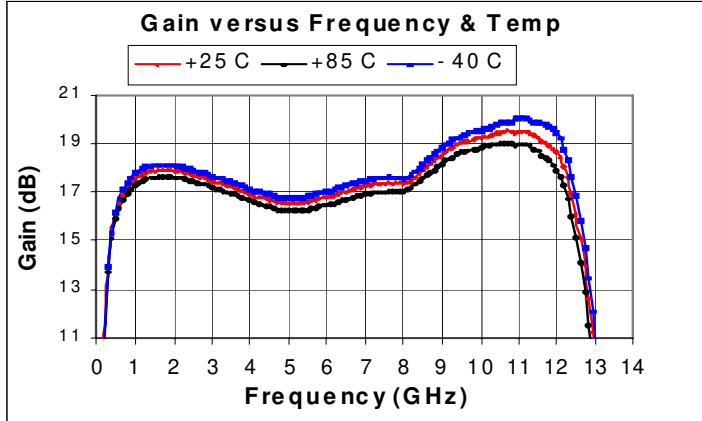
The MLA-01122B-C4 is a packaged fully-matched broadband Low-Noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. This MMIC is suited for Satellite Communications, Microwave radios, Instrumentation, Wideband Systems and also many commercial wireless applications where low-noise figure with high-gain is desirable. It has excellent gain (17 dB) and Noise Figure (1.4 dB, mid-band) over a broad frequency range. Typical P-1dB is 16 dBm and OIP3 is +27dBm @ 6 GHz. It has on-chip bias circuit, choke and DC blocking to provide bias stability and ease of use. The 2<sup>nd</sup> Gate voltage input can be used for gain control if necessary. Available in 4x4mm, 24 Lead Ceramic SMT Package.

### ELECTRICAL SPECIFICATIONS: VDD=+5.0V, VG1=+0.13V, VG2=+2V, IDD=55 mA, Ta=25 C, ZO=50 ohm <sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TYPICAL DATA	UNITS
Frequency Range		1-12	GHz
Gain	1 - 8 GHz	17	dB
	10 - 12 GHz	19	
Gain Flatness	1 - 8 GHz	0.7	+/-dB
	1 - 12 GHz	1.5	
Input Return Loss	2 GHz	15	dB
	5 GHz	9.5	
	10 GHz	13	
Output Return Loss		11	dB
Output P1dB	2 GHz	17.5	dBm
	6 GHz	16.0	
	10 GHz	15.0	
	12 GHz	13.0	
Output IP3 @ 0 dBm/tone, 1 MHz separation	2 GHz	30	dBm
	6 GHz	27	
	12 GHz	25	
Noise Figure	2 GHz	1.3	dB
	6 GHz	1.4	
	12 GHz	1.9	
Operating Bias Conditions: VDD IDD	VG1=+0.13V, VG2=+2V	+5	V
		55	mA
Stability Factor K	0.05 to 20 GHz	> 1	

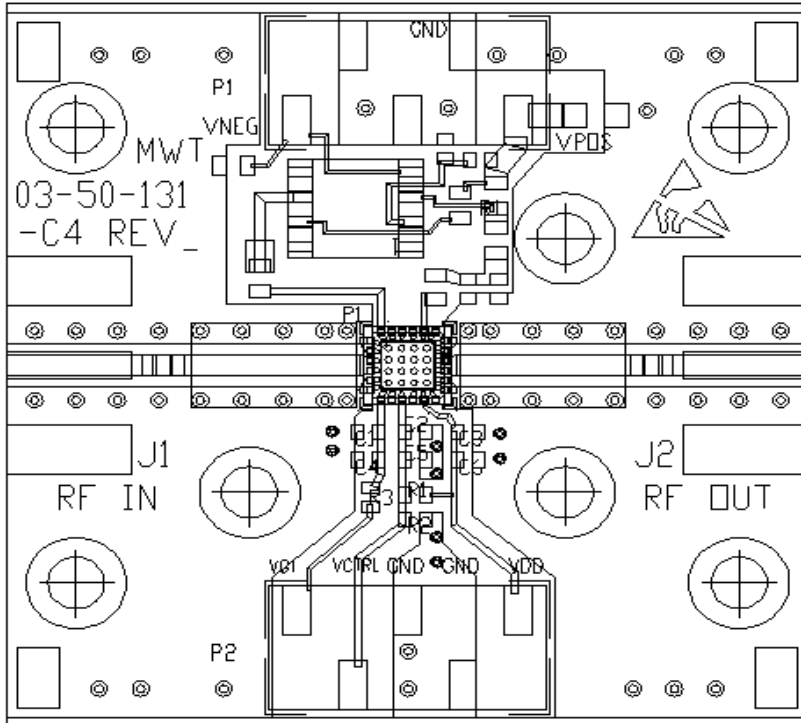
(1) All data is measured on Evaluation Board, with VG2 bias derived from VDD bias using resistive voltage divider as shown in Evaluation Board Schematic & Layout. (2) Vg1 can be slightly positive or negative depending on the lot and operation current.

**TYPICAL RF PERFORMANCE:**  $VDD=+5.0V$ ,  $VG1=+0.13V$ ,  $VG2=+2V$ ,  $IDD=55\text{ mA}$ ,  $Ta=25\text{ C}$ ,  $ZO=50\text{ ohm}$  <sup>(1)</sup>





### EVALUATION BOARD LAYOUT:



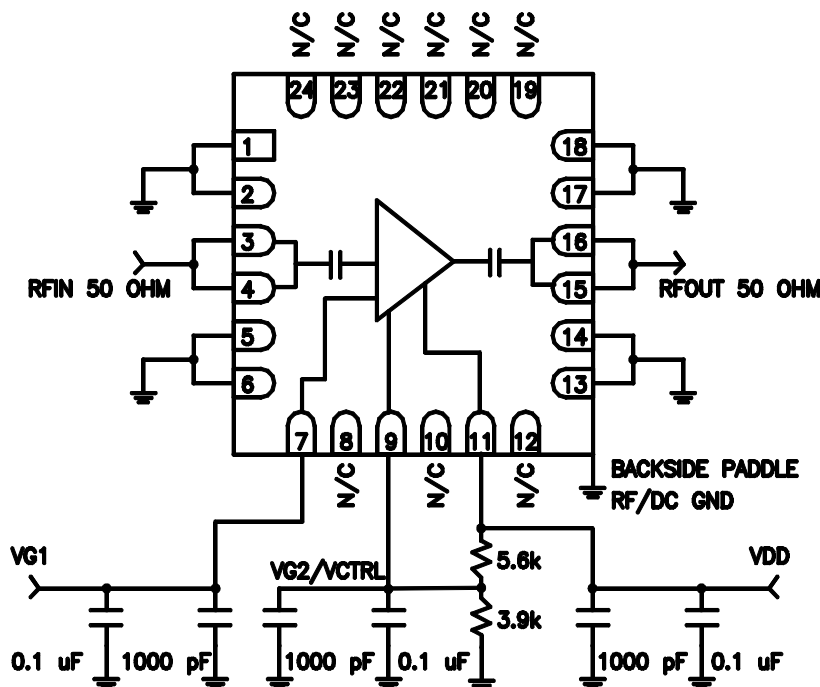
#### Parts List:

C1,C2,C3: 04025C102KAT2A 1000pF AVX  
 C4,C5,C6: 0402ZD104KA T2A 0.1uF AVX  
 R1: RK73B1ETTP562J(0402)5.6k AVX  
 R2: RK73B1ETTP392J(0402)3.9k AVX  
 R3: RK73Z1ETTP(0402)0 Ohms AVX  
 P2: TSM-105-01-S-SV SAMTEC  
 J1,J2: 142-0701-841 JOHNSON  
 PCB: 20 mil thick 2-Layer R04003  
 Vias are plated & filled with Cu  
 paste & planarized

#### NOTES:

1) BACKSIDE OF PACKAGE IS RF/DC GND AND MUST BE GROUNDED WITH ENOUGH VIAS AS SHOWN TO PCB RF/DC GND FOR BEST ELECTRICAL AND THERMAL PERFORMANCE

### APPLICATION CIRCUIT SCHEMATIC:

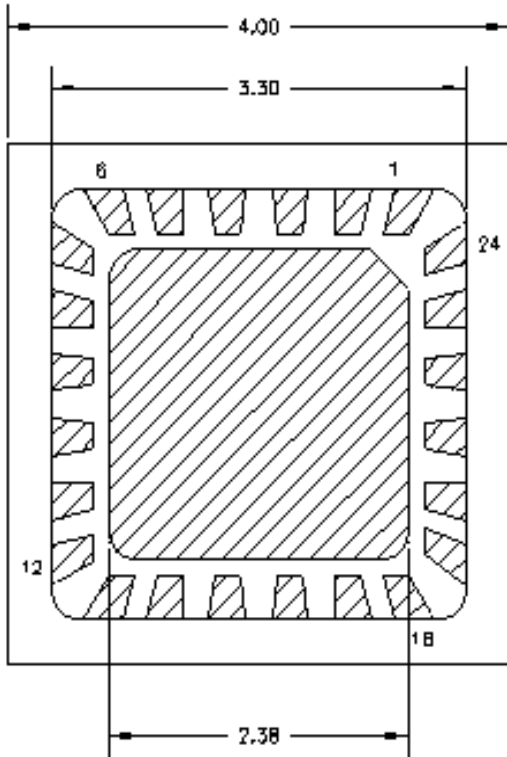


#### Notes:

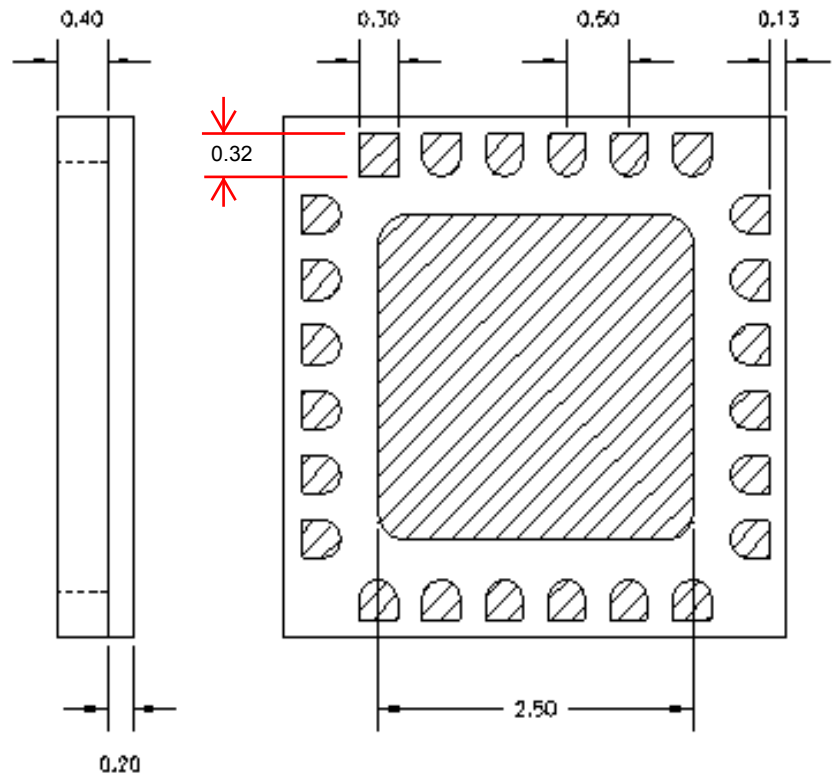
- 1) Package Backside is RF/DC GND and must be well grounded through PCB vias.
- 2) External DC bypass capacitors must be placed as close to package as possible.

**MECHANICAL INFORMATION**

**Outline Drawing**



TOP VIEW



BOTTOM VIEW

Notes:

- 1) 4X4 mm, 24 Lead Ceramic Package Outline Drawing.
- 2) Dimensions are in millimeters.
- 3) Lead and Ground Paddle Plating: Gold
- 4) Package Material: Black Alumina
- 5) All GND Leads and Backside Paddle must be grounded to PCB RF/DC ground.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETERS	UNITS	MAX
VDD	Drain Voltage	V	7
IDD	Drain Current	mA	100
Pdiss	DC Power Dissipation	W	0.4
Pin max	RF Input Power	dBm	13
Toper	Operating Case/Lead Temp Range	°C	-40 to +85
Tch	Channel Temperature	°C	150
Tstg	Storage Temperature	°C	-60 to 150

Exceeding any on of these limits may cause permanent damage.

**Functional Diagram**

